University of Pennsylvania
Department of Electrical and System Engineering
Computer Organization

ESE534, Spring 2010 — Assignment 8: Interconnect — March 29

Due: Monday, April 12, 12:00PM

For this assignment, you will model mesh interconnect and explore design parameters for mesh networks using Toronto's placement and routing tool `vpr`. We will look at the characteristics of two specific designs (apex4, tseng).

1. Use `vpr` in global route mode to determine the minimum global channel width and number of used segments for each design.
2. Create a model for the switching energy consumed by the network when using fully interconnected switchboxes[1] and length one segments. This is the model that can achieve the minimum global channel width identified above. Writeup should describe the composition and derivation of your model.
3. Use your model and data above to estimate the network switching energy required for each design.
4. Use `vpr` in route only mode to determine how the channel width, number of used segments, and delay varies when the segment length is increased from 1 to 10 when using a subset (diamond) switchbox. For each design, make a table with segment length, delay, channel width, and segment count columns. Plot each of {delay, channel width, segment count} versus segment length for each design.
5. Create a model for the switching energy consumed by the detailed routing network using the subset switchbox. You will need to use this model to estimate energy of various architectural and design cases, so parametrize it appropriately. Writeup should describe the composition and derivation of your model.
6. Use your model and `vpr` route results to estimate the network switching energy required for each design at each segment length. Make a table of results and plot energy versus segment length for each design.
7. Identify the segment length that minimizes the network switching energy for each design?
8. How does the minimum energy of the subset switchbox population at the energy minimizing segment length compare to the energy for the fully connected switchbox design?
9. How could leakage energy change your selection of the network energy minimizing segment length in 7? What segment length(s) would you choose under what conditions?

[1] Each wire can connect to any of the wires in any of the 3 adjacent channels.

We are deliberately giving you less guidance for models on this assignment.

- Designs are in: `/home1/e/ese534/hw8/nets/`
- Associated placements are in: `/home1/e/ese534/hw8/place/`
- Assume $V_{dd} = 1.0$V.
- Assume equal switching probability on all LUT outputs of 15%.
- Assume each logic-block length metal wire has $C_{metal} = 1.5 \times 10^{-15}$F.
- Assume each switch box or connection box switch that touches a segment contributes $C_{sw} = 0.4 \times 10^{-15}$F.
- Assume any switch box or connection box switch that is used (enabled so that signals pass through it) provides an additional (internal) switched load of $C_{sw} = 2.0 \times 10^{-15}$F.
- Pay attention to the Logic Block to channel IO population as described in the architecture file. The Mesh-of-Trees paper shows a picture of this connection (Figure 10).
- `vpr` assumes there is a single switch that allows you to make a corner turn between horizontal and vertical segments which do not end in a particular switchbox. Consequently, each track which does not end at a switchbox contributes 1 switch, while a track that does end contributes 6. (We did not count this extra switch in the equations in the Mesh-of-Trees paper.)

vpr notes:

- You can find a copy of the `vpr` executable on the CETS computing systems: `/project/ese/ic/usr/vpr/vpr`
- You can find the manual for vpr: `/home1/e/ese534/hw8/vpr_manual430.pdf`
- To perform this experiment, you will need to create a separate architecture file for each segment length. The architecture file is described in Section 6.2.3 of the vpr manual (around pp. 17–20). For this problem you will especially be interested in Figure 7 and the example on the top of that page that goes with it.
- A base, segment length 1, architecture file is provided in: `/home1/e/ese534/hw8/arch/seg1.txt`
- Keep full population of connection boxes and switch boxes (`Frac_cb` and `Frac_sb` will be 1) for all architectures.
- A typical command for invoking vpr in detail route mode (problem 4) will look like:
  `vpr apex4.net seg1.txt apex4.placed apex4.seg1.route -nodisp -route_only -router_algorithm breadth_first`
  Where:
  - `apex4.net` is the design (the netlist)
  - `seg1.txt` is the architecture file
  - `apex4.placed` is a placement for the design
  - `apex4.seg1.route` is the file in which to store the route for the design
  - `-nodisp` tells it not to bring up the interactive X display
  - `-route_only` tells it not to perform placement (use the given placement)
  - `-router_algorithm breadth_first` tells it to use a channel minimizing router
- If you drop the `-nodisp` option, you can interact with vpr and it will show you pictures of the design. See the vpr manual for further detail on this and other vpr options.
- Note that the vpr output tells you the channel width, delay, and number of segments used. You want "physical segments".
- A typical command for invoking vpr in global route mode (problem 1) will look like:
  `vpr apex4.net seg1.txt apex4.placed apex4.seg1.route -nodisp -route_only -router_algorithm breadth_first -route_type global`
  - `-route_type global` tells it to perform global rather than detail routing