

# ESE534 Computer Organization

Day 9: February 17, 2010  
Interconnect Introduction



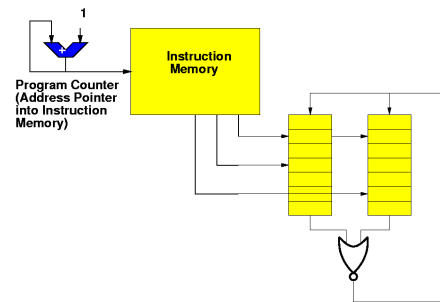
## Today

- Spatially Programmable
- Crossbar
- Hybrid Spatial/Temporal
- Bus
- Ring
- Mesh

## Spatially Programmable

Day 6

## Temporal Programmable

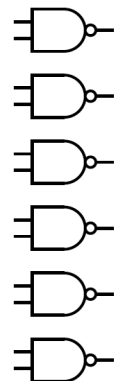


## Spatially Programmable

- Program up any function
- Not sequentialize in time
- *E.g.* Want to build any FSM

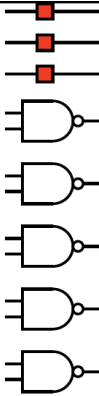
## Needs?

- Need a collection of gates.
- What else will we need?



## Needs

- Need some registers
- Need way to programmably wire gates together

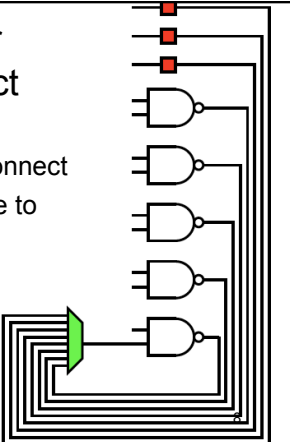


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## Multiplexer Interconnect

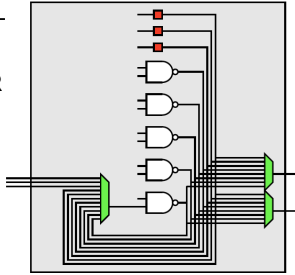
- Use a multiplexer for programmable interconnect
- Can select any source to be an input for a gate
- How big is an N-input multiplexer?



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## Sources?

- What are potential sources?
  - Inputs to circuit (FSM) --
  - Outputs of gates -- G
  - Outputs of registers -- R
- $N = I + G + R$

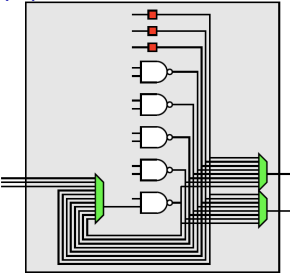


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## Sinks

- Which things need programmable inputs? (and how many?)
  - Circuit outputs -- O
  - Gate -- needs one per input --  $kG$ 
    - Assuming k-input gates
  - Registers -- R
  - $M = O + R + kG$



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## N-input, M-output Multiplexing

- Area?
- Instruction Bits?
- Data input switching
  - Delay?
  - Capacitance Switched?
- Control input switching
  - Delay?
  - Capacitance switched?

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## Mux Programmable Interconnect

- Area  $M \times N = (I + G + R) \times (O + kG + R)$   
 $= kG^2 + \dots$
- Scales faster than gates!

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## Interconnect Costs

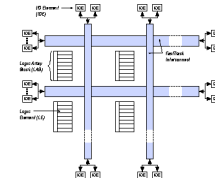
- We can do better than this
  - Touch on a little later in lecture
  - Dig into details later in term
- Even when we do better
- Interconnect can be dominate
  - Area, delay, energy
  - Particularly for Spatial Architectures
  - (saw in HW3, memory can dominate for temporal)

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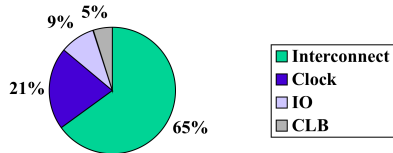
## Dominant Time

Design	Path	Total Delay	LUT Delay	Inter. %
Altera 10K130V-2	LUT-local-LUT	2.5 ns	2.1 ns	16%
	LUT-row-local-LUT	6.6 ns	2.1 ns	68%
	LUT-column-local-LUT	11.1 ns	2.1 ns	81%
	LUT-row-column-local-LUT	15.6 ns	2.1 ns	87%
	LUT-row-fanout-local-LUT (fanout)	28 ns	2.1 ns	90%



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## Dominant Power [Energy]



XC4003A data from Eric Kusse (UCB MS 1997)

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## Crossbar

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## Crossbar

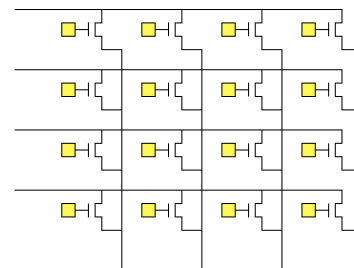
- Allows us to connect any of a set of inputs to any of the outputs.
- This is functionality provided with our muxes

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## Crossbar Structure

- Can be more efficient

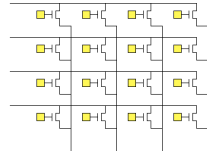


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## Crossbar Costs

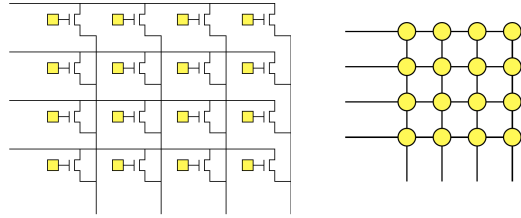
- Area still goes as  $M \times N$
- Delay  $M + N$ 
  - More realistic even for mux implementation
- Energy still goes as  $M \times N$



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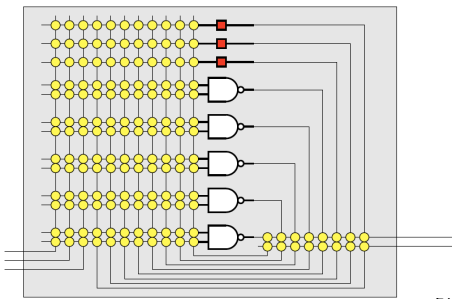
## Crossbar Notation



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## Gates with Crossbar Interconnect



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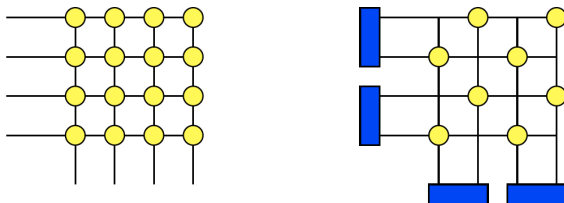
## Switching $w$ -bit words

- Consider grouping outputs (inputs) into  $w$ -bit words
  - E.g. maybe operators are 16-bit ALUs
- How does this change switching requirements?
  - Don't need to switch bit 3 to bit 7
  - Reduces switching needed

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## Switching words ( $w=2$ shown)



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## Switching $w$ -bit words

- $N/w$   $w$ -bit inputs,  $M/w$   $w$ -bit outputs
- Instruction Bits
  - Factor of  $w$  fewer outputs to switch
  - Factor of  $w$  fewer inputs  $\rightarrow M/w(\log_2(N/w))$
- Area:
  - Factor of  $w$  fewer switches
- Delay:
  - Factor of  $w$  fewer sources
- Energy:
  - Factor of  $w$  fewer switches

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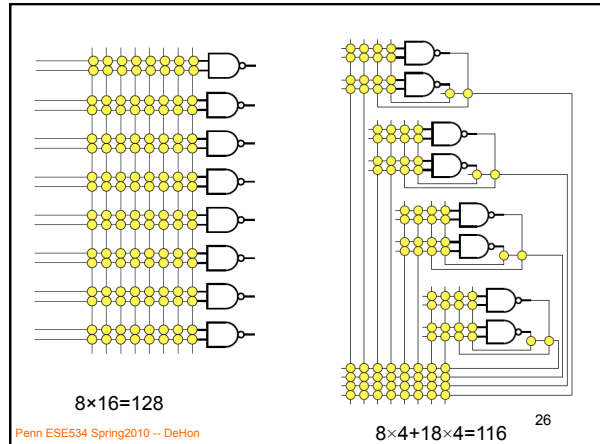
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## Locality

- Maybe we don't need to connect everything to everything?
- Cluster groups of  $C$  things at leaves
  - CG gates, CR registers
  - Limit cluster I/O – CI, CO
  - Crossbar within cluster
  - Crossbar among clusters

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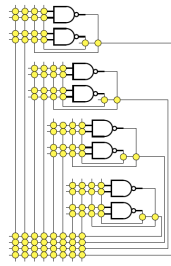


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## Costs

- Cluster Crossbar:
  - Inputs:  $CI+CG+CR$
  - Outputs:  $CO+kCG+CR$
- Master Crossbar:
  - Inputs:  $I+(G/CG)*CO$
  - Outputs:  $O+(G/CG)*CI$
- $(G/CG) \times CO \times (G/CG) \times CI + (G/CG) \times k \times CG^2$
- $G^2 \times (CI \times CO / CG^2) + G \times CG \times k$



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## Costs

- $G^2 \times (CI \times CO / CG^2) + G \times CG \times k$
- Compare:  $kG^2$
- E.g.  $CG=8, CI=CO=2, G=256, k=2$ 
  - $2^{16} \times (2 \times 2 / 8^2) + 2^8 \times 8 \times 2$  vs  $2 \times 2^{16}$
  - $2^{10} + 2^{12}$  vs  $2^{17}$

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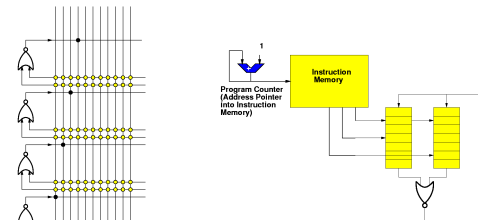
## Hybrid Temporal/Spatial

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## Extremes

- Fully Spatial
- Fully Temporal



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## General Case Between

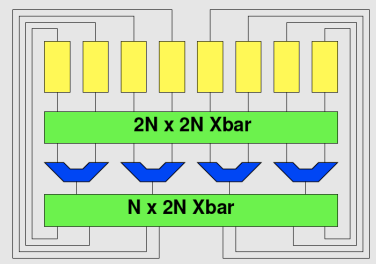
- How many concurrent operators?
- How much serialization?

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## Separate Data Memory and Compute

- Memory banks and compute



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## Crossbar Generalized

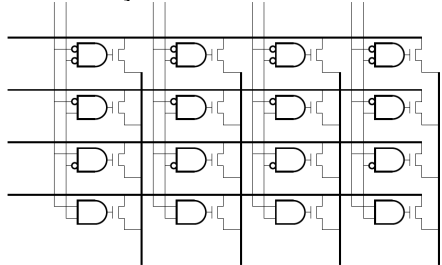
- What's different about this crossbar?

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## Dynamic Crossbar

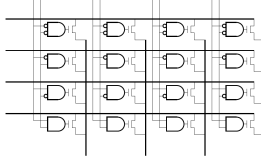
- Need to switch crossbar configuration on each cycle



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## Dynamic Crossbar



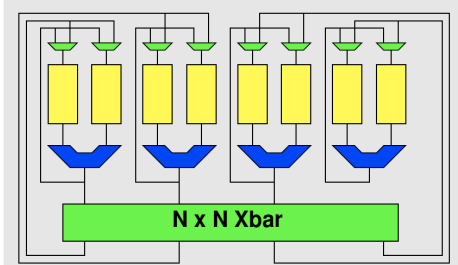
- Switching time matters
- Must also supply crossbar controls
  - More wires into array
  - How many?
- Area
  - Bit-level switching case?  $N (1+\log(N)) M$
  - W-bit word case?  $\sim N (1+\log(N)/W) M$

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## Local Memory Case

- Put memory local to compute



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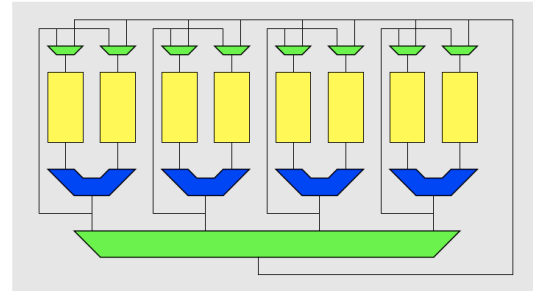
## Reduce Interconnect?

- How can we reduce interconnect?
  - Maybe don't need to deliver a non-local value to every bank on every cycle?
  - Maybe don't need to communicate everywhere?

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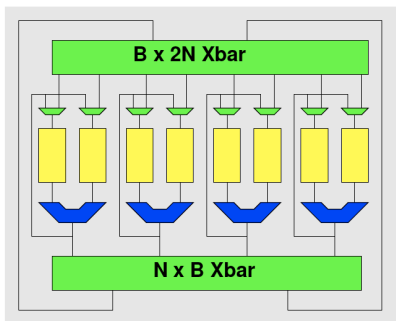
## Single Global Bus



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## Multiple Global Busses

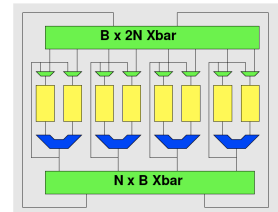


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## Interconnect Resource

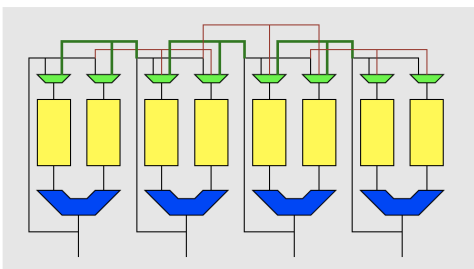
- Can communication B values per cycle
- Could be dominant area/energy
  - Don't want too large
- Could be bottleneck in computation?
  - Don't want too small



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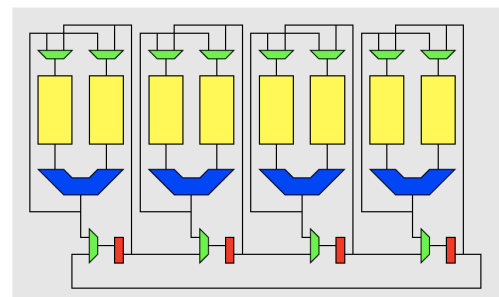
## Nearest Neighbor Interconnect



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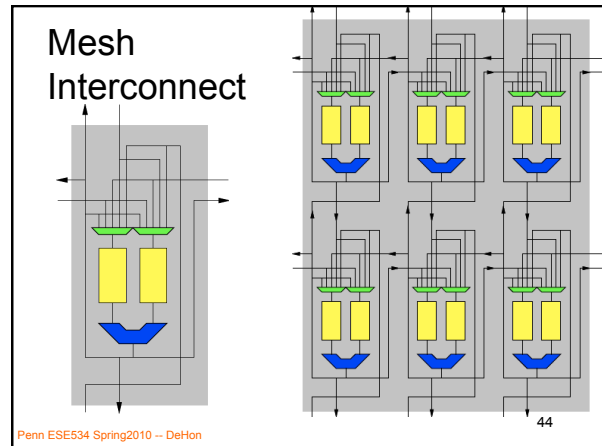
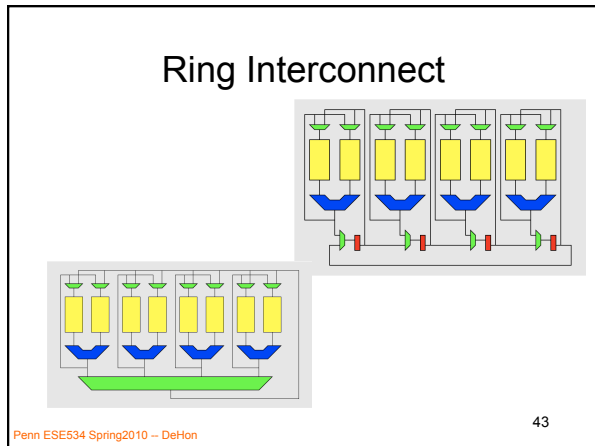
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## Ring Interconnect



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- ### Interconnect Design Space
- Large interconnect design space
  - We will be exploring systematically
    - Day17—20+24
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- ### Admin
- Assignment grades, feedback on blackboard for HW1—HW3
  - Drop Date Friday (André away Friday)
  - No class next Monday (2/22)
  - Class Wednesday (2/24)
  - HW5 due Friday 3/5
    - Think of it as 3/3 with freedom to turnin 3/5
    - Out by Friday...
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- ### Big Ideas
- Interconnect can be programmable
  - Interconnect area/delay/energy can dominate compute area
  - Exploiting structure can reduce area
    - Word structure
    - Locality
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