

University of Pennsylvania
Department of Electrical and System Engineering
Computer Organization

ESE534, Spring 2012 Assignment 3: Scaling and Energy Monday, January 30, 2012

Due: Monday, February 6, 12:00PM

For some of these questions you will need to consult the ITRS. Please use the 2011 edition. You can find ITRS editions at <http://public.itrs.net>.

1. Assuming $V_{dd}=10V$ in a $10\mu m$ process and $V_{dd}=1V$ in a $100nm$ process and assume everything else scales according to ideal scaling.
 - (a) How much faster are the gates than ideal scaling?
 - (b) Assuming you can exploit this gate speedup to increase frequency of operation, how does power density scale between $10\mu m$ and $100nm$? and how does this relate to ideal scaling?
2. Using ITRS 2011 data for $32nm$ (2012) and $9.9nm$ (2022) High Performance (HP) process nodes, how much does the dynamic power gap grow between 2012 and 2022?
 - Part of this problem is intended to familiarize you with the ITRS. You will need to figure out how to find the parameters you need to make this estimate in the ITRS tables. **Hint:** You probably need to look in the PIDS section and tables.
 - State the equations you use for your calculations.
 - Identify the tables and specific entries you use from the ITRS for the technology constants.
 - Note that the ITRS often gives transistor-related values in terms of some value (like capacitance or current) per micron. You will need to scale those to an appropriate (scaled) transistor width to make the proper comparison.

3. Consider a 100 Million transistor integrated circuit chip that will be used in a battery-operated, portable device (*e.g.* tablet). The power budget for this chip is 1W. Assume you can view the chip as containing up to 25 Million CMOS NAND2 gates and each gate drives a total capacitance of $C_g = 5 \times 10^{-16}$ F. This is built in a 45nm process with $V_{dd}=1$ V, $V_{th} = 300$ mV, The critical path for the chip is designed for 1GHz operation. Leakage for each gate is:

$$I_{leak} = 6 \times 10^{-7} \times e^{-\left(\frac{300mV}{40mV}\right)} \text{ A}$$

Saturation current (I) for each gate is:

$$I = 5 \times 10^{-5} (V_{dd} - V_{th}) \text{ A}$$

- (a) Operating at 1GHz, how many gates can be switched in each cycle without exceeding the 1W power limit?
 - (b) If we lower V_{dd} from 1V to 0.5V, what is the new top frequency of operation (assuming 1GHz was the top speed of operation for $V_{dd}=1$ V)? (This question is simply about frequency; do not worry about the power limit for this question, you will come back to that in part (c)). You may assume cycle time is dominated by gate delay and gate delay is proportional to CV/I .
 - (c) Assuming we run the chip at the clock rate from 2(b) with $V_{dd}=0.5$ V:
 - i. How many gates can switch in a cycle without exceeding the 1W power limit?
 - ii. What is the ratio of gates switchable per **second** between $V_{dd}=0.5$ V and $V_{dd}=1.0$ V operation?
4. Using ITRS 2011 data for 32nm (2012), identify the operating frequency at which leakage energy and dynamic energy are equal for the three processes variants: High Performance (HP), Low Operating Power (LOP) and Low Standby Power (LSTP). You may assume a uniform activity factor, α , of 0.10. State additional assumptions you need to make in order to perform this estimate.

5. This question effectively asks you to review the Day 6 preclass exercise 2 and consider different threshold voltages. [This changed on 2/1/12]
- (a) Write the equation for total Energy considering leakage as a function of V .
- Assume cycle time is: $T_{cycle} = (1\text{fF} \times V)/I$
 - Assume $I = 100\text{nA} \times 10^{((V-V_{th})/90\text{mV})}$
(Note: difference here from preclass is V_{th} vs. 360mV)
 - Assume $I_{chip-leak} = 10^9 \times 100\text{nA} \times 10^{((-V_{th})/90\text{mV})}$
(Note: difference here from preclass is V_{th} vs. 360mV)
 - Assume energy is both switching and leakage:
 - $E_{switch} = 10\text{nF} \times V^2$
 - $E_{leak} = T_{cycle} \times V \times I_{chip-leak}$
 - $E = E_{switch} + E_{leak}$
- (b) How does the minimum energy relate to V_{th} ?
- (c) How does the cycle time at minimum energy relate to V_{th} ?
6. Using your results from the problems above, explain why your cell phone processor runs slower than your desktop or laptop processor.
- You may consider an iPhone 4S as your cell phone.
 - You may consider an Intel Xeon E3-1230 as your desktop processor.
 - If you don't know the clock frequencies and other characteristics of the appropriate processors, you may want to search the web.