ESE534: Computer Organization

Day 23: April 11, 2012
Control

Previously

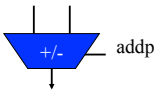
- Looked broadly at instruction effects
- Explored structural components of computation
  - Interconnect, compute, retiming
- Explored operator sharing/time-multiplexing
- Explored branching for code compactness

Today

- Instantaneous compute requirement vs. total compute requirement
- Control
  - data-dependent operations
- Different forms
  - local
  - instruction selection
- Control granularity as another parameter in our architecture space

Control

- **Control**: That point where the data affects the instruction stream (operation selection)
  - Typical manifestation
    - data dependent branching
      - if (a!=0) OpA else OpB
      - bne
    - data dependent state transitions
      - new => goto S0
      - else => stay
    - data dependent operation selection

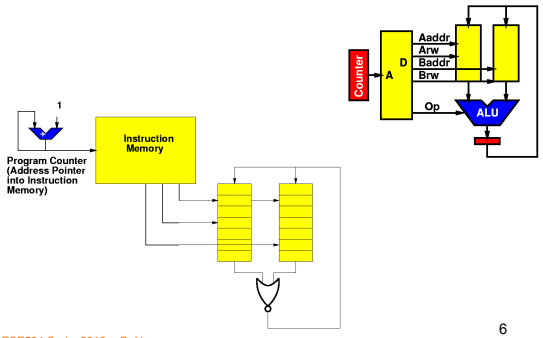


Control

- **Viewpoint**: can have instruction stream sequence without control
  - *I.e.* static/data-independent progression through sequence of instructions is control free
    - C0→C1→C2→C0→C1→C2→C0→…
  - Similarly, FSM w/ no data inputs
  - *E.g.* HW4…non-branching multiplier

Day 8 and 9

Programmable Architecture



Terminology (reminder)

- **Primitive Instruction (*pinst*)**
  - Collection of bits which tell a bit-processing element what to do
  - Includes:
    - select compute operation
    - input sources in space (interconnect)
    - input sources in time (retiming)
- **Configuration Context**
  - Collection of all bits (*pinsts*) which describe machine's behavior on one cycle

Back to "Any" Computation

- Design must handle all potential inputs (computing scenarios)
- Requires sufficient generality
- However, computation for **any** given input may be *much* smaller than general case.

Instantaneous compute << potential compute

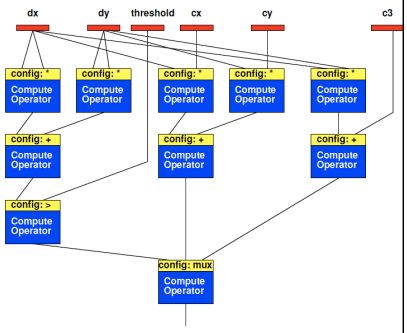
Preclass 1

```
if ((dx*dx+dy*dy)>threshold)
   z=cx*dx+cy*dy
else
   z=dx*dy+c3
```

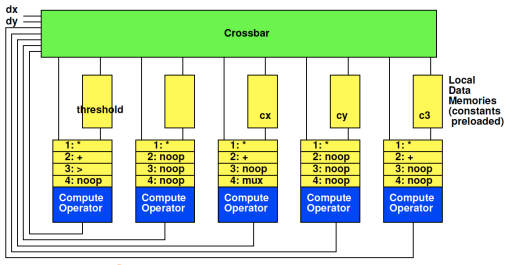
- How many operations performed?
- Cycles?
- Compute Blocks needed?

Preclass 1

- Delay?
- Operations?



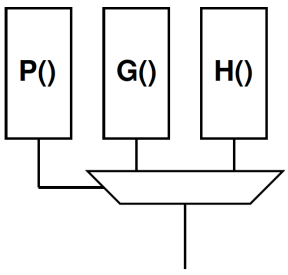
Preclass



- Operations?
- Cycles?
- How did it do that? (reduce delay)

If-Conversion

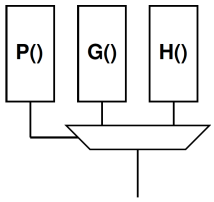
```
if (P())
   G()
else
   H()
```



If-Conversion

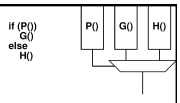
- Trade-off:
  - –Latency
  - –Work

```
if (P())
   G()
else
   H()
```

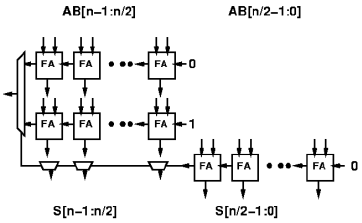


Day 3

Idea

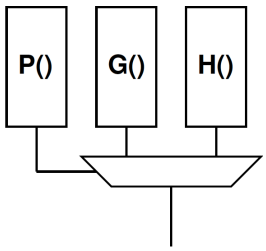


- Compute both possible values and select correct result when we know the answer



If-Conversion ~= Predicated Operations

```
if (P())
   G()
else
   H()
```



P1=P()
P2=!P1
P1 G()
P2 H()

P1=t1>t2
P2=!P1
…
P1 z=t4
P2 z=t5

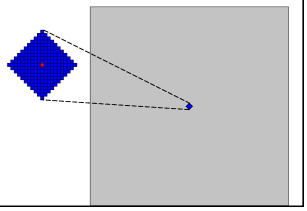
Why important?

Instruction Control Latency

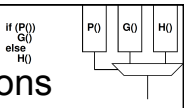
- For time-multiplexed (data-independent) sequencing
  - – Can pipeline instruction distribution
  - – Instruction memory read
- Now decision→PC→distribution→read latency becomes part of critical path

Clock Cycle Radius

- Radius of logic can reach in one cycle (45 nm)
  - – Radius 10 (preclass 19: L_{seg}=5 → 50ps)
    - Few hundred PEs
  - – Chip side 600-700 PE
    - 400-500 thousand PEs
  - – 100s of cycles to cross

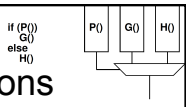


Two Control Options



1. Local control
   - – unify choices
     - build all options into spatial compute structure and select operation → Mux-conversion
2. Instruction selection
   - – provide a different instruction (instruction sequence) for each option
   - – selection occurs when chose which instruction(s) to issue

Two Control Options



1. Local control
2. Instruction selection

May use both within an application

- Local control in critical path, inner-loops, where latency rather than parallelism limited
- Instruction-selection coarse-grain selection
  - At coarse level
  - Or where have plenty of task parallelism so latency not limit computation

Video Decoder

- *E.g.* Video decoder [frame rate = 33ms]
  - if (packet==FRAME)
    - if (type==I-FRAME)
      - I-FRAME computation
    - else if (type==B-FRAME)
      - B-FRAME computation
- Millions of cycles per frame
  - Instruction control between frames
    - Local control within frames

Packet Processing

- If IP-V6 packet
  - ….
- If IP-V4 packet
  - …
- If VoiP packet
  - …
- If modem packet
  - ….

Control Granularity

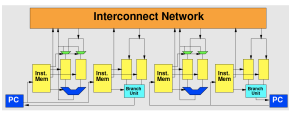
Architectural Parameter(s)
For Instruction Selection

Preclass

```
WAIT:  if (in.type==header)
         cnt=in.header_payload_size;
         checksum=0;
         goto RECEIVE;
       else goto WAIT;
RECEIVE: checksum=checksum xor in;
       data[packet][cnt]=in;
       cnt--;
       if (cnt==0) goto CHECK;
       else goto RECEIVE;
CHECK: if (in==checksum)
         packet++;
       goto WAIT
```


Preclass

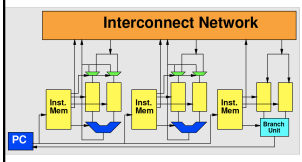
- How support
  - Two ports
  - On two 2-issue VLIWs
  - with separate controllers?




```
WAIT:  if (in.type==header)
         cnt=in.header_payload_size;
         checksum=0;
         goto RECEIVE;
       else goto WAIT;
RECEIVE: checksum=checksum
  xor in;
       data[packet][cnt]=in;
       cnt--;
       if (cnt==0) goto CHECK;
       else goto RECEIVE;
CHECK: if (in==checksum)
         packet++;
       goto WAIT
```

Preclass

- How support
  - two ports
  - on one 3-issue VLIW
  - with single controller?




```
WAIT:  if (in.type==header)
         cnt=in.header_payload_size;
         checksum=0;
         goto RECEIVE;
       else goto WAIT;
RECEIVE: checksum=checksum
  xor in;
         data[packet][cnt]=in;
         cnt--;
         if (cnt==0) goto CHECK;
         else goto RECEIVE;
CHECK: if (in==checksum)
         packet++;
         goto WAIT
```

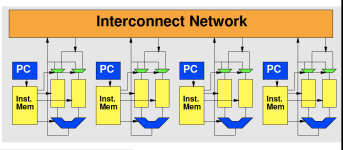

Instruction Control

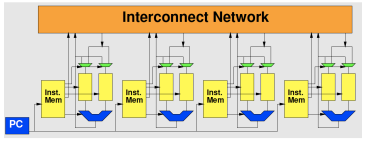
- If FSMs (ports) advance orthogonally
  - (really independent control)
  - context depth => product of states
    - Product of PCs
  - *I.e.* w/ single controller (PC)
    - must create product FSM
    - which may lead to state explosion
      - N FSMs, with S states => S^N product states

Day 10

Architectural Differences

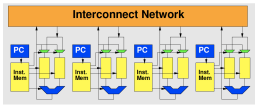
- What differentiates a VLIW from a multicore?

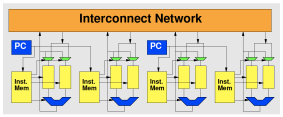


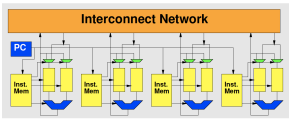


Architectural Questions

- How many pinsts/controller?







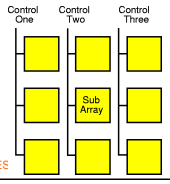
Day 11

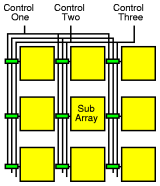
Architecture Taxonomy

PCs	Pints/PC	depth	width	Architecture
0	N	1	1	FPGA
1	N (48,640)	8	1	Tabula ABAX (A1EC04)
1	1	1024	32	Scalar Processor (RISC)
1	N	D	W	VLIW (superscalar)
1	1	Small	W*N	SIMD, GPU, Vector
N	1	D	W	MIMD
16	1 (4?)	2048	64	16-core

Architectural Questions

- How many pinsts/controller?
- Fixed or Configurable assignment of controllers to pinsts?
  - …what level of granularity?





Architectural Questions

- Effects of:
  - Too many controllers?
  - Too few controllers?
  - Fixed controller assignment?
  - Configurable controller assignment?

Architectural Questions

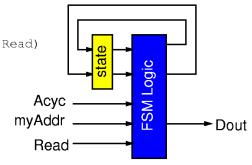
- Too many:
  - wasted space on extra controllers
  - synchronization?
- Too few:
  - product state space and/or underuse logic
- Fixed:
  - underuse logic if when region too big
- Configurable:
  - cost interconnect, slower distribution

FSM Control Factoring Case Study

FSM Example (local control)

FSM Description

```
Idle  (00):
      if (Acyc & myAddr & Read)
          goto Wait1
      else
          goto Idle
Wait1 (01):
      goto Data
Data  (10):
      Assert Dout
      goto Wait2
Wait2 (11):
      goto Idle
```



FSM Logic

```
Dout = S1*/S0
NS0 =  /S1*/S0*Acyc*myAddr*Read + S1*/S0
NS1 = /S1*S0 + S1*/S0
```

4 4-LUTs
2 LUT Delays

FSM Example

Context 0 (S1=0)

```
Dout = 0
NS0 = /S0*Acyc*myAddr*Read
NS1 = S0
```

3 4-LUTs
1 LUT Delay

Context 1 (S1=1)

```
Dout = /S0
NS0 = /S0
NS1 = /S0
```


Local Control

- LUTs used ≠ LUT evaluations produced
- → Counting LUTs not tell cycle-by-cycle LUT needs

FSM Example (Instruction)

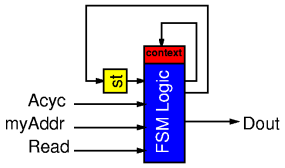
Context 0 (S1=0)

```
Dout = 0
NS0 = /S0*Acyc*myAddr*Read
NS1 = S0
```

3 4-LUTs
1 LUT Delay

Context 1 (S1=1)

```
Dout = /S0
NS0 = /S0
NS1 = /S0
```

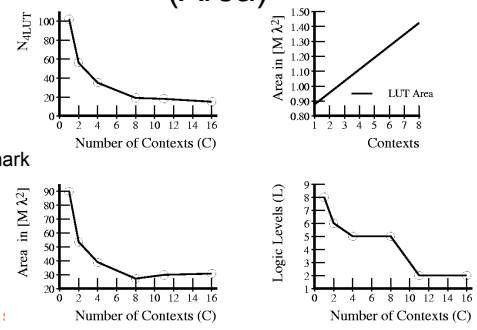


FSM Example

- FSM -- canonical "control" structure
  - captures many of these properties
  - can implement with deep multicontext
    - instruction selection
  - can implement as multilevel logic
    - unify, use local control
- Serve to build intuition

Partitioning versus Contexts (Area)

CSE benchmark



Partitioning versus Contexts (Heuristic)

- Start with dense `mustang` state encodings
- Greedily pick state bit that produces
  - least greatest area split
  - least greatest delay split
- Repeat until have desired number of contexts

Partition to Fixed Number of Contexts

FSM	States	Best Single Context	Area Ratio by Number of Context (Dense Encodings) 1	2	4	8	16	32	64
Area Target									
average ratio		1.00	1.51	0.86	0.63	0.56	0.70	1.09	1.92
average delta		0.00	-0.27	0.33	1.27	2.18	2.70	3.03	3.06
Delay Target									
average ratio		1.00	1.45	1.05	0.59	0.50	0.62	0.95	1.67
average delta		0.00	-0.91	-0.48	0.06	0.64	0.91	1.15	1.21

Extend Comparison to Memory

- Fully local => compute with LUTs
- Fully partitioned => lookup logic (context) in memory and compute logic
- How compare to fully memory?
  - Simply lookup result in table?

Memory FSM Compare (small)

FSM	states	ins	outs	**Min area** ($M\lambda^2$)	Integral Addr. & Data Organization	**Memory area** ($M\lambda^2$)	**FPGA area** ($M\lambda^2$)	**8-ctx DPGA area** ($M\lambda^2$)
bbtas	6	2	2	0.1	$2^5 \times 5$	0.2	6.1	7.1
dk15	4	3	5	0.3	$2^5 \times 7$	0.3	21.9	10.0
dk17	8	2	3	0.2	$2^5 \times 6$	0.2	16.7	8.5
dk512	15	1	3	0.3	$2^5 \times 7$	0.3	17.6	10.0
mc	4	3	5	0.3	$2^5 \times 7$	0.3	7.0	10.0
modulo12	12	1	1	0.1	$2^5 \times 5$	0.2	10.5	7.1
beecount	7	3	4	0.5	$2^5 \times 7$	0.5	12.3	10.0
dk14	7	3	5	0.5	$2^5 \times 8$	0.6	50.9	11.4
dk16	27	2	3	1.0	$2^7 \times 8$	1.3	70.2	11.4
donfile	24	2	1	0.7	$2^7 \times 6$	0.9	40.4	8.5
s27	6	4	1	0.5	$2^7 \times 4$	0.6	4.4	5.7
s8	5	4	1	0.4	$2^7 \times 4$	0.6	10.5	5.7
bbara	10	4	2	1.2	$2^8 \times 6$	1.8	21.9	11.4
ex6	8	5	8	3.4	$2^8 \times 11$	3.4	50.0	15.7
ex4	14	6	9	14.0	$2^{10} \times 13$	16.0	18.4	18.5
bbsse	16	7	7	27.0	$2^{11} \times 11$	27.0	43.9	21.4
cse	16	7	7	27.0	$2^{11} \times 11$	27.0	72.9	27.1
tbk	32	6	3	19.7	$2^{11} \times 8$	19.7	298.5	68.4

Memory FSM Compare (large)

FSM	states	ins	outs	**Min area** ($M\lambda^2$)	Integral Addr. & Data Organization	**Memory area** ($M\lambda^2$)	**FPGA area** ($M\lambda^2$)	**8-ctx DPGA area** ($M\lambda^2$)
sse	16	7	7	27.0	$2^{11} \times 11$	27.0	43.9	21.4
s386	13	7	7	22.9	$2^{11} \times 11$	27.0	36.9	18.5
keyb	19	7	2	20.4	$2^{12} \times 7$	34.4	98.3	31.3
planet	48	7	19	184.3	$2^{13} \times 25$	245.8	131.7	54.1
pma	24	8	8	95.8	$2^{13} \times 13$	127.8	72.0	34.2
s1	20	8	6	67.6	$2^{13} \times 11$	108.1	120.3	62.7
s1a	20	8	6	67.6	$2^{13} \times 11$	108.1	63.2	54.1
ex1	20	9	19	294.9	$2^{14} \times 24$	471.9	105.4	55.5
s1488	48	8	19	368.6	$2^{14} \times 25$	491.5	133.5	74.0
styr	30	9	10	276.5	$2^{14} \times 15$	294.9	163.3	57.0
s208	18	11	2	309.7	$2^{16} \times 7$	550.5	33.4	12.8
sand	32	11	9	1101.0	$2^{16} \times 14$	1101.0	156.3	62.7
s820	25	18	19	188743.7	$2^{23} \times 24$	241591.9	80.8	64.1
s420	18	19	2	79272.3	$2^{24} \times 7$	140928.6	35.1	14.2
s510	47	19	7	384408.9	$2^{25} \times 13$	523449.1	47.4	25.6

Memory FSM Compare (notes)

- Memory selected was "optimally" sized to problem
  - in practice, not get to pick memory allocation/organization for each FSM
  - no interconnect charged
- Memory operate in single cycle
  - but cycle slowing with inputs
- Smaller for <11 state+input bits
- Memory size not affected by CAD quality (FPGA/DPGA is)

Admin

- Reading for Monday on Blackboard
- FM2 Monday

Big Ideas [MSB Ideas]

- **Control**: where data effects instructions (operation)
- Two forms:
  - local control
    - all ops resident → fast selection
  - instruction selection
    - may allow us to reduce instantaneous work requirements
    - introduce issues
      - depth, granularity, instruction load and select time

Big Ideas [MSB-1 Ideas]

- If-Conversion
  - Latency vs. work tradeoff
- Intuition → explored canonical FSM case
  - few context can reduce LUT requirements considerably (factor dissimilar logic)
  - similar logic more efficient in local control
  - overall, moderate contexts (*e.g.* 8)
    - exploits both properties … better than extremes