Consider the following 1D placement for the logic:

\[
A = i_0 \cdot i_1; \quad B = A + i_2; \quad C = i_0 \cdot i_3; \quad D = B + C; \quad o_4 = D
\]

Assume:
- Input pins are on the left of the gate.
- Gate output is the rightmost pin on the gate.

1. What is the maximum channel density? [ ]

2. Assign the net connections to channels to minimize the number of channels required.

3. How many channels do you need to route the all the nets? [ ]