**Problem:** Using the library of gates shown below, implement this netlist shown.

- What is the cost if you cover each drawn gate directly with its associated gate in the library (i.e. use only inverter and nand2 gates)?
- What portions of the graph can the nand3 cover?
- What assembly of gates has the least area?
- What area does this achieve?

**Library** (numbers on right are area cost of each gate)

- Inverter: 2
- Nand2: 3
- Nand3: 4
- Nand4: 6