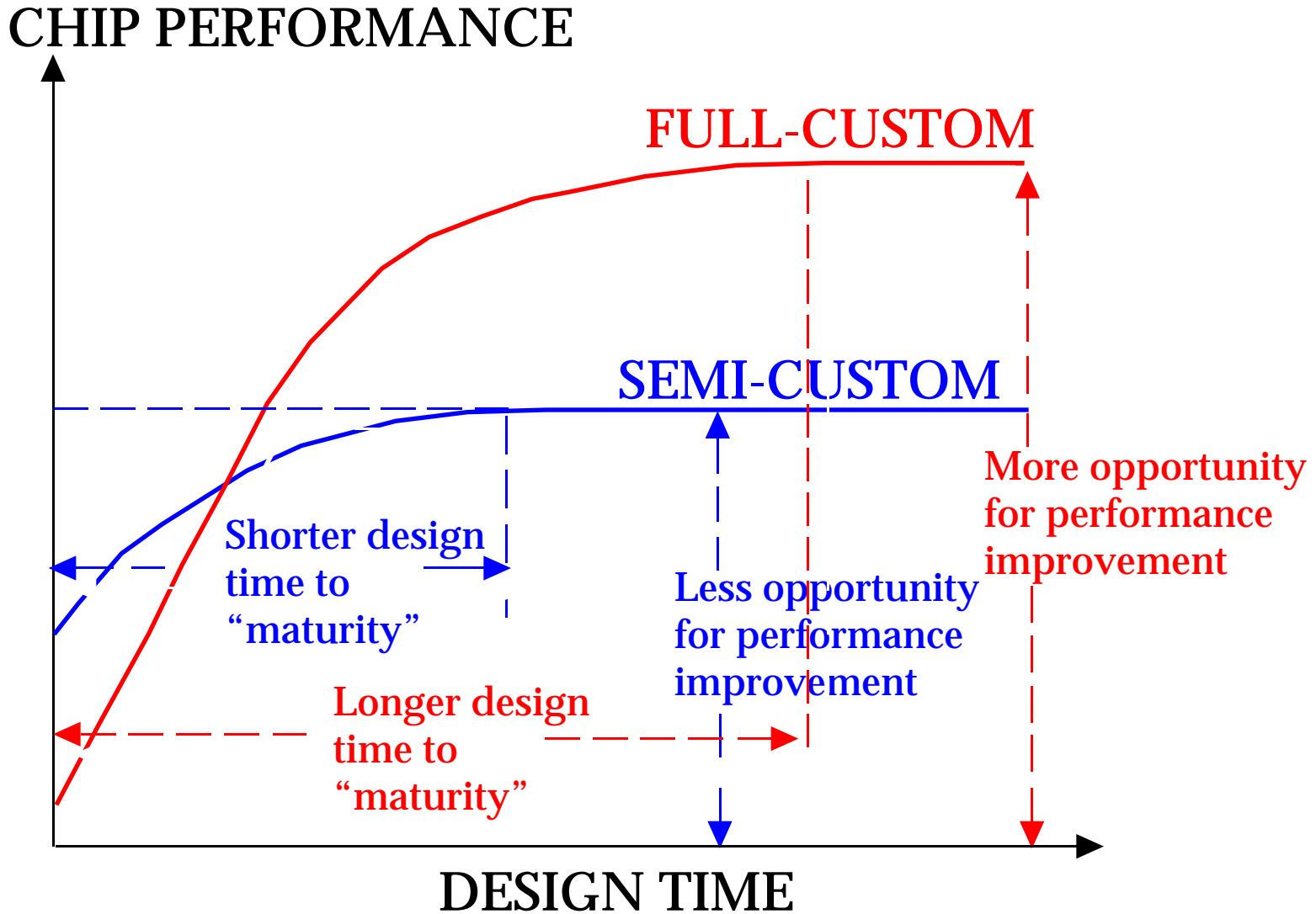


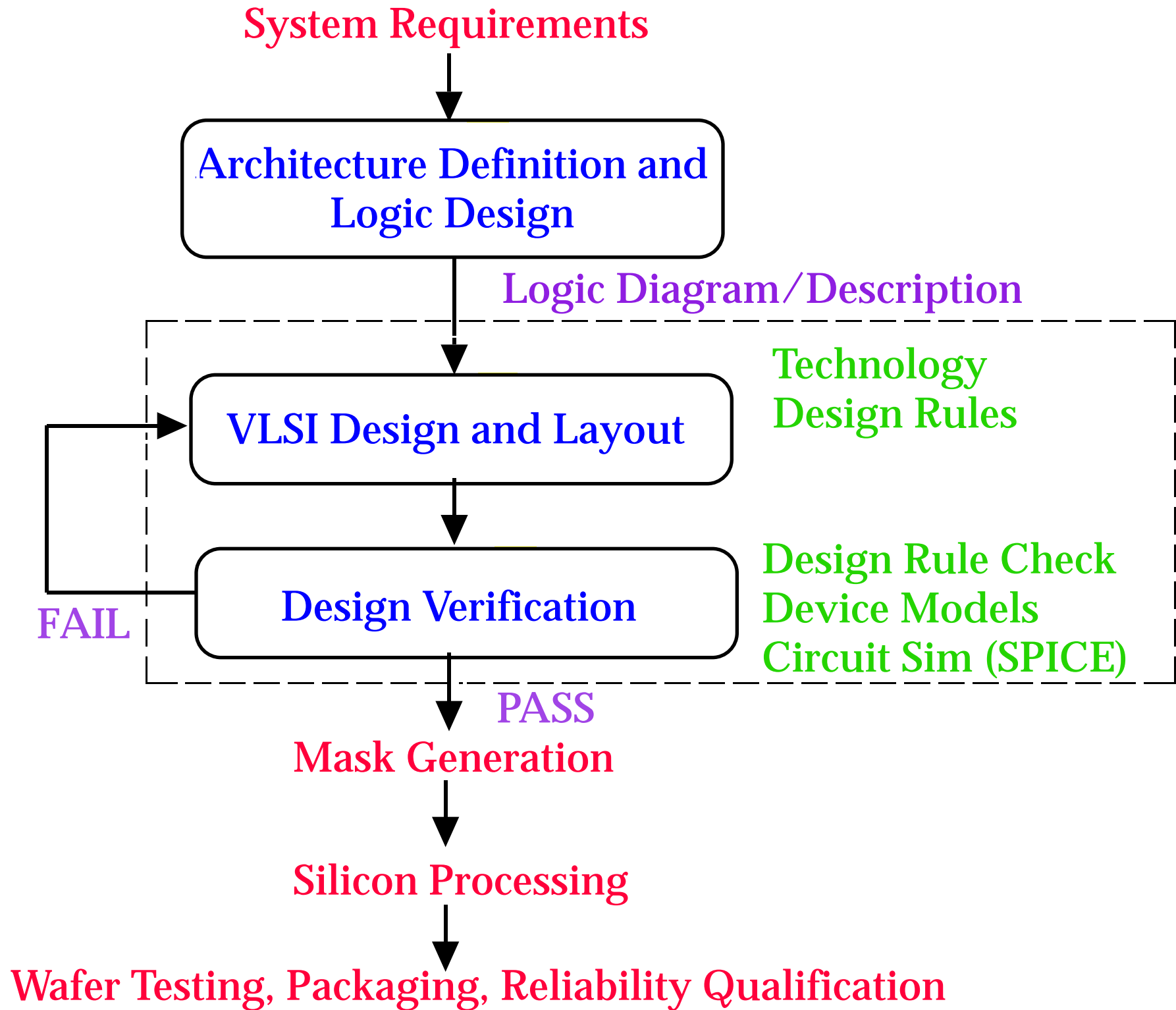
ESE 570 VLSI DESIGN METHODOLOGIES

VLSI TECHNOLOGY AND DESIGN DRIVERS

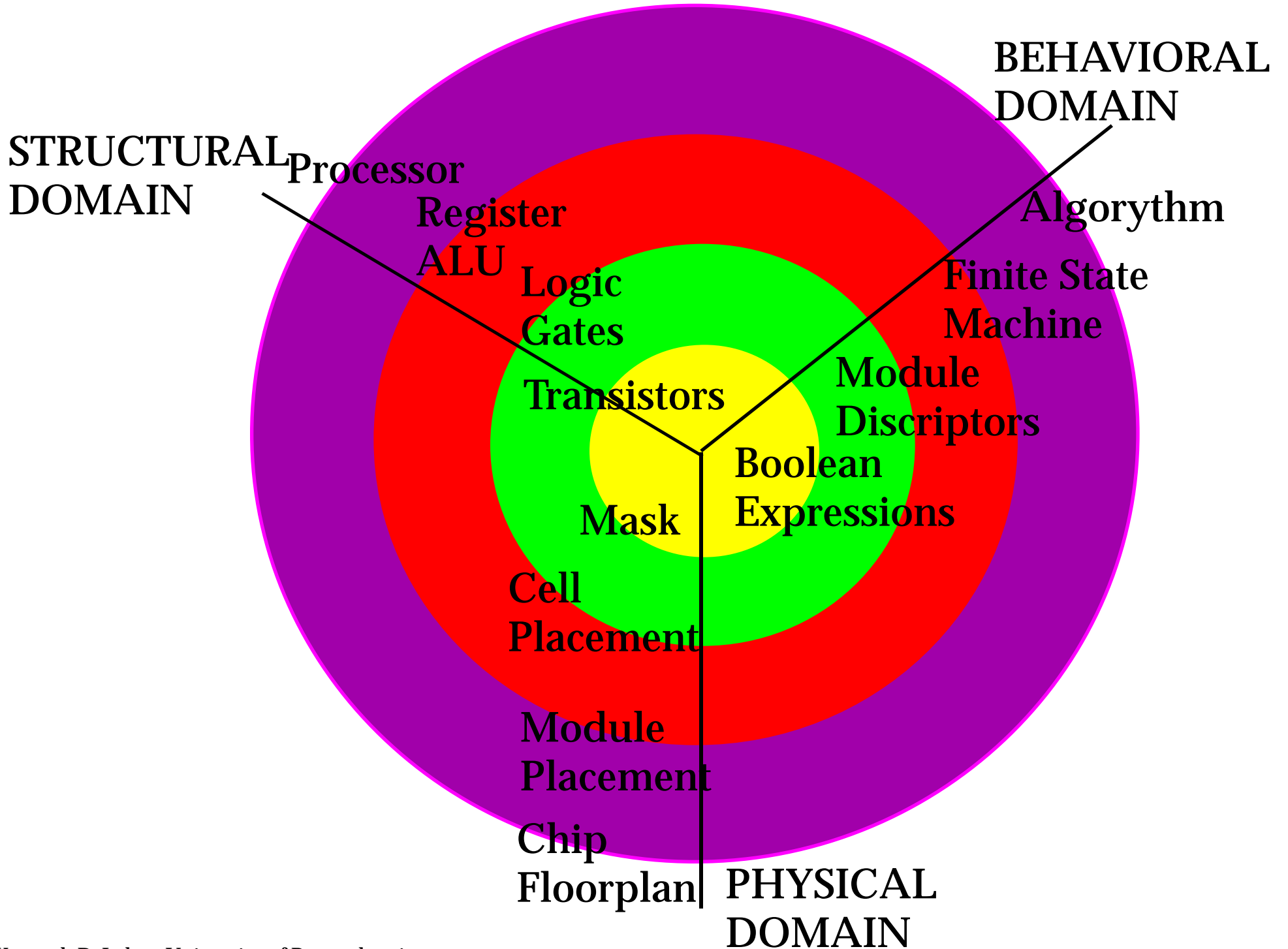
- > LESS AREA, MORE COMPACTNESS AT ALL SYSTEM LEVELS**
- > LESS POWER CONSUMPTION**
- > FEWER CHIPS/COMPONENTS PER BOARD AND SYSTEM**
- > HIGHER RELIABILITY, DUE TO IMPROVED ON-CHIP INTERCONNECTS**
- > HIGHER SPEED DUE TO REDUCED INTERCONNECT LENGTH**
- > MANUFACTURING COST REDUCTIONS**

IMPACT OF DIFFERENT VLSI DESIGN STYLES ON DESIGN CYCLE TIME AND ACHIEVABLE CHIP PERFORMANCE

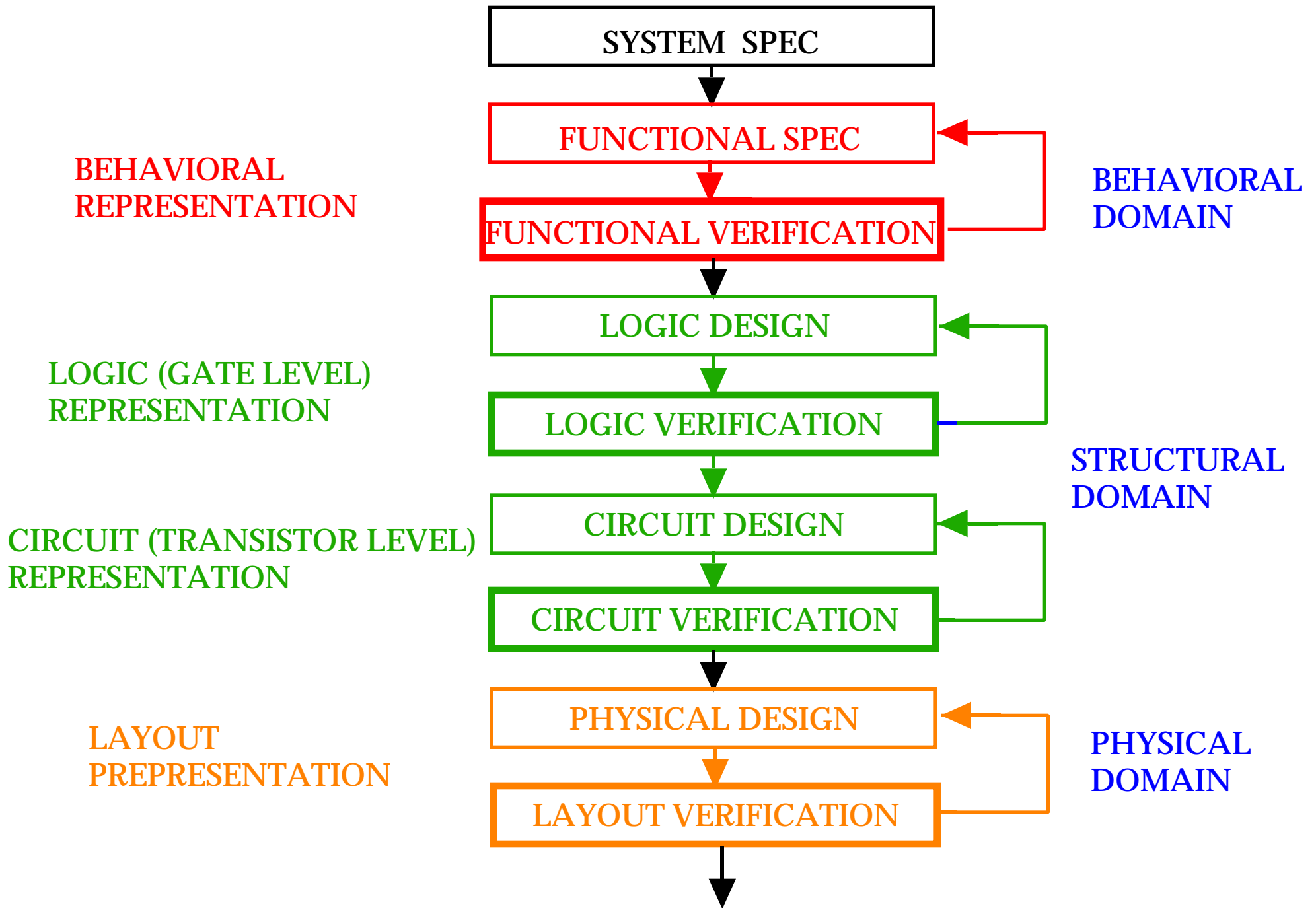




VLSI DESIGN FLOW - 3 DOMAIN REPRESENTATIONS

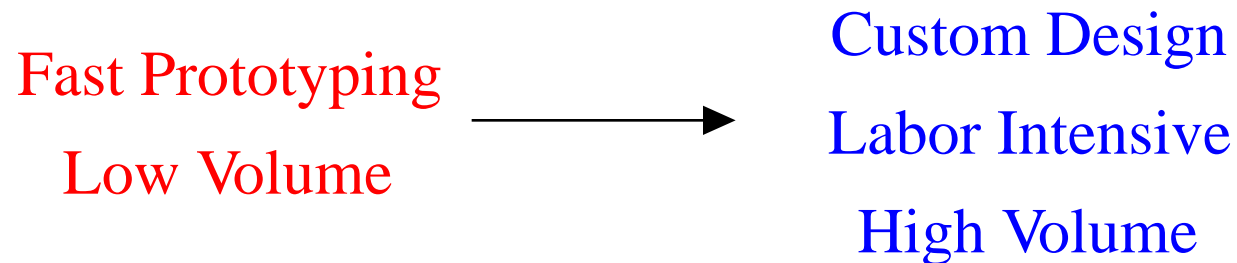


SIMPLIFIED VLSI DESIGN FLOW VIEW IN THREE DOMAINS



OBJECTIVE: transfer design description in behavioral domain into a fully equivalent design descriptions in the other domains.

- > Guiding Design Organization Principles
- > Design Options Available to CMOS IC Designers



Design Strategies

Design Parameters By Which Design Success Is Measured:

Performance Specs - function, timing, speed, power

Size of Die - manufacturing cost

Time to Design - engineering cost and schedule

Ease of Test Generation & Testability - engineering cost, manufacturing cost, schedule

Design is a continuous tradeoff to achieve performance specs with adequate results in all the other parameters.

Structured Design Strategies

Strategies common for complex hardware and software projects.

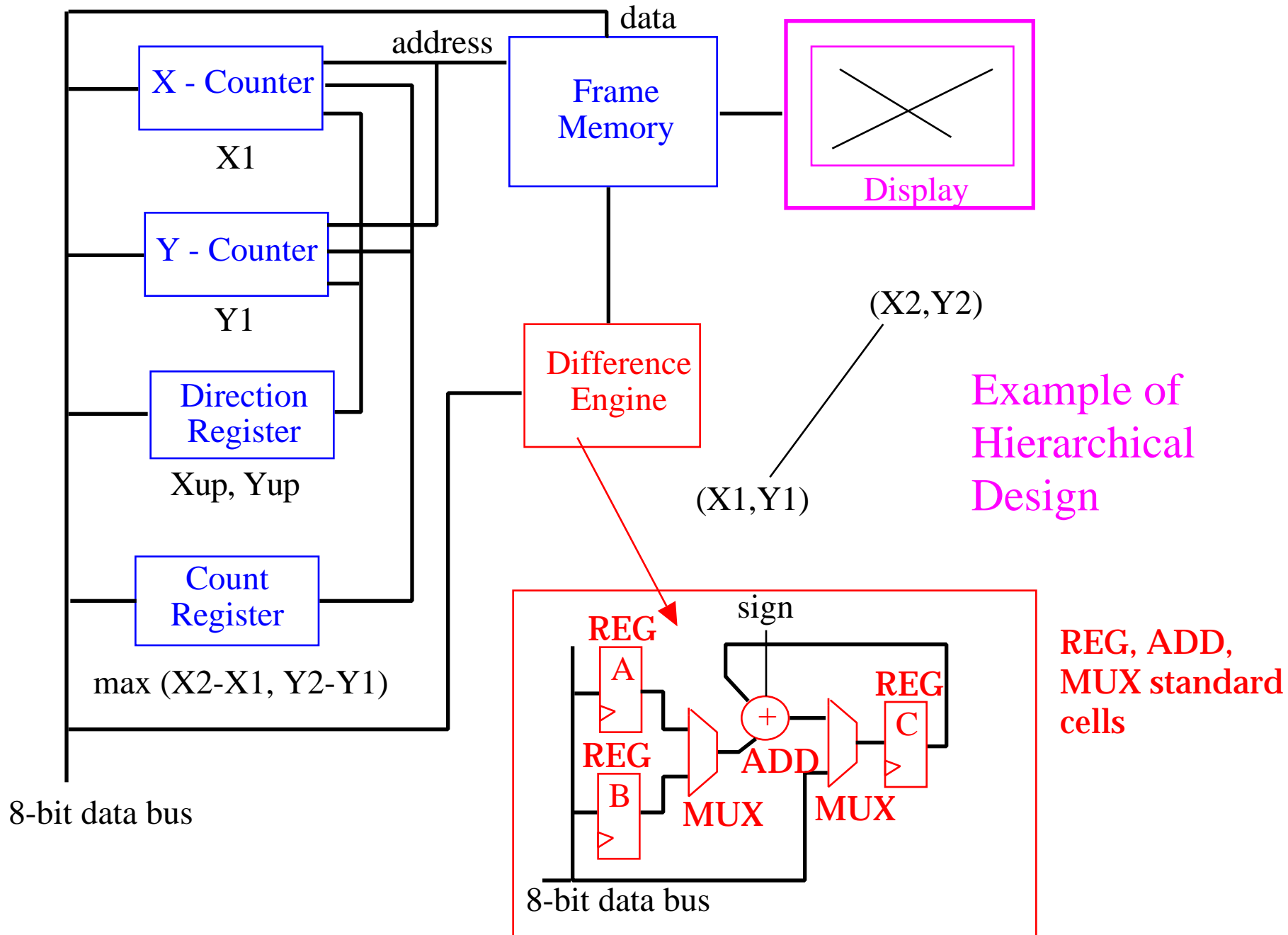
- > **Hierarchy**: Subdivide the design into several levels of sub-modules
- > **Modularity**: Define sub-modules unambiguously & well defined interfaces
- > **Regularity**: Subdivide to max number of similar sub-modules at each level
- > **Locality**: Max local connections, keeping critical paths within module boundaries

MODULARITY

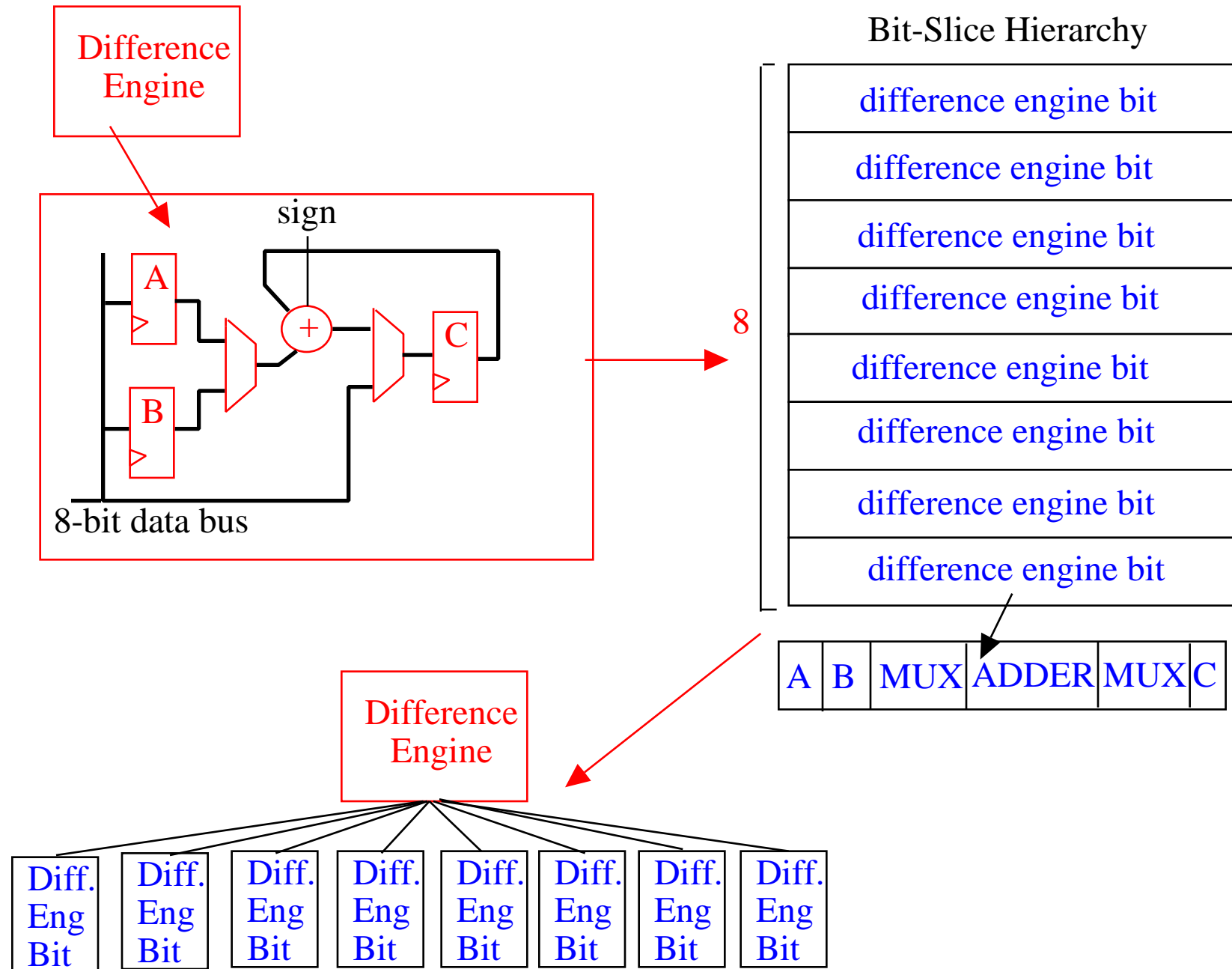
ADDS TO HIERARCHY AND REGULARITY THE QUALITIES OF
WELL DEFINED FUNCTIONS AND INTERFACES

- > Unambiguous functions
- > Well defined behavioral, structural, and physical interfaces
- > Enables modules to be individually designed and evaluated.

TOP LEVEL DIAGRAM OF A RASTER GRAPHICS VECTOR GENERATOR



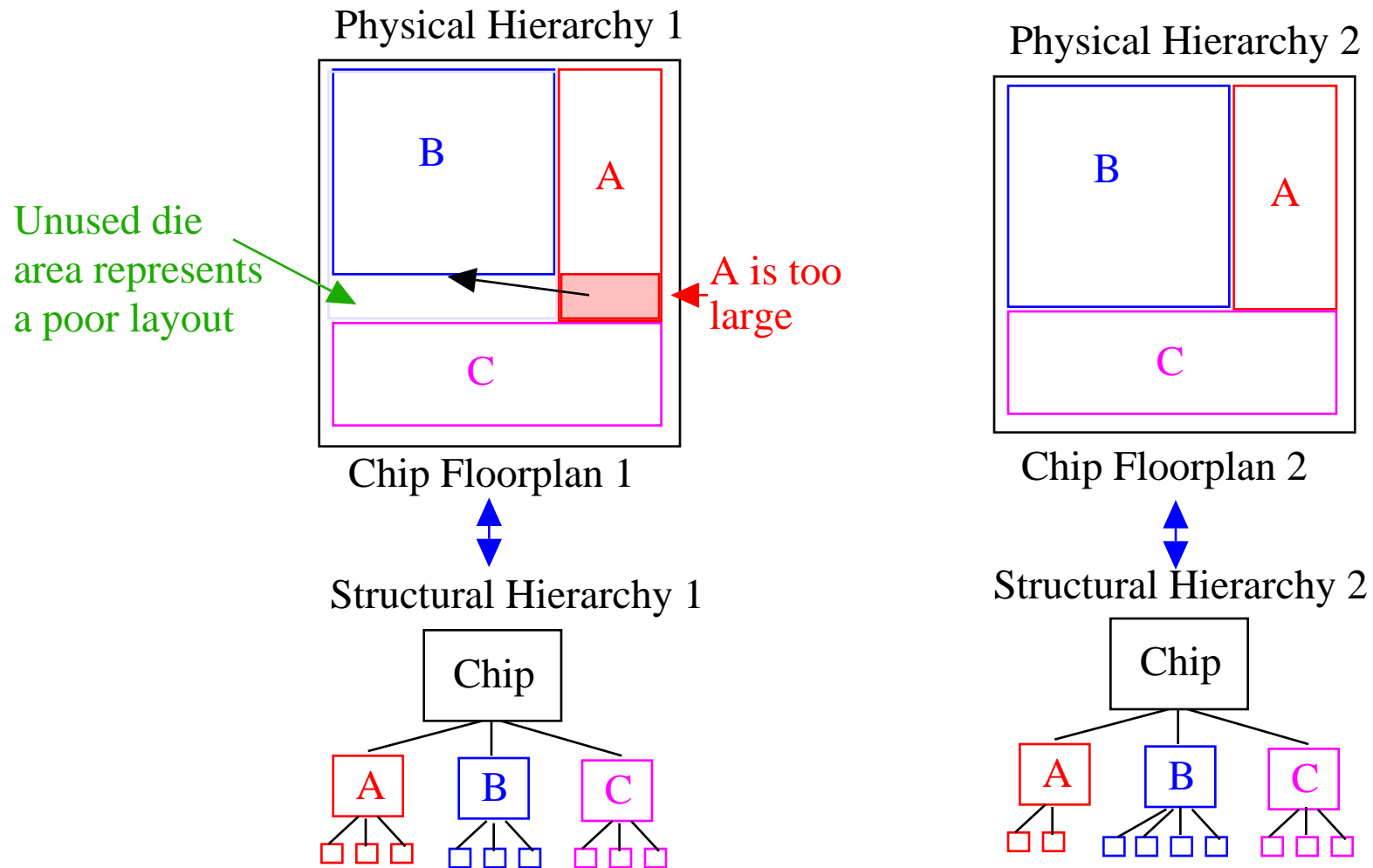
PHYSICAL MODULARITY FOR DIFFERENCE ENGINE BASED ON 8 IDENTICAL BIT SLICES



MAINTAIN IDENTICAL HIERARCHIES IN BEHAVIORAL, STRUCTURAL AND PHYSICAL DOMAINS

FLOORPLANNING

Mapping Structural Hierarchy into Physical Hierarchy



REGULARITY

DESIGN THE CHIP HIERARCHY INTO **IDENTICAL OR SIMILAR** MODULES
EXTENDED USE OF REGULARITY **SIMPLIFIES** THE DESIGN PROCESS
REGULARITY CAN EXIST AT **ALL LEVELS** OF DESIGN HIERARCHY

- > **Circuit Level:** uniform transistor sizes rather than manually optimizing each device.
- > **Logic Level:** identical gate structures rather than customize every gate.
- > **Architecture Level:** construct architectures that use a number of identical processor structures

LOCALITY

TIME LOCALITY: modules see a common clock and synchronous timing is applied.

- > Robust clock generation and distribution is critical
- > Critical paths, where possible, are to be kept within module boundaries
- > Any global module to module signal should have an entire clock cycle to traverse the chip.
- > Replicate logic, if necessary, to alleviate cross-chip crossings.
- > Locate modules in layout to minimize large or "global" routes between modules.

CMOS CHIP DESIGN OPTIONS

- > Programmable Logic - μ P, DSP
- > Programmable Logic Structures - FPGA
- > Programmable Interconnect - FPGA
- > Mask Programmable Gate Arrays
- > Standard Cell Design
- > Mixed Standard Cell & Custom Design
- > Full Custom Mask Design

Design Investment
Increasing (for a
given application)



STANDARD-CELLS (POLYCELL) BASED DESIGN

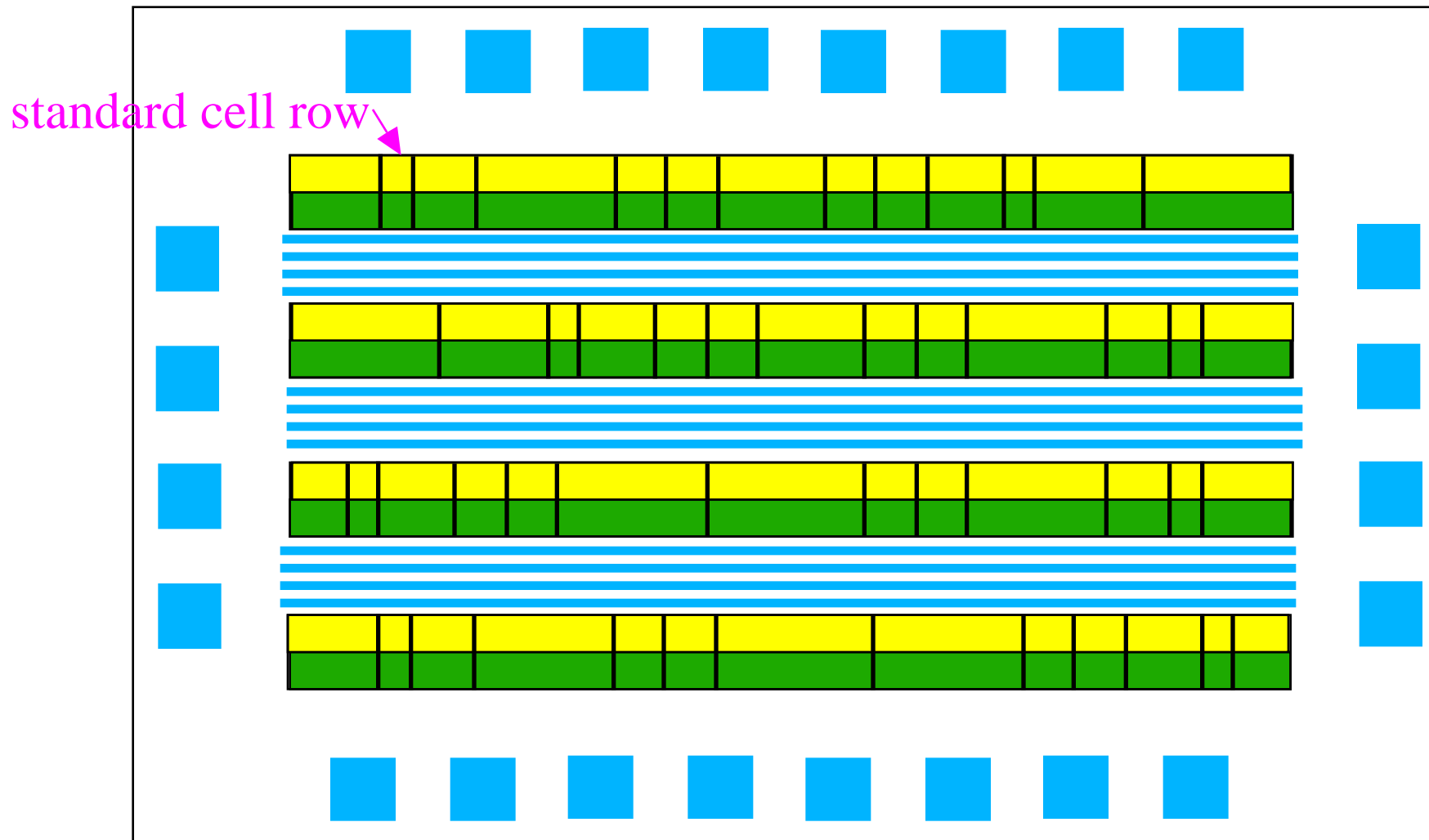
- > **Predominant full-custom design style.**
- > Standardization is achieved at the logic or function level.
- > Specific designs for each gate can developed and stored in a software database or cell library.
 - + Behavioral, Structural, and Physical Domain descriptions per cell
- > Layout is usually automatically placed and routed using CAD software.

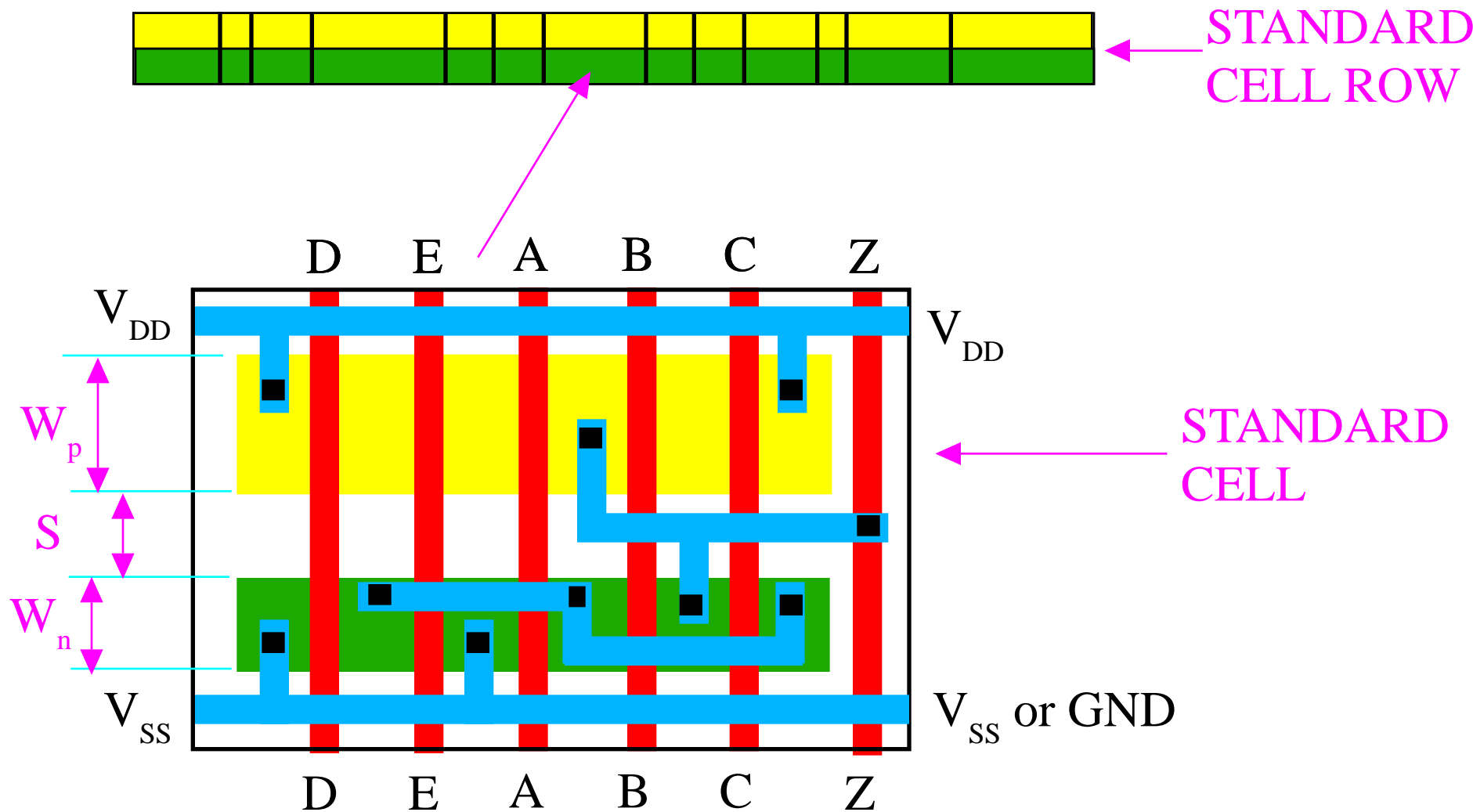
Typical Standard Cell Library contents:

- > **SSI logic:** e.g. nand, nor, xor, inverters, buffers, latches, registers
 - + Each gate can have multiple implementations to provide proper drive for different fan-outs, e.g. standard size, 2x, 4x
- > **MSI logic:** e.g. decoders, encoders, adders, comparators
- > **Datapath:** e.g. ALUs, adders, register files, shifters
- > **Memories:** e.g. RAM, ROM
- > **System level blocks:** e.g. multipliers, microcontrollers

SSI/LSI blocks: layout style is rows of constant high blocks separated by rows of routing.

SSI/LSI standard cell concept is extended to **higher level functions**, often available as parameterized modules.





DESIGN QUALITY

- > ACHIEVE SPECIFICATIONS (Static & Dynamic)
- > DIE SIZE
- > POWER DISSIPATION

- > TESTABILITY
- > YIELD AND MANUFACTURABILITY
- > RELIABILITY

-> TESTABILITY

- + generation of good test vectors
- + availability of reliable test fixture at speed
- + design of testable chip

-> YIELD AND MANUFACTURABILITY

- + functional yield
- + parametric yield

-> RELIABILITY

- + premature aging (Infant mortality)
- + ESD/EOS
- + latchup
- + on-chip noise and crosstalk
- + power and ground bouncing

PACKAGING TECHNOLOGY

-> INCLUDE IMPORTANT PACKAGE RELATED PARASITICS IN THE CHIP DESIGN AND SIMULATION <-

- > Package Power & Ground Planes -> on-chip power and ground busses
- > Bond Wire Lengths -> on-chip inductive effects
- > Thermal Resistance -> temp rise due to on-chip power dissipation
- > Package Cost

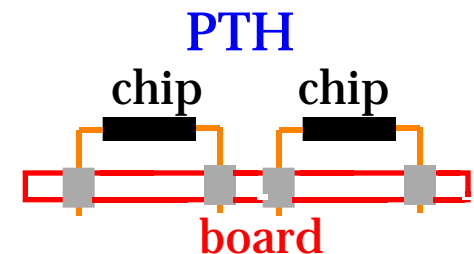
IMPORTANT PACKAGE DESIGN CONCERNS:

- > hermetic seals to prevent penetration of moisture
- > thermal conductivity
- > thermal expansion coefficient
- > pin density
- > parasitic inductance and capacitance
- > -particle protection (memories)

PACKAGE TYPES

DUAL IN-LINE PACKAGE (DIP)

1. ceramic or plastic pin-through-hole (PTH)
2. low cost, but large size
3. high lead inductance (22 - 36 nH)
4. max pin count usually 64

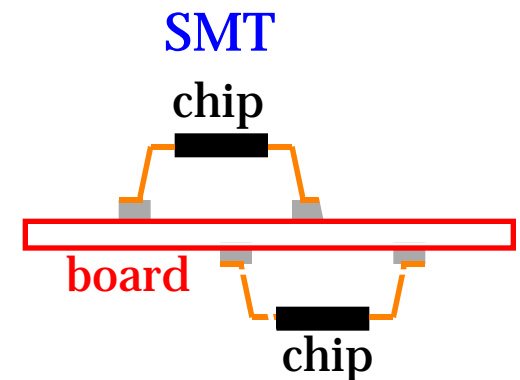


PIN GRID ARRAY (PGA) PACKAGE

1. ceramic or plastic pin-through-hole (PTH)
2. higher pin count (100 - 400 pins)
3. larger PCB area and higher cost than DIP

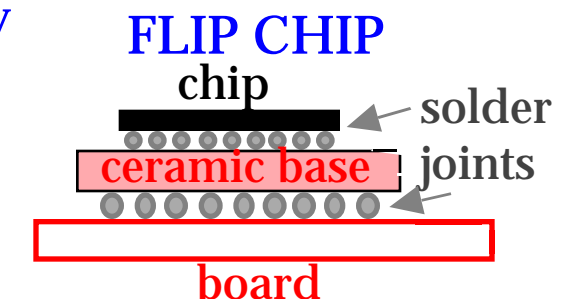
CHIP CARRIER PACKAGE (CCP)

1. surface-mounted technology (SMT)
2. leadless chip carrier supports high pin count
3. more efficient use of PCB area than DIP or PGA
4. Flip chip or ball grid array technology for higher density



MULTI-CHIP MODULE (MCM)

1. multiple chips assembled on a common substrate
2. high performance applications
3. most efficient use of PCB area



VLSI CAD TECHNOLOGY

CATEGORIES OF CAD TOOLS

1. High Level Synthesis (HDLs)
2. Logic Synthesis
3. Circuit Optimization
 - a. transistor sizing for min delays
 - b. process variations
 - c. statistical design
4. Layout
 - a. floorplanning
 - b. place & route
 - c. module generation
 - d. automatic cell placement and routing
5. Layout Extraction
6. Simulation (SPICE for circuit-level simulation)
7. Layout - Schematic Verification
8. Design Rule Check