

# Curriculum Vitae

## Nachiket G. Kapre

California Institute of Technology, Pasadena  
Computer Science  
Pasadena, CA 91125  
Date of Birth: September 2nd, 1980  
Citizenship: India

Office: (215) 573-4325  
Cell: (626) 319-2649  
Email: [nachiket@caltech.edu](mailto:nachiket@caltech.edu)  
Homepage: <http://www.cs.caltech.edu/~nachiket>  
Homepage: <http://www.seas.upenn.edu/~kapre>

### Research Fields

Concurrent and Spatial Architectures, Parallel Processing, FPGA-based Systems, Reconfigurable Computing

### Education

**Ph.D. Computer Science**, California Institute of Technology,

Expected: January 2010

Thesis: *A Highly-Parallel Architecture for Accelerating the Circuit Simulator SPICE*

*Committee:* André DeHon (UPenn), Steven Trimberger (Xilinx), Shuki Bruck (Caltech), Dan Meiron (Caltech)

**M.S. Computer Science**, California Institute of Technology

June 2006

Thesis: *Packet-Switched FPGA-Overlay Networks*

**M.S. Electrical Engineering**, California Institute of Technology

June 2005

**B.E. Electronics and Telecommunication Engineering**, University of Pune, India

August 2002

Thesis: *FPGA-based Testing System for Siemens Railway Signalling Relays*

Ranked 1st in a class of 773 students in the Sophomore, Junior, and Senior years

### Employment

**University of Pennsylvania** Visiting Graduate Student, Fall 2006–present

Working remotely towards a Caltech CS PhD

**Xilinx Inc.** Summer Intern, Summer 2005

Developed architectural modeling tools for memory controllers in streaming designs

**Koch Lab (Caltech)** Research Assistant, Spring 2004

Worked on analysis and engineering of a parallel, streaming saliency-detector using FPGAs

**Paxonet Communications Inc. (now Conexant)** Design Engineer, 2002–2003

Worked on design and verification of ASIC/FPGA IP cores for optical telecommunication protocols

**Siemens Inc.** Intern, 2002  
Worked on automated testing of mechanical relays

## Publications

- Nachiket Kapre, and André DeHon  
**“Parallelizing Sparse Matrix-Solve for SPICE Circuit Simulation using FPGAs”**  
*International Conference on Field Programmable Technology* December 2009
- Nachiket Kapre, and André DeHon  
**“Performance Comparison of Single-Precision SPICE Model-Evaluation on FPGA, GPU, Cell, and Multi-Core Processors”**  
*International Conference on Field Programmable Logic and Applications* September 2009
- Nachiket Kapre, and André DeHon  
**“Acceleration SPICE Model-Evaluation using FPGAs”**  
*IEEE Symposium on Field-Programmable Custom Computing Machines* April 2009
- Karl Papadantonakis, Nachiket Kapre, Stephanie Chan, and André DeHon  
**“Pipelined Saturated Accumulation”**  
*IEEE Transactions on Computers Volume 58 Issue 2 Page 208-219* February 2009
- Nachiket Kapre, and André DeHon  
**“Optimistic Parallelization of Floating-Point Accumulation”**  
*IEEE Symposium on Computer Arithmetic* June 2007
- Nachiket Kapre, Nikil Mehta, Michael deLorimier, Raphael Rubin, Henry Barnor, Michael Wilson, Michael Wrighton, and André DeHon  
**“Packet-Switched vs. Time-Multiplexed FPGA Overlay Networks”**  
*IEEE Symposium on Field-Programmable Custom Computing Machines* April 2006
- Michael deLorimier, Nachiket Kapre, Nikil Mehta, Dominic Rizzo, Ian Eslick, Raphael Rubin, Tomas Uribe, Thomas Knight Jr., and André DeHon  
**“GraphStep: A System Architecture for Sparse Graph Algorithms”**  
*IEEE Symposium on Field-Programmable Custom Computing Machines* April 2006
- Karl Papadantonakis, Nachiket Kapre, Stephanie Chan, and André DeHon  
**“Pipelined Saturated Accumulation”**  
*International Conference on Field-Programmable Technology* December 2005
- André DeHon, Joshua Adams, Michael deLorimier, Nachiket Kapre, Yuki Matsuda, Helia Naeimi, Michael Vanier, and Michael Wrighton  
**“Design Patterns for Reconfigurable Computing”**  
*IEEE Symposium on Field-Programmable Custom Computing Machines* April 2004

### Book Chapter

- Nachiket Kapre, and André DeHon  
**“Programming FPGA Applications in VHDL”**  
 From *Reconfigurable Computing: The Theory and Practice of FPGA-based Computation*  
 By Scott Hauck and André DeHon, Published by Morgan Kaufman/Elsevier, Copyright 2008,  
 ISBN-13: 978-0-12-370522-8, Pages 129-153

## Selected Talks

**“Accelerating the SPICE Circuit Simulator using FPGAs”**

Austin, USA *IBM, Inc.* August 2009.

**“Accelerating SPICE Model-Evaluation using FPGAs”**

San Jose, USA *Xilinx, Inc* February 2009.

**“Exploiting Application Structure in On-Chip Network Design”**

Gent, Belgium *University of Gent* and Munich, Germany *TU Munich* July-August 2007.

**“Optimistic Parallelization of Floating-Point Accumulation”**

Montpellier, France *IEEE Symposium on Computer Arithmetic* June 2007.

**“Packet-Switched vs. Time-Multiplexed FPGA Overlay Networks”**

Napa Valley, *IEEE Symposium on Field-Programmable Custom Computing Machines* April 2006.

## Patents

André DeHon and Nachiket Kapre

**“Method and a circuit using an associative calculator for calculating a sequence of non-associative operations”**

US 2007/0234128, Under review, Applied in January 2007

## Teaching

TA for ESE680s2: Computer Organization, Spring 2007 : University of Pennsylvania

TA for CS137: Electronic Design Automation, Winter 2006 : California Institute of Technology

## Professional Activities

Reviewer for ACM Transactions on Reconfigurable Technology and Systems

Student Member of the IEEE and ACM