Chapter 8: MEMS Packaging

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I. Introduction

MEMS is a relatively new field which is tied so closely with silicon processing that most of the early packaging technologies will most likely use "off-the-shelf" packaging "borrowed" from the semiconductor microelectronics field. Packaging of microelectronics circuits is the science and art of establishing interconnections and an appropriate operating environment for predominantly electrical (and in the case of MEMS, electromechanical) circuits to process and/or store information.

Packaging manifests itself in novel and unique creations that ingeniously reconcile and satisfy what seem to be mutually exclusive application requirements and constraints posed by the laws of nature and the properties of materials and processes. All applications can be summed up in three terms: cost, performance and reliability.

Packaging can span from the consumer to midrange systems to the high performance/reliability applications. It must be noted that no sharp boundaries exist between the classes, only a gradual shift from optimization for parameters which control performance and cause the cost to increase. All along, the reliability must also be considered. The packaging chapter that follows will summarize the primary package types that will likely apply to MEMS technology and the concerns that traditionally have concerned the microelectronics field.

Webster's dictionary defines **package** as a group or a number of things, boxed and offered as a unit. MEMS packages can contain many electrical and mechanical components. To be useful to the outside world these components need interconnections. Alone, a MEM die sawed from a wafer is extremely fragile and must be protected from mechanical damage and hostile environments. To function, electrical circuits need to be supplied with electrical energy, which is consumed and transformed into mechanical and thermal (heat) energy. Because the system operates best within a limited temperature range, packaging must offer an adequate means for removal of heat.

II. Functions of MEMS Packages

The package serves to integrate all of the components required for a system application in a manner that minimizes size, cost, mass and complexity. The package provides the interface between the components and the overall system. The following subsections present the three main functions of the MEMS package: mechanical support, protection from the environment, and electrical connection to other system components.

A. Mechanical Support

Due to the very nature of MEMS being mechanical, the requirement to support and protect the device from thermal and mechanical shock, vibration, high acceleration, particles, and other physical damage (possibly radiation) during storage and operation of the part becomes critical. The mechanical stress endured depends on the mission or application. For example, landing a spacecraft on a planet's surface creates greater mechanical shock than experienced by a communication satellite. There is also a difference between space and terrestrial applications.

The coefficient of thermal expansion (CTE) of the package should be equal to or slightly greater than the CTE of silicon for reliability, since thermal shock or thermal cycling may cause die cracking and delamination if the materials are unmatched or if the silicon is subject to tensile stress. Other important parameters are thermal resistance of the carrier, the material's electrical properties, and its chemical properties, or resistance to corrosion.

Once the MEMS device is supported on a (chip) carrier, the wire bonds or other electrical connections are made, the assembly must be protected from scratches, particulates, and other physical damage. This is accomplished either by adding walls and a cover to the base or by encapsulating the assembly in plastic or other material. Since the electrical connections to the package are usually made through the walls, the walls are typically made from glass or ceramic. The glass or ceramic can also be used to provide electrical insulation of the leads as they exit through a conducting package wall (metal or composite materials). Although the CTE of the package walls and lid do not have to match the CTE of silicon based MEMS as they are not in intimate contact (unless an encapsulating material is used), it should match the CTE of the carrier or base to which they are connected.

B. Protection From Environment

a) The Simple – Mechanical only

Many MEMS devices are designed to measure something in the immediate surrounding environment. These devices range from biological ‘sniffers’ to chemical MEMS that measure concentrations of certain types of liquids. So the traditional ‘hermeticity’ that is generally thought of for protecting microelectronic devices may not apply to all MEMS devices. These devices might be directly mounted to a printed circuit board (PCB) or a hybrid–like ceramic substrate and have nothing but a ‘housing’ to protect it from mechanical damage such as dropping or something as simple as damage from the operator’s thumb.

b) The Traditional – Hermetic and non-Hermetic

Many elements in the environment can cause corrosion or physical damage to the metal lines of the MEMS as well as other components in the package. Although there is no moisture in space, moisture remains a concern for MEMS in space applications since it may be introduced into the package during fabrication and before sealing. The susceptibility of the MEMS to moisture damage is dependent on the materials used in its manufacture. For example, Al lines can corrode quickly in the presence of moisture, whereas Au lines degrade slowly, if at all, in moisture. Also, junctions of dissimilar metals can corrode in the presence of moisture. Moisture is readily absorbed by some materials used in the MEMS fabrication, die attachment, or within the package; this absorption causes swelling, stress, and possibly delamination.

To minimize these failure mechanisms, MEMS packages for high reliability applications may need to be hermetic with the base, sidewalls, and lid constructed from materials that are good barriers to liquids and gases and do not trap gasses that are later released.

C. Electrical Connection to Other System Components

Because the package is the primary interface between the MEMS and the system, it must be capable of transferring DC power and in some designs, RF signals. In addition, the package may be required to distribute the DC and RF power to other components inside the package. The drive to reduce costs and system size by integrating more MEMS and other components into a single package increases the electrical distribution problems as the number of interconnects within the package increases.

When designs also require high frequency RF signals, the signals can be introduced into the package along metal lines passing through the package walls, or they may be electromagnetically coupled into the package through apertures in the package walls. Ideally, RF energy is coupled between the system and the MEMS without any loss in power, but in practice, this is not possible since perfect conductors and insulators are not available. In addition, power may be lost to radiation, by reflection from components that are not impedance matched, or from discontinuities in the transmission lines. The final connection between the MEMS and the DC and RF lines is usually made with wire bonds, although flip-chip die attachment and multilayer interconnects using thin dielectric may also be possible.

D. Thermal Considerations

For small signal circuits, the temperature of the device junction does not increase substantially during operation, and thermal dissipation from the MEMS is not a problem. However, with the push to increase the integration of MEMS with power from other circuits such as amplifiers perhaps even within a single package, the temperature rise in the device junctions can be substantial and cause the circuits to operate in an unsafe region. Therefore,

thermal dissipation requirements for power amplifiers, other large signal circuits, and highly integrated packages can place severe design constraints on the package design.

The junction temperature of an isolated device can be determined by

$$Tj = Q * R, + T_{case}$$

where

Q is the heat generated by the junction and is dependent on the output power of the device and its efficiency,

R is the thermal resistance between the junction and the case, and

T is the temperature of the case.

Normally, the package designer has no control over *Q* and the case temperature, and therefore, it is the thermal resistance of the package that must be minimized. Figure 8-1 is a schematic representation of the thermal circuit for a typical package, where it is assumed that the package base is in contact with a heat sink or case.

It is seen that there are three thermal resistances that must be minimized: the resistance through the package substrate, the resistance through the die-attach material, and the resistance through the carrier or package base. Furthermore, the thermal resistance of each is dependent on the thermal resistivity and the thickness of the material. A package base made of metal or metal composites has very low thermal resistance and therefore does not add substantially to the total resistance. When electrically insulating materials are used for bases metal-filled via holes are routinely used, under the MEMS, to provide a thermal path to the heat sink. Although thermal resistance is a consideration in the choice of the die attach material, adhesion and bond strength are even more important. To minimize the thermal resistance through the die-attach material, the material must be thin, there can be no voids, and the two surfaces to be bonded should be smooth.

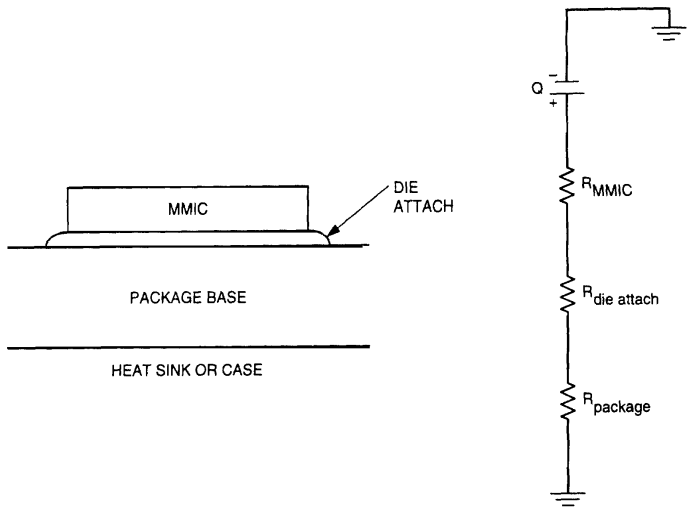

Figure 8-1: Cross section of MMIC attached to a package and its equivalent thermal circuit.

III. Types of MEMS Packages

Each MEMS application usually requires a new package design to optimize its performance or to meet the needs of the system. It is possible to loosely group packages into several categories. Four of these categories: 1) all metal packages, 2) ceramic, 3) plastic packages, and 4) thin-film multilayer packages are presented below.

A. Metal Packages

Metal packages are often used for microwave multichip modules and hybrid circuits because they provide excellent thermal dissipation and excellent electromagnetic shielding. They can have a large internal volume while still maintaining mechanical reliability. The package can use either an integrated base and sidewalls with a lid or it can have a separate base, sidewalls, and lid. Inside the package, ceramic substrates or chip carriers are required for use with the feedthroughs.

The selection of the proper metal can be critical. CuW (10/90), Silvar™ (a Ni-Fe alloy), CuMo (15/85), and CuW (15/85) all have good thermal conductivity and a higher CTE than silicon, which makes them good choices. Kovar™, a Fe-Ni-Co alloy commonly. All of the above materials, in addition to Alloy-46, may be used for the sidewalls and lid. Cu, Ag, or Au plating of the packages is commonly done.

Before final assembly, a bake is usually performed to drive out any trapped gas or moisture. This reduces the onset of corrosion-related failures. During assembly, the highest temperature curing epoxies or solders should be used first and subsequent processing temperatures should decrease until the final lid seal is done at the lowest temperature to avoid

later steps damaging earlier steps. Au-Sn is a commonly used solder that works well when the two materials to be bonded have similar CTEs. Au-Sn solder joints of materials with a large CTE mismatch are susceptible to fatigue failures after temperature cycling. The AuSn intermetallics that form tend to be brittle and can accommodate only low amounts of stress.

Welding (using lasers to locally heat the joint between the two parts without raising the temperature of the entire part) is a commonly used alternative to solders. Regardless of the seal technology, no voids or misalignments can be tolerated since they can compromise the package hermeticity. Hermeticity can also be affected by the feedthroughs that are required in metal packages. These feedthroughs are generally made of glass or ceramic and each method (glass seal or aluminum feedthrough) has its weakness. Glass can crack during handling and thermal cycling. The conductor exiting through the ceramic feedthrough may not seal properly due to metallurgical reasons. Generally, these failures are due to processing problems as the ceramic must be metallized so that the conductor (generally metal) may be soldered (or brazed) to it. The metallization process must allow for complete wetting of the conducting pin to the ceramic. Incomplete wetting can show up as a failure during thermal cycle testing.

B. Ceramic Packages

Ceramic packages have several features that make them especially useful for microelectronics as well as MEMS. They provide low mass, are easily mass produced, and can be low in cost. They can be made hermetic, and can more easily integrate signal distribution lines and feedthroughs. They can be machined to perform many different functions. By incorporating multiple layers of ceramics and interconnect lines, electrical performance of the package can be tailored to meet design requirements. These types of packages are generally referred to as co-fired multilayer ceramic packages. Details of the co-fired process are outlined below. Multilayer ceramic packages also allow reduced size and cost of the total system by integrating multiple MEMS and/or other components into a single, hermetic package. These multilayer packages offer significant size and mass reduction over metal-walled packages. Most of that advantage is derived by the use of three dimensions instead of two for interconnect lines.

Co-fired ceramic packages are constructed from individual pieces of ceramic in the "green" or unfired state. These materials are thin, pliable films. During a typical process, the films are stretched across a frame in a way similar to that used by an artist to stretch a canvas across a frame. On each layer, metal lines are deposited using thick-film processing (usually screen printing), and via holes for interlayer interconnects are drilled or punched. After all of the layers have been fabricated, the unfired pieces are stacked and aligned using registration holes and laminated together. Finally, the part is fired at a high temperature. The MEMS and possibly other components are then attached into place (usually organically (epoxy) or metallurgically (solders), and wire bonds are made the same as those used for metal packages.

Several problems can affect the reliability of this package type. First, the green-state ceramic shrinks during the firing step. The amount of shrinkage is dependent on the number and position of via holes and wells cut into each layer. Therefore, different layers may shrink more than others creating stress in the final package. Second, because ceramic-to-metal adhesion is not as strong as ceramic-to-ceramic adhesion, sufficient ceramic surface area must be available to assure a good bond between layers. This eliminates the possibility of continuous ground planes for power distribution and shielding. Instead, metal grids are used for these purposes. Third, the processing temperature and ceramic properties limit the choice of metal lines. To eliminate warping, the shrinkage rate of the metal and ceramic must be matched. Also, the metal must not react chemically with the ceramic during the firing process. The metals most frequently used are W and Mo. There is a class of Low Temperature Co-fired Ceramic (LTCC) packages. The conductors that are generally used are Ag, AgPd, Au, and AuPt. Ag migration has been reported to occur at high temperatures, high humidity, and along faults in the ceramic of LTCC.

C. Thin-Film Multilayer Packages

Within the broad subject of thin-film multilayer packages, two general technologies are used. One uses sheets of polyimide laminated together in a way similar to that used for the LTCC packages described above, except a final firing is not required. Each individual sheet is typically 25 μm and is processed separately using thin-film metal processing. The second technique also uses polyimide, but each layer is spun onto and baked on the carrier or substrate to form 1- to 20 μm-thick layers. In this method, via holes are either wet etched or reactive ion etched (RIE). The polyimide for both methods has a relative permittivity of 2.8 to 3.2. Since the permittivity is low and the layers are thin, the same characteristic impedance lines can be fabricated with less line-to-line coupling; therefore, closer spacing of lines is possible. In addition, the low permittivity results in low line capacitance and therefore faster circuits.

D. Plastic Packages

Plastic packages have been widely used by the electronics industry for many years and for almost every application because of their low manufacturing cost. High reliability applications are an exception because serious reliability questions have been raised. Plastic packages are not hermetic, and hermetic seals are generally required for high reliability applications. The packages are also susceptible to cracking in humid environments during temperature cycling of the surface mount assembly of the package to the mother-board. Plastic packaging for space applications may gain acceptability as time goes on. The reliability of plastic packages is presented in Section 8-V.

IV. Package-to-MEMS Attachment

The method used to attach a MEMS device to a package is a general technology applicable to most Integrated Circuit (IC) devices. Generally referred to as *die attach*, the function serves several critical functions. The main function is to provide good mechanical attachment of the MEMS structure to the package base. This ensures that the MEMS chip (or die) does not move relative to the package base. It must survive hot and cold temperatures, moisture, shock and vibration. The attachment may also be required to provide a good thermal path between the MEMS structure and the package base. Should heat be generated by the MEMS structure or by the support circuitry, the attachment material should be able to conduct the heat from the chip to the package base. The heat can be conducted away from the chip and 'spread' to the package base which is larger in size and has more thermal mass. This spreading can keep the device operating in the desired temperature range. If the support circuitry requires good electrical contact from the silicon to the package base, the attachment material should be able to accommodate the task.

The stability and reliability of the attach material is largely dictated by the ability of the material to withstand thermomechanical stresses created by the differences in the coefficient of thermal expansion (CTE) between the MEMS silicon and the package base material. These stresses are concentrated at the interface between the MEMS silicon backside and the attach material and the interface between the die attach material and the package base. Silicon has a CTE between 2 and 3 ppm/^{o}C while most package bases have higher CTE (6 to 20 ppm/^{o}C). An expression which relates the number of thermal cycles that a die attach can withstand before failure is based on the Coffin-Manson relationship for strain. The equation below defines the case for die attach,

$$N(f) \propto g^{m}\left(\frac{2*t}{L*\Delta CTE*\Delta T}\right)$$

where

γ	=	shear strain
m	=	material constant
L	=	diagonal length of the die
T	=	die-attach material thickness

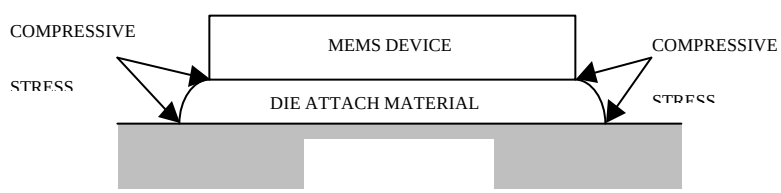

Figure 8-2: MEMS device in compression.

Voids in the die attach material cause areas of localized stress concentration that can lead to premature delamination. Presently, MEMS packages use solders, adhesives or epoxies for die attach. Each method has advantages and disadvantages that affect the overall MEMS reliability. Generally, when a solder is used, the silicon die would have a gold backing. Au-Sn (80-20) solder generally is used and forms an Au-Sn eutectic when the assembly is heated to approximately 250°C in the presence of a forming gas. When this method is applied, a single rigid assembled part with low thermal and electrical resistances between the MEMS device and the package. One problem with this attachment method is that the solder attach is rigid (and brittle) which means it is critical for the MEMS device and the package CTEs match since the solder cannot absorb the stresses.

Adhesives and epoxies are comprised of a bonding material filled with metal flakes as shown in the figure. Typically, Ag flakes are used as the metal filler since it has good electrical conductivity and has been shown not to migrate through the die attach material.[1,2] These die attach materials have the advantage of lower process temperatures. Generally between 100 and 200 ^{o}C are required to cure the material. They also have a lower built-in stress from the assembly process as compared to solder attachment. Furthermore, since the die attach does not create a rigid assembly, shear stresses caused by thermal cycling and mechanical forces are relieved to some extent.[3,4] One particular disadvantage of the soft die attach materials are that they have a significantly higher electrical resistivity which is 10 to 50 times greater than solder and a thermal resistivity which is 5 to 10 times greater than solder. Lastly, humidity has been shown to increase the aging process of the die-attach material.[2]

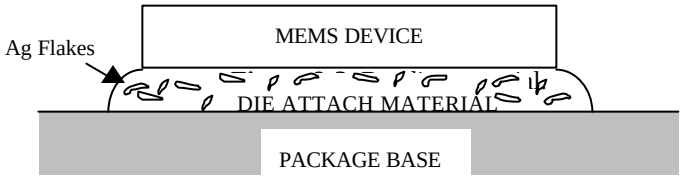

Figure 8-3: Schematic representation of silver filled epoxy resin.

V. Chip Scale Packaging

A. Flip Chip

Controlled Collapse Chip Connection (C4) is an interconnect technology developed by IBM during the 1960s as an alternative to manual wire bonding.

Often called "flip-chip," C4 attaches a chip with the circuitry facing the substrate. C4 uses solder bumps (C4 Bumps) deposited through a Bump Mask onto wettable chip pads that connect to matching wettable substrate pads (Figure 8-4). MEMS technology initially may not use flip chip packaging but the drive toward miniaturization may necessitate its incorporation into future designs.

"Flipped" chips align to corresponding substrate metal patterns. Electrical and mechanical interconnects are formed simultaneously by reflowing the C4 Bumps (Figure 8-5). The C4 joining process is self-aligning, i.e., the wetting action of the solder will align the chip's bump pattern to the corresponding substrate pads. This action compensates for slight chip-to-substrate misalignment (up to several mils) incurred during chip placement.

An added feature of C4 is the ability to rework. Several techniques exist that allow for removal and replacement of C4 chips without scrapping the chip or substrate. In fact, rework can be performed numerous times without degrading quality or reliability.

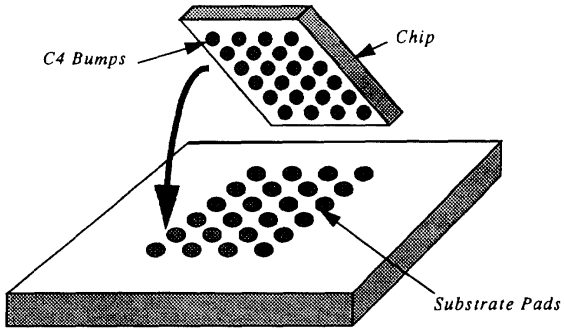

Figure 8-4: C4 (Controlled Collapse Chip Connection) flip chip.

For improved reliability, chip underfill may be injected between the joined chip and substrate as illustrated in Figure 8-5. It should be noted that any rework must be performed prior to application of chip underfill.

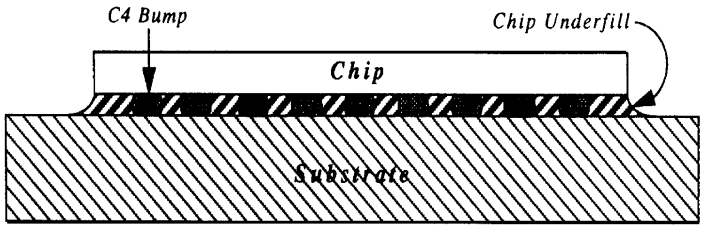

Figure 8-5: Mechanical and electrical connections.

It is important to recognize certain C4 characteristics when deciding on an interconnect technology. While application, size, performance, reliability and cost all must be factored in the selection process. However, these factors cannot be applied to the chip or product only. The overall impact <u>at the system level</u> must be considered for an equivalent comparison.

The primary advantage of C4 is its enabling characteristics. Specific advantages include:

- Size and weight reduction
- Applicability for existing chip designs
- Increased I/0 capability
- Performance enhancement
- Increased production capability
- Rework/chip replacement

Key considerations include:

- Additional wafer processing vs. wire bond
- Supplemental design groundrules
- Wafer probe complexity for array bump patterns
- Unique thermal considerations

Most importantly, C4 provides performance, size and I/O density improvements. With C4, nearly the entire chip surface can be utilized for interconnect pad locations. In fact, it has been demonstrated that one can have over 2500 C4 Bumps on a chip, and chips with over 1500 C4 Bumps are in production.

C4 enables increased interconnect density. Signal, clock and power connections can be placed almost anywhere on the chip and redundancy means distributions can be optimized for minimum noise and skew, current density and line length. Additionally, on-chip wiring can be reduced since z-axis escapes are available where needed.

Figure 8-6 compares single row wirebond and C4 chips. Each chip is 8 mm (200 mil) square. Wirebond pitch is 76 μm (3 mil) pads on 100 μm (4 mil) centers. C4 pitch is 100 μm (4 mil) bumps on 230 μm (9 mil) centers. In this example, interconnect density is increased over 140% using C4.

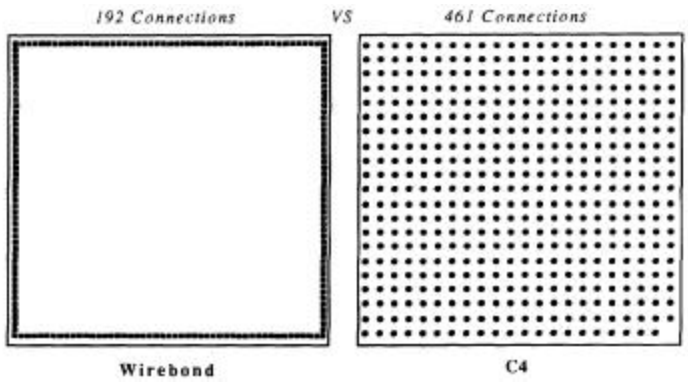

Figure 8-6: Interconnect density (wire bond vs. C4).

The reliability of flip-chip contacts is determined by the difference in the CTE between the chip and the ceramic substrate or the organic printed circuit board (PCB). For example, the CTE for silicon is ~2 – 3 ppm/^{o}K, for 96% alumina it is 6.4 ppm/^{o}K, and for PCB it is typically 20 to 25 ppm/^{o}K. The CTE mismatch between the chip and the carrier induces high thermal and mechanical stresses and strain at the contact bumps. The highest strain occurs at the corner joints, whose distance is the largest from the distance neutral point (DNP) on the chip. For example, the DNP for a 2.5- x 2.5-mm chip is 1.7 mm. The thermomechanical stress and strain cause the joints to crack. When these cracks become large, the contact resistance increases, and the flow of current is inhibited. This ultimately leads to chip electrical failure. The typical reliability defined failure criterion is an increase in resistance in excess of 30 mΩ over the zero time value.[5] The tradeoff in selecting the bump height is that large bumps introduce a series inductance that degrades high-frequency performance and increases the thermal resistance from the device to the carrier, if that is the primary heat path.

The reliability of the bump joints is improved if, after reflow, a bead of encapsulating epoxy resin is dispensed near the chip and drawn by capillary action into the space between the chip and the carrier. The epoxy is then cured to provide the final flip-chip assembly. Figure 8-5

shows a typical flip-chip package. The epoxy-resin underfill mechanically couples the chip and the carrier and locally constrains the CTE mismatch, thus improving the reliability of the joints. The most essential characteristic of the encapsulant is a good CTE match with the z-expansion of the solder or the bump material. For example, if one uses 95 Pb/5 Sn solder having a CTE of 28 ppm/^{o}K, an encapsulant with a CTE of about 25 ppm/^{o}K is recommended. Underfilling also allows packaging of larger chips by increasing the allowable DNP. In some cases, the encapsulant acts as a protective layer on the active surface of the chip

Good adhesion among the underfill material, the carrier, and the chip surface is needed for stress compensation. The adhesion between the surfaces can be lost and delamination can take place if contaminants, such as post-reflow flux residue, are present. For this reason, a fluxless process for flip-chip assembly is desirable.[5] Unfortunately, flip-chip bonding on PCB requires the use of flux.[6] However, on ceramic carriers with gold, silver, and palladium-silver thick-film patterns and via metallizations, fluxless flipchip thermocompression bonding with gold-tin bumps has demonstrated high reliability.[5] The results of reliability testing[5] are summarized in Table 8-1 and may serve as a guideline for future work.

Parameter	Value
Bump height	30 to 70 μm
Chip size	A few mm
Chip carrier	Ceramic
Carrier camber	5 μm per cm
Camber compensation	By bump deformation
Underfill	Yes
Thermal cycling	After 6500 cycles (-55°C to +125°C), no contact failure and no change in contact resistance
High-temperature storage	After 1000 h, no increase in contact resistance
Temperature and humidity	After 1000 h (85'C and 85% RH), no change in contact resistance
Pressure-cooker test	After 1000 h (121°C and 29.7 psi), contact resistance increased slightly from 3 mW to 4 mW

Table 8-1: Summary of reliability test conditions and results for fluxless flip-chip thermocompression-bonded bump contacts.

Finally, care should be taken that the encapsulant or underfill covers the entire underside without air pockets or voids, and forms complete edge fillets around all four sides of the chip. Voids create high-stress concentrations and may lead to early delamination of the encapsulant. After assembly, a scanning acoustic microscope can be used to locate voids in the encapsulant. The encapsulant should also be checked for microcracks or surface flaws, which have a

tendency to propagate with thermal cycling and environmental attacks, eventually leading to chip failure.[7]

B. Ball-Grid-Array (BGA)

Ball Grid Array is a surface mount chip package that uses a grid of solder balls as its connectors. It is noted for its compact size, high lead count and low inductance, which allows lower voltages to be used. BGAs come in plastic and ceramic varieties. It essentially has evolved from the C4 technology whereas more I/Os can be utilized in the same area as in a peripherally leaded package (or chip). The CBGA and PBGA are not truly Chip Scale Packaging but the evolution to the µBGA has come out of the experience the industry has gained from the CBGA and PBGA packages.

i) Ceramic Ball-Grid-Array (CBGA)

Originally designed by IBM, the CBGA was developed to complement their C4 (flip-chip) technology. The package is comprised of a ceramic (alumina) substrate and a C4 chip and an aluminum lid as depicted in Figure 8-7. The ball-grid spacing is on 50 mil centers with solder balls composed of high melt solder (90/10 Pb/Sn) attached by eutectic solder (63/37 Sn/Pb). Recent designs have concentrated on miniaturization and have reduced the package size and utilized 40 mil on center solder balls.

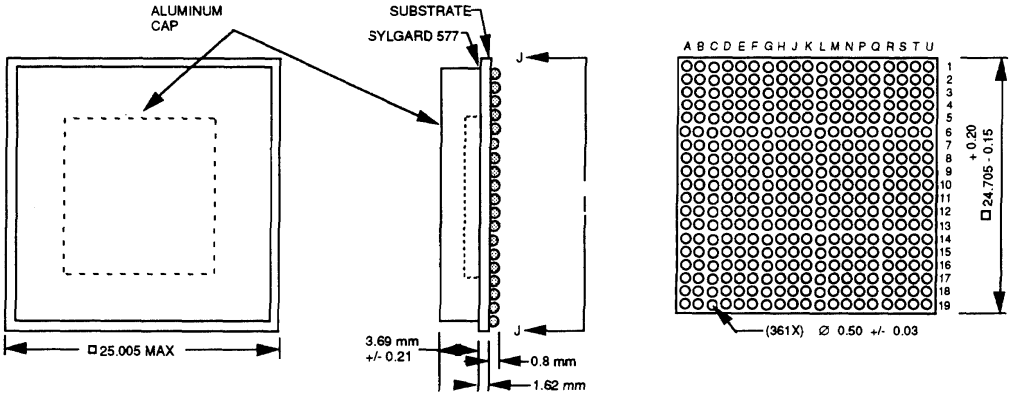

Figure 8-7: Ceramic Ball-Grid-Array Package shown with connections on 50 mil centers with a) top view, b) side view and c) bottom view illustrating the high number of connections.

Aluminum covers that have typically been used with the C4 technology have been bonded with a silicone adhesive (Sylgard 577) to provide a non-hermetic seal. With the flip-chip technology this is usually adequate for most applications. A hermetic seal can be accomplished by designing a seal ring into the ceramic and using a Ni/Fe cover plate for soldering.

The package as described above has a cavity which would allow for typical chip-and-wire technology to be utilized. A MEMS device could be utilized in the wire bond package configuration first and migrate to use as a flip-chip in later designs.

ii) Plastic Ball-Grid-Array (PBGA)

The Plastic Ball-Grid-Array (PBGA) is very similar to the plastic packaging technology described in Section 8-V. It is based on the same chip-and-wire technology and has moisture sensitivity (i.e., susceptible to 'popcorn' cracking during solder reflow) issues just like plastic packaging. It is different in that it is built on a printed circuit board substrate rather than a leadframe (metal) material (Figure 8-8). The attach method (to the motherboard) is accomplished by soldering solder balls or bumps rather than leads.

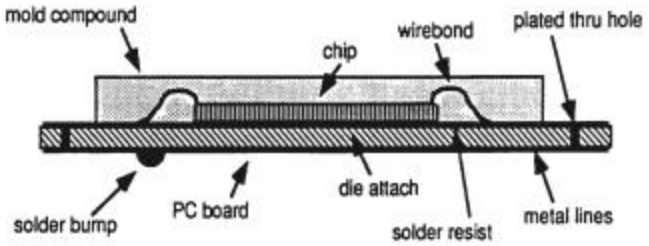

Figure 8-8: A schematic representaion of a Plastic Ball-Grid-Array Package.

One advantage this technology has over conventional plastic packaging is that the PC board material (which can vary from FR4 to polyimide to BT resin to name a few materials) can be a simple 2 layer board or be made of multiple layers. Additional layers allow for power and ground planes.

iii) Micro-Ball-Grid-Array (μBGA)

μBGA is a true "Chip Scale Package" (CSP) solution, only slightly larger than the die itself (die + 0.5mm). It is the ideal package for all memory devices such as Flash, DRAM and SRAM. uBGA packages enable broad real-estate reductions of typically 50-80 percent over existing packages. End use applications include cell phones, sub-notebooks, PDAs, camcorders, disk drives, and other space-sensitive applications. This package is also an

excellent solution for applications that require a smaller, thinner, lighter or electrically enhanced package. It therefore lends itself nicely to space flight applications.

The uBGA package is constructed utilizing a thin, flexible circuit tape for its substrate and low stress elastomer for die attachment. The die is mounted face down and its electrical pads are connected to the substrate in a method similar to TAB bonding. After bonding these leads to the die, the leads are encapsulated with an epoxy material for protection. Solder balls are attached to pads on the bottom of the substrate, in a rectangular matrix similar to other BGA packages. The backside of the die is exposed allowing heat sinking if required for thermal applications. Ball pitches available today are 0.50, 0.75, 0.80, and 1.0 mm. Other features and benefits include: 0.9 mm mounted height, excellent electrical and moisture performance, 63/37 Sn/Pb solder balls, and full in-house design services.

VI. Multichip Packaging

A. MCM/HDI

Multichip packaging of MEMS can be a viable means of integrating MEMS with other microelectronic technologies such as CMOS. One of the primary advantages of using multichip packaging as a vehicle for MEMS and microelectronics is the ability to efficiently host die from different or incompatible fabrication processes into a common substrate. High performance multichip module (MCM) technology has progressed rapidly in the past decade, which makes it attractive for use with MEMS.

The Chip-on-Flex (COF) process has been adapted for the packaging of MEMS.[8] One of the primary areas of the work was reducing the potential for heat damage to the MEMS devices during laser ablation. Additional processing has also been added to minimize the impact of incidental residue on the die.[9]

i) COF/HDI Technology

COF is an extension of the HDI technology developed in the late 1980's. The standard HDI "chips first" process consists of embedding bare die in cavities milled into a ceramic substrate and then fabricating a layered thin-film interconnect structure on top of the components. Each layer in the HDI interconnect overlay is constructed by bonding a dielectric film on the substrate and forming via holes through laser ablation. The metallization is created through sputtering and photolithography.[10]

COF processing retains the interconnect overlay used in HDI, but molded plastic is used in place of the ceramic substrate. Figure 8-9 shows the COF process flow. Unlike HDI, the interconnect overlay is prefabricated before chip attachment. After the chip(s) have been bonded to the overlay, a substrate is formed around the components using a plastic mold

forming process such as transfer, compression, or injection molding. Vias are then laser drilled to the component bond pads and the metallization is sputtered and patterned to form the low impedance interconnects.[11]

For MEMS packaging, the COF process is augmented by adding a processing step for laser ablating large windows in the interconnect overlay to allow physical access to the MEMS devices. Figure 8-10 depicts the additional laser ablation step for MEMS packaging. Additional plasma etching is also included after the via and large area laser ablations to minimize adhesive and polyimide residue which accumulates in the exposed windows.

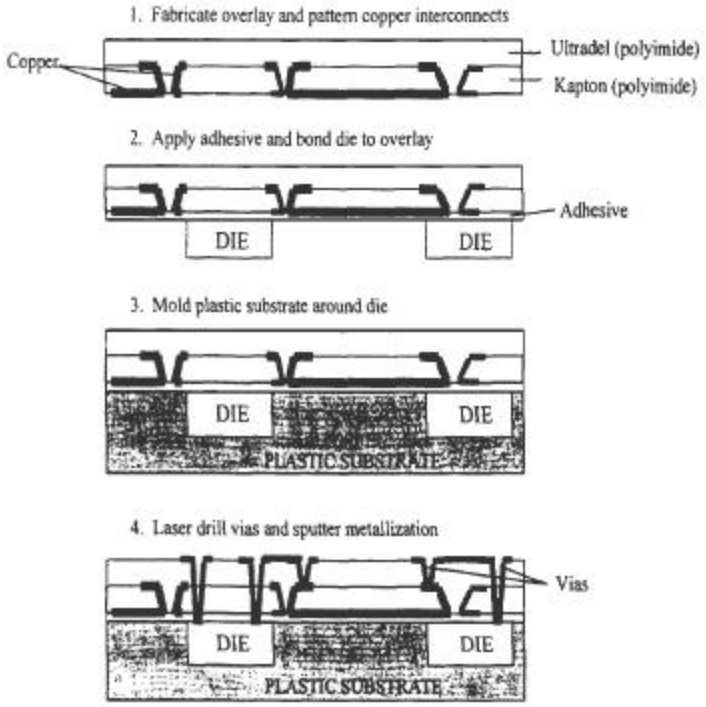

Figure 8-9: Chip-on-Flex (COF) process flow.[1]

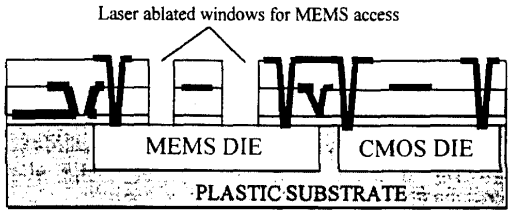

Figure 8-10: Large area ablation for MEMS access in COF package.

ii) MEMS Test Chip

MEMS test die can be used in research to assess the impact of various packaging technologies on MEMS. Test die typically contain devices and structures designed to facilitate a structured method of monitoring the health of MEMS devices after packaging.

Surface micromachined test die have been available through the Multi-User MEMS Processes (MUMPs). The MUMPs process has three structural layers of polysilicon which are separated by sacrificial layers of silicon oxide. The substrate is electrically isolated from the polysilicon layers by a silicon nitride barrier. The top layer of the process is gold and is provided to facilitate low-impedance wiring of the MEMS devices but can also be used as a reflective surface for optical devices. Table 8-2 lists nominal thicknesses of the various layers, and Figure 8-11 shows a cross-sectional view of a notional MUMPs layout.

Layer	Thickness (mm)
Gold	0.5
Poly 2	1.5
2nd Oxide	0.75
Poly 1	2.0
1st Oxide	2.0
Poly 0	0.5
Nitride	0.6

Table 8-2: MUMPs layer thickness.[10]

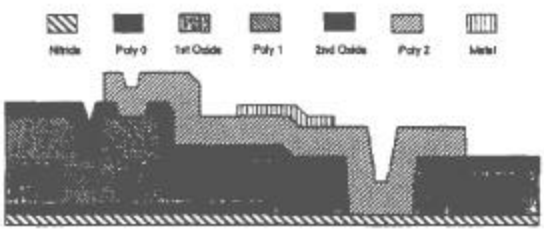

Figure 8-11: Cross-section of MUMPs layout.[10]

Among the test structures on the test die are breakage detectors to monitor excess force and polysilicon resistors to monitor excess heating. Other devices on the die are representative of MEMS structures which might be used in an actual application. Table 8-3 lists general categories of devices on the surface micromachining test die.

Device Category
Breakage Detectors
Polysilicon Resistors
Variable Capacitors
Flip-up and Rotating Devices
Thermal Actuators
Electrostatic Piston Mirrors
Electrostatic Comb Drives

Table 8-3: MEMS device categories included on surface micromachining test die.

The bulk micromachining test die was fabricated through MOSIS using the Orbit CMOS MEMS process. The CMOS MEMS process is based on the standard 2 μm CMOS technology. The CMOS process has two metal and two polysilicon layers. Additional processing is added to allow MEMS fabrication. Provisions are made to specify cuts in the overglass to expose the silicon substrate for bulk micromachining. In addition, regions of boron doping can be specified to form etch steps for anisotropic silicon etchants such as ethylene diamine Pyrocatechol (EDP) and potassium hydroxide (KOH). These tools allow for bulk micromachining to be accomplished in the standard CMOS process.[12] Table 8-4 lists some of the device categories represented on our bulk micromachining test die. A sampling of integrated circuits such as ring oscillators for testing package interconnects was also included on the test die.

Device Category
Breakage Detectors
Polysilicon Resistors

Cantilevers
Suspended Structures
Thermal Bimorphs

Table 8-4: MEMS device categories included on bulk micromachining test die.

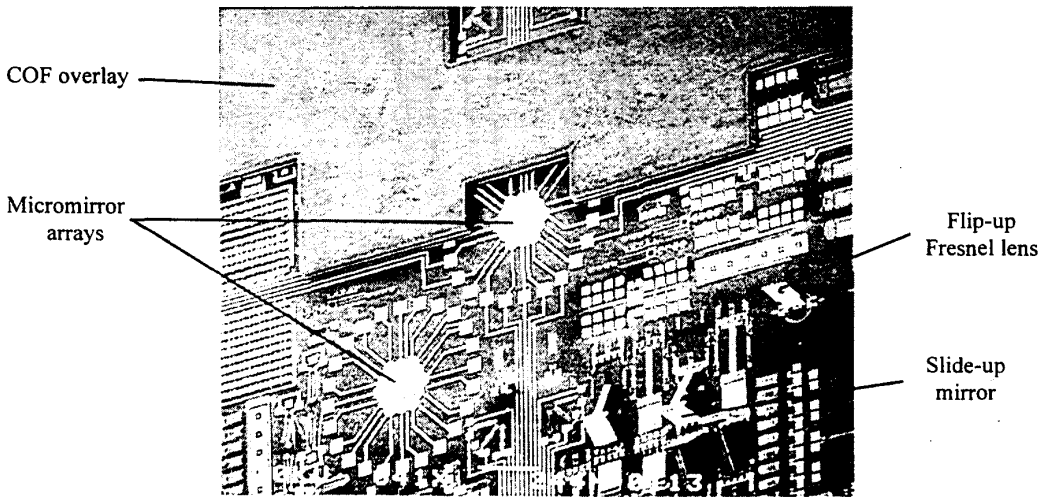

Figure 8-12: Windows laser ablated in COF overly for MEMS access.[9]

B. System on a Chip (SOAC)

System on a chip may not necessarily be classified as a packaging technology. It is derived from the wafer fabrication process where numerous individual functions are processed on a single piece of silicon. These processes, generally CMOS technology, are compatible with the MEMS processing technology. Most SOAC chips are designed with a microprocessor of some type, some memory, some signal processing and others. It is very conceivable that a MEMS device could one day be incorporated on a SOAC. Initially, it may be incorporated by some other packaging technology such as flip chip or µBGA.

VII. Plastic Packaging (PEMs)

Most MEMS designs either have moving parts or do not allow for intimate contact of an encapsulating material such as in a traditional plastic package. Furthermore, plastic packages have not gained wide acceptance in the field of space applications. However, there are many semiconductor designs that are beginning to be flown in space applications. Programs such as Commercial of the Shelf (COTS) which include Plastic Encapsulated Microelectronics (PEMs) are gaining wide acceptance. It is therefore important to outline the basic issues in PEMs for MEMS applications.

Studies have shown that during the high-temperature soldering process encountered while mounting packaged semiconductor devices on circuit boards, moisture present in a plastic package can vaporize and exert stress on the package. This stress causes the package to crack and also causes delamination between the mold compound and the lead frame or die. This phenomenon is often referred to as 'popcorn' cracking. These effects are most pronounced if the package has greater than 0.23% absorbed moisture before solder reflow.[13] Figure 8-13 shows a typical example of a package crack. The mismatch in thermal expansion coefficients of the package's components also induces stresses. If these combined stresses are greater than the fracture strength of the plastic, cracks will develop. The cracks can provide a path for ionic contaminants to reach the die surface, and/or die delamination can cause wire-bond failure. Hence, these are reliability concerns.

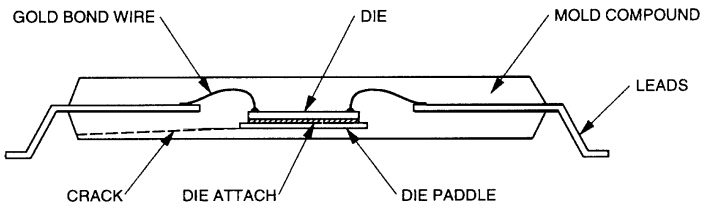

Figure 8-13: Typical plastic package showing the onset of a crack.

JEDEC defines five classes for moisture resistance of plastic packages and sensitivity to 'popcorning'. Class 1 is defined as unlimited exposure to moisture and the package will still not exhibit delamination during the surface mount operation. Class 5 can tolerate minimal exposure to moisture before it needs to be dried (by baking in an oven set at ~125°C for a duration of 8 to 24 hours depending on the package). Classes 2 through 4 are defined as somewhere in between the extremes. Most commercial packages are classified as class 3 moisture resistant.

To overcome the delamination problem, results derived from numerical simulation and experimental data can serve as a guide in the selection of suitable molding compound properties.[14] The properties considered are the adhesion strength, S, and the coefficient of thermal expansion, α. These results are summarized in Figure 8-14.

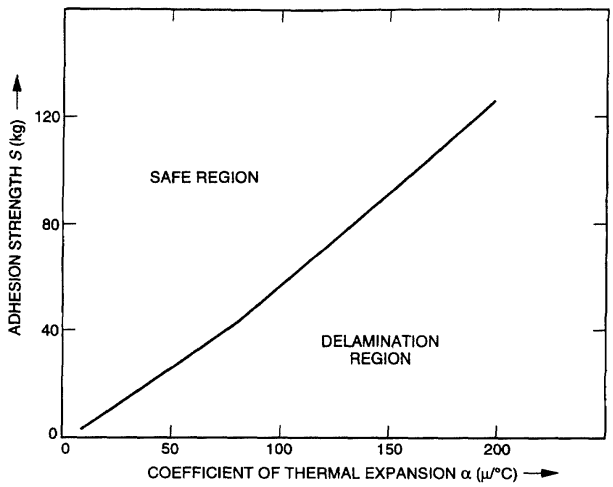

Figure 8-14: Mold compound properties.

The amount of moisture a particular package design can take up prior to delamination and catastrophic popcorning can be empirically determined as shown in Figure 8-15. As can be seen, a high moisture environment (as well as high temperature) greatly reduces the amount of time on a production floor prior to the surface mount operation.

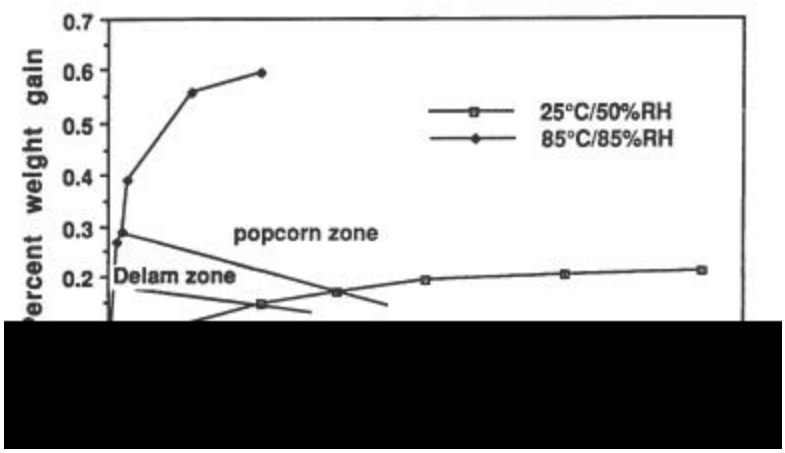

Figure 8-15: Moisture weight gain of a plastic package exposed to two different moisture conditions.

Also, it has been shown that polyimide die overcoat, or PIX, can reduce the percent of die or pad delamination by up to 30% on parts subjected to temperature cycling.[13,15] This PIX coating can mechanically support air bridges during plastic encapsulation, provide a more uniform electrical environment for the die, and provide protection to the surface of the die. Figure 8-16 shows cross sections of three PIX-treated dies. It has been reported that the PIX shown in Figure 8-16(a) yields the best improvement in reliability.[13] The PlXs shown in 8-16(b) and (c) are not as desirable, because, respectively, they cause wirebond stress and do not protect the die surface.

VIII. Additional Reading

H. L. Hvims, "Conductive Adhesives for SMT and Potential Applications," IEEE *Trans. on Components, Packaging, and Manuf. Tech. - Part-B,* Vol. 18, No. 2, pp. 284-291, May 1995.

0. Rusanen and J. Lenkkeri, "Reliability Issues of Replacing Solder With Conductive Adhesives in Power Modules," *IEEE Trans. on Components, Packaging, and Manuf. Tech. - Part-B,* Vol. 18, No. 2, pp. 320-325, May 1995.

T. Tuhus and A. Bjomeklett, "Thermal Cycling Reliability of Die Bonding Adhesives," *1993 IEEE Annual Inter. Reliability Physics Symp. Digest,* pp. 208, March 23-25, 1993.

P. Yalamanchili and A. Christou, "Finite Element Analysis of Millimeter Wave MMIC Packages Subjected to Temperature Cycling and Constant Acceleration," *1993 GaAs REL Workshop Programs and Abstracts,* October 10, 1993.

J. Kloeser, E. Zake. F. Bechtold, and H. Reichl, "Reliability Investigations of Fluxless Flip-Chip Interconnections on Green Tape Ceramic Substrates," IEEE *Trans. Components, Packaging, and Manufacturing Technology, Part* A, Vol. 19, No. 1, pp. 24-33, March 1996.

J. Giesler, G. O'Malley, M. Williams, and S. Machuga, "Flip Chip on Board Connection Technology: Process Characterization and Reliability," *IEEE Trans. Components, Packaging, and Manufacturing Technology, Part 8,* Vol. 17, No. 3, pp. 256-263, August 1994.

D. Suryanarayana, T. Y. Wu, and J. A. Varcoe, "Encapsulant used in Flip-Chip Packages," *IEEE Trans. Components, Packaging, and Manufacturing Technology,* Vol. 16, No. 8, pp. 858-862, December 1993.

J. Butler, V. Bright, and J. Comtois, "Advanced multichip module packaging of microelectromechanical systems," *Tech Digest of the 9th International Conference on Solid-State Sensors and Actuators (Transducers '97*), Vol. 1, pp. 261-264, June 1997.

J. Butler, V. Bright, R. Saia and J. Comtois, "Extension of High Density Interconnect Multichip Module Technology for MEMS Packaging", SPIE Vol. 3224, pp. 169 - 177.

W. Daum, W. Burdick Jr., and R. Fillion, "Overlay high-density interconnect: A chips-first multichip module technology," *IEEE Computer,* Vol. 26, No. 4, pp. 23-29, April 1993.

R. Filtion, R. Wojnarowski, R. Saia, and D. Kuk, "Demonstration of a chip scale chip-on-flex technology," *Proceedings of the 1996 International Conference on Multichip Modules,* SPIE vol. 2794, pp. 351-356, April 1996.

J. Marshall, M. Parameswaran, M. Zaghloul, and M. Gaitan, "High-level CAD melds micromachined devices with foundries," *Circuits and Devices,* Vol. 9, no. 6, pp. 10- 17, November 1992.

T. M. Moore and S. J. Kelsall, "The Impact of Delamination on Stress-Induced and Contamination-Related Failure in Surface Mount ICs," *1992 IEEE Annual Int. Reliability Physics Symp. Proc.,* pp. 169-176, March 31-April 2, 1992.

A. A. 0. Tay, G. L. Tam, and T. B. Lim, "Predicting Delamination in Plastic IC Packages and Determining Suitable Mold Compound Properties," *IEEE Trans. Components, Packaging, and Manufacturing Technology-Part 8,* Vol. 17, No. 2, pp. 201-208, May 1994.

W. J. Roesch and A. L. Rubalcava, "GaAs IC Reliability in Plastic Packages," *1995 GaAs Reliability Workshop Programs and Abstracts,* pp. 25-30, October 29, 1995.

A. A. 0. Tay, K. S. Yeo, and J. H. Wu, "The Effect of Wirebond Geometry and Die Setting on Wire Sweep," *IEEE Trans. Components, Packaging, and Manufacturing Technology-Part B,* Vol. 18, No. 1, pp. 201-209, February 1995.