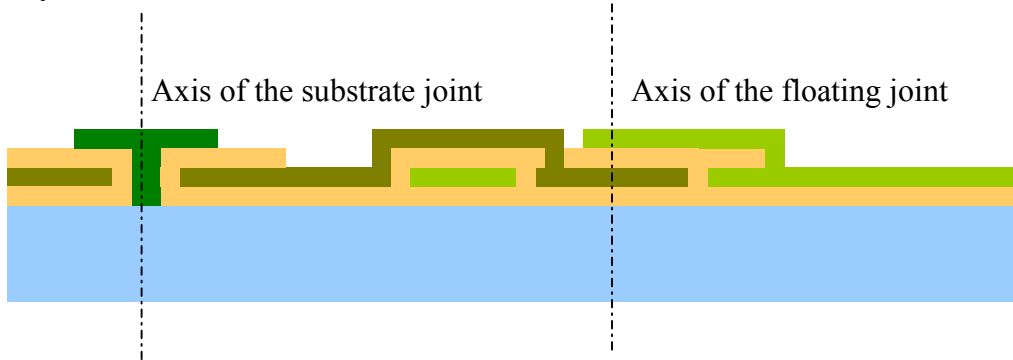


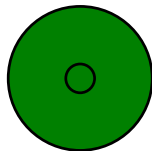
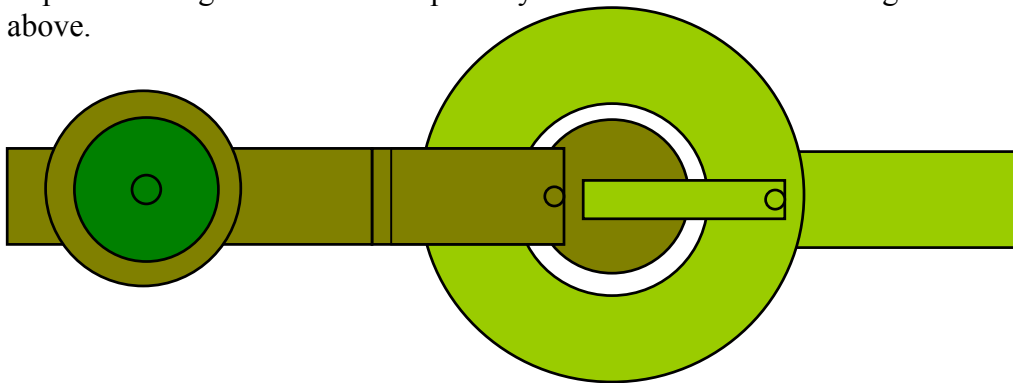
### Solution to homework #2

#### Problem 1

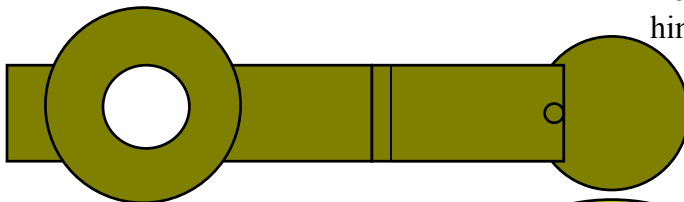
In-plane substrate and floating joints using only two structural layers and two sacrificial layers.



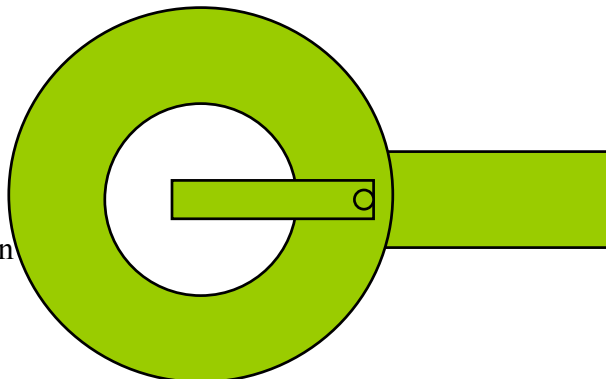
Top views – together and then separately below with colors matching with the side view above.



Hub of the substrate hinge

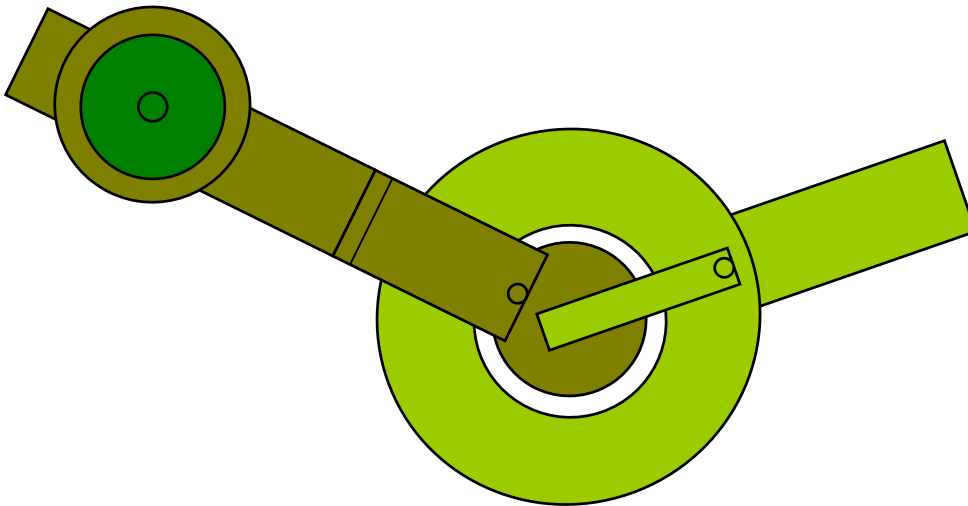


Body with substrate and floating hinges at the either end



Body with the floating hinge on one end

After rotating the substrate and floating hinges...

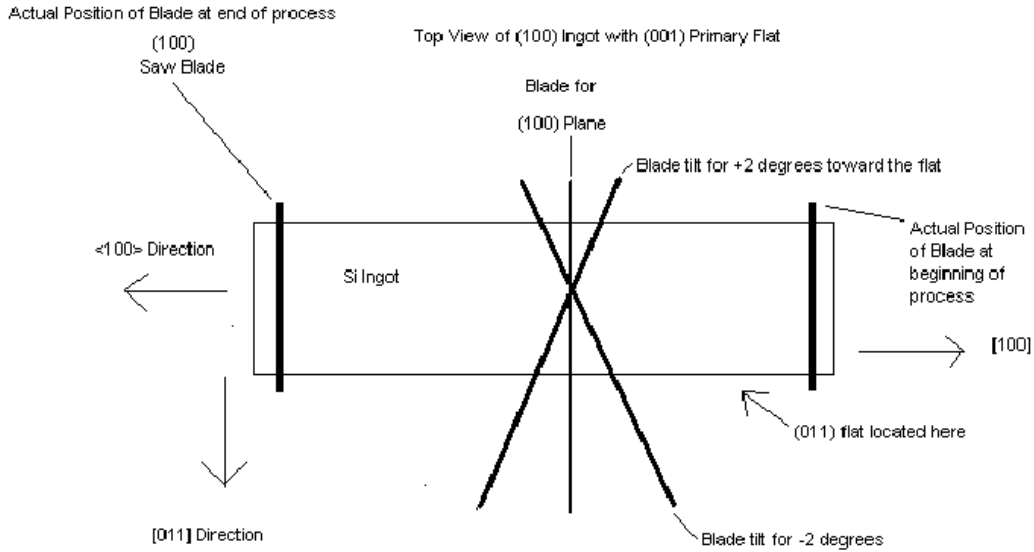


### Problem 2

First, we need to clarify the way the flat on (100) wafers is oriented. It is usually said that it is along the [110] direction. But a closer examination tells us that it is actually [011] direction. Since the choice of the coordinate system is arbitrary, [110] and [011] directions might mean the same direction for different peoples with different choices of coordinate frames. This causes some confusion. But to understand the KOH etching of (100) silicon as per the known results, the wafer flat is along [011] direction and the rectangle should be aligned with this direction.

For further clarity, consider how a (100) silicon ingot is cut to create the wafer flat before it is sliced to thin wafers (see Figure 2.1). Now, compare with the silicon crystal polyhedron. It is the [011] direction that actually lies parallel to the (100) plane and not the [110] direction. Thus, the rectangle of  $200\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$  is to be drawn at  $45^\circ$  to the square representing the (100) plane in the silicon crystal polyhedron with  $200\text{ }\mu\text{m}$  side oriented along the [011] direction.

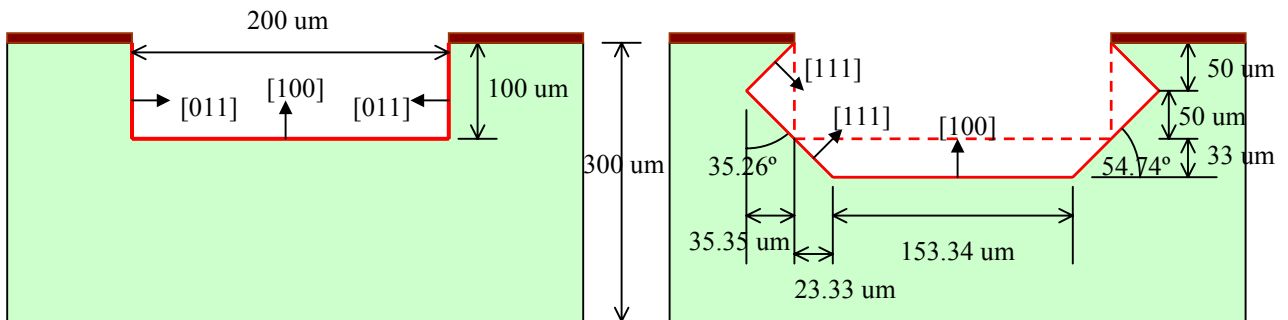
Now, with this orientation, when we vertically go down with the DRIE etch, (011) planes get exposed rather than (010) planes. The etch rate along (011) planes is the same as that on the (110) planes because the choice of the coordinate system is arbitrary. The etch stops on (111) planes in both (100) and (011) oriented surfaces. So, the etch proceeds as shown in Figure 2.2. The conformation is shown in the experimental evidence shown in Figure 2.3 where the KOH etch seems to be for much less time.



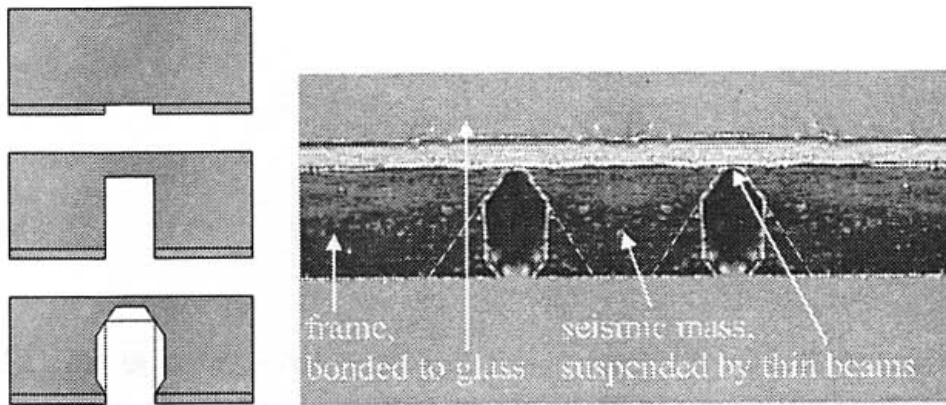
**Figure 2.1** Slicing of (100) silicon wafers and the orientation of the primary flat in the [011] direction (from Virginia Semiconductor's website)

After DRIE...

After KOH etching with the same mask...



**Figure 2.2** Cross-section profiles after DRIE and then KOH etch



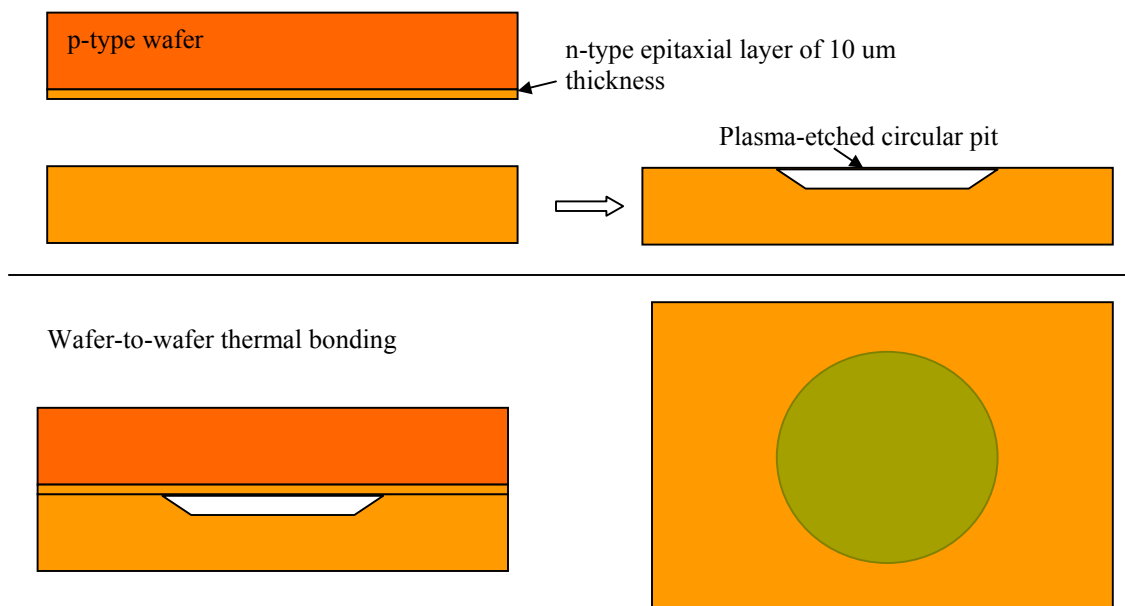
**Figure 2.3** The experimentally observed cross-sections if the KOH is for a very short time (from Steve Reyntjens PhD thesis, K. U. Leuven)

### Problem 3

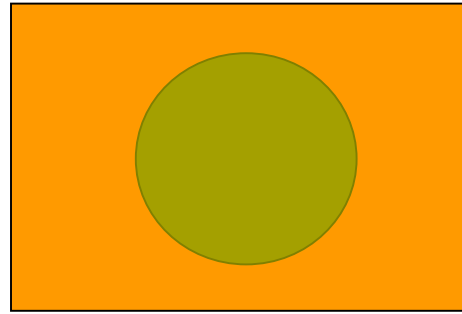
#### Sources:

- 1) "A Merged MEMS-CMOS Process Using Silicon Wafer Bonding", L. Parameshwaran, C. Hsu, and M. A. Schmidt, IEDM 95, pp. 613-616.
- 2) "Silicon Pressure Sensor Using A Wafer-Bonded Sealed-Cavity Process," L. Parameshwaran, A. Mirza, W. K. Chan, and M. A. Schmidt, Transducers 95, pp. 582-585.

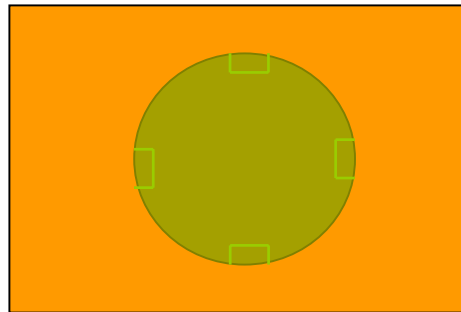
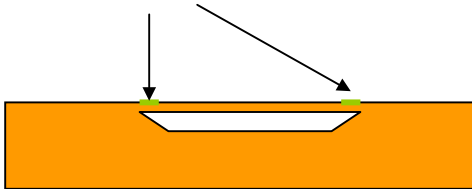
The process begins with two (100) oriented silicon wafers, one of p-type and another of n-type. A 10  $\mu\text{m}$  thick n-type layer is grown epitaxially on the p-type silicon wafer. A shallow circular pit is etched into the n-type silicon wafer using plasma etching. The two wafers are then cleaned and are brought into contact (the shallow pit on the n-type wafer is in contact with the n-type epi layer of the p-type wafer) and annealed at 1100  $^{\circ}\text{C}$  for one hour. This enables the bonding of the two wafers. Next, the p-type wafer is thinned down by grinding and polishing, and then electrochemically etched so that the etch stops on the n-type epi layer. This leaves a circular membrane of uniform thickness of 10  $\mu\text{m}$ . At four locations along the periphery, U-shaped piezoresistors are formed by a masked doping (e.g., using ion implantation). A subsequent metallization step creates the electrical connections (e.g., using lift-off patterning). A hole is opened at the back using KOH for connecting to the pressure source and the device is packaged.



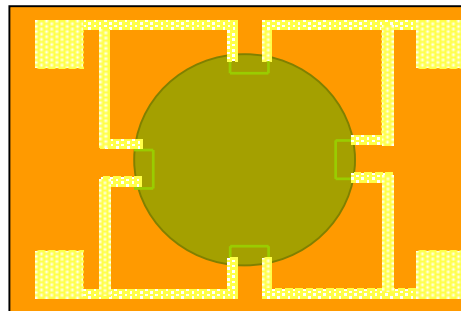
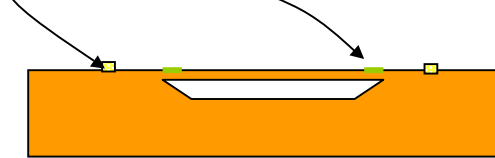
Grinding and polishing followed by electrochemical etching that stops on n-type layer



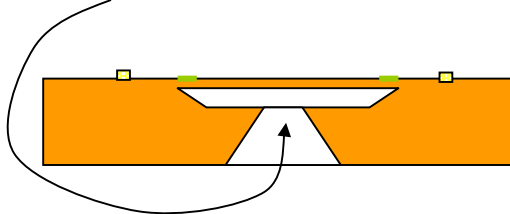
Implant piezoresistors using a mask



Metallization to define the electrical connections



KOH etching at the bottom to create an opening



Possible packaging

