

Intro. to Computer Architecture
CSE 240 Autumn 2004**Homework 4**
DUE: Mon. 11 October 2004

Write your answers on these pages. Additional pages may be attached (with staple) if necessary. Please ensure that your answers are legible. Please show your work. Due at the *beginning of class*. Total points: 60.

1. [6 Points] **Instruction Encoding.** Suppose a machine encodes instructions in 32-bits according to the following format. Assume there are 290 opcodes and 60 registers.

OPCODE	DR	SR1	SR2	UNUSED
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- (a) What is the minimum number of bits required to represent the OPCODE field?
- (b) What is the minimum number of bits required to represent each of the register fields (*e.g.*, DR)?
- (c) What is the maximum number of bits left available for the UNUSED field and how many values could it encode?
2. [12 Points] **LC-3 Instruction Encoding.** For these questions assume the LC-3 instruction encoding (inside the back cover of your textbook). You may also need to consult Appendix A.
- (a) What is the range of values (in decimal) that may be specified by the immediate field in an AND instruction?

3. [14 Points] **LC-3**. Suppose you want to execute the program made up of the instructions in the final column of following table.

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Instruction
x3001																	R2 <- M[R1+0]
x3002																	R3 <- M[R1+1]
x3003																	BRzp x3006
x3004																	R3 <- NOT R3
x3005																	R3 <- R3 + 1
x3006																	R2 <- R2 + R3
x3007																	M[R1+2] <- R2

- (a) Give the binary encoding of each instruction in the table. Write your answers in the table, above.
- (b) Trace the execution of the above program, starting at x3001, by completing the following table. Give the PC and instruction to execute in the first two columns, and give the state of the registers and condition codes *after* the execution of that instruction (**leave an entry blank if it has not been changed by the instruction**). The initial register state and the effect of the first instruction are given in the first two rows. Assume memory locations x3100 and x3101 contain 2 and -3, respectively.

PC	Instruction	R0	R1	R2	R3	R4	R5	R6	R7	CCs
<i>initial register state</i> ⇒		0	x3100	0	3	4	5	6	7	
x3001	R2 <- M[R1+0]			2						P

- (c) In a sentence, what does this code compute?

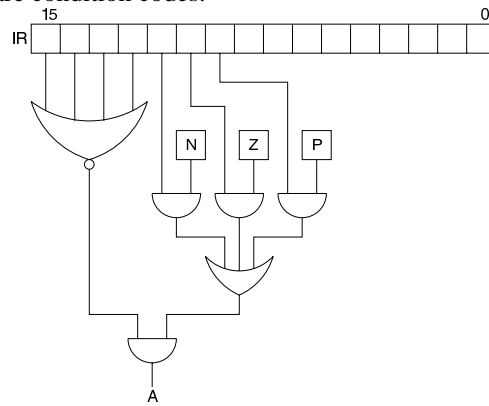
- (c) Describe what this code does, assuming execution starts at address x3001. What registers or memory serve as input to this code? And what registers or memory serve as output? Be very careful in determining the input and output (*i.e.*, just because a register appears in the code does not mean that it is input or output).

- (d) Under what circumstances will this program fail to perform its principal task?

5. [6 Points] **Instruction Processing.** The PC, IR, MAR, MDR, and RF (register file) are structures written in various phases of the instruction processing cycle, depending on the opcode of the particular instruction being executed. In each cell in the table below, enter the opcodes that write to each structure (row) during the corresponding phase (column) of the instruction processing cycle. To make this simpler, let's only consider the following opcodes: AND, LDR, STR, and JMP.

	FETCH	DECODE	EVAL ADDR	FETCH OPERANDS	EXECUTE	STORE
PC						
IR						
MAR						
MDR						
RF						

6. [6 Points] **LC-3 Implementation.** Consider the logic diagram below showing part of the control structure of an LC-3 machine. N, Z, and P are condition codes.



(a) What does the output of the NOR gate tell us?

(b) What does the output of the OR gate tell us?

(c) What is the purpose of the signal labeled A?

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7. [No Points] **Last and Most Important Question!** Please give us your feedback!

(a) How many hours did you spend on this assignment?

(b) On a scale of 1-5, how difficult did you find this assignment? (1-easiest, 5- most difficult)

(c) Do you have any other comments on your experience completing this assignment? What are they?