1. The measured voltage and current data for an MOS transistor are given below.

<table>
<thead>
<tr>
<th>$V_{gs}$ (V)</th>
<th>$V_{ds}$ (V)</th>
<th>$V_{sb}$ (V)</th>
<th>$I_{ds}$ (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>3</td>
<td>0</td>
<td>100</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>0</td>
<td>225</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>0</td>
<td>400</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3</td>
<td>64</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>3</td>
<td>169</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>3</td>
<td>324</td>
</tr>
</tbody>
</table>

(a) Determine the type of the transistor (i.e. n or p and enhancement or depletion) and its mode of operation (i.e. cutoff, non-saturated, saturated). (5 pts)

(b) Calculate values for $\beta_n$, $V_{T0}$, and $V_T$. Assume $\lambda = 0$. (20 pts)

Solution:

(a). The MOS transistor is in the ON state $I_{ds} > 0$ for $V_{gs} > 0$ and $V_{ds} > 0$. Thus the device must be an n-type enhancement transistor. Since $V_{ds} = V_{gs} > V_{gs} - V_T$, the transistor is operating in saturation.

(b). To compute $\beta_n$: use $I_{ds} = \frac{\beta_n}{2} (V_{gs} - V_T)^2$ or $\sqrt{I_{ds}} = \sqrt{\frac{\beta_n}{2}} (V_{gs} - V_T)$. Note that $V_T$ is given by

$$V_T = V_{T0} + \gamma [\sqrt{2\phi_b + |V_{sb}|} - \sqrt{2\phi_b}]$$

Let $I_{ds1}$, $V_{gs1}$ and $I_{ds2}$, $V_{gs2}$ be two current-voltage pairs from the given table. Then we can eliminate $V_T$ by forming the difference

$$\sqrt{I_{ds1}} - \sqrt{I_{ds2}} = \frac{\beta_n}{2} (V_{gs1} - V_{gs2})$$

Solving for $\beta_n$ yields

$$\beta_n = \frac{2 \sqrt{I_{ds1}}}{V_{gs1} - V_{gs2}} \sqrt{I_{ds2}} - \sqrt{I_{ds2}} = \frac{2 \sqrt{400 \mu A - 100 \mu A}}{5V - 3V} = \frac{2 \sqrt{[20 - 10]^2 \mu A}}{2 \times 2V^2} = 50 \mu A/V^2$$

To compute $V_{T0}$: use data for $V_{sb} = 0$ V, i.e. $V_T = V_{T0}$ in $\sqrt{I_{ds}} = \sqrt{\frac{\beta_n}{2}} (V_{gs} - V_T)$. 


Solve $\sqrt{I_{ds}} = \sqrt{\frac{\beta_n}{2}(V_{gs} - V_{T0})}$ for $V_{T0}$ and use any $I_{ds}$, $V_{gs}$ pair where $V_{sb} = 0$, i.e.

$$V_{T0} = V_{gs} - \sqrt{\frac{2I_{ds}(V_{sb} = 0\text{V})}{\beta_n}} = 3\text{ V} - \sqrt{\frac{2(100)\mu\text{A}}{50\mu\text{A/V}^2}} = 3\text{ V} - \sqrt{4\text{ V}} = 1\text{ V}$$

To compute $V_T$: use use data for $V_{sb} = 3\text{ V}$ and $\sqrt{I_{ds}} = \sqrt{\frac{\beta_n}{2}(V_{gs} - V_{T})}$. Solve for $V_T$ and use any $I_{ds}$, $V_{gs}$ pair where $V_{sb} = 3\text{ V}$, i.e.

$$V_T = V_{gs} - \sqrt{\frac{2I_{ds}(V_{sb} = 3\text{V})}{\beta_n}} = 3\text{ V} - \sqrt{\frac{2(64)\mu\text{A}}{50\mu\text{A/V}^2}} = 3\text{ V} - \sqrt{2.56\text{ V}} = 1.4\text{ V}$$

2. Consider the resistive-load inverter circuit in Figure P2 and the SPICE data in TABLE 4 on page 6 of the formula/data handout.

(a) Determine the $V_{OH}$ for this inverter circuit. (5 pts)

(b) Determine the $W/L$ ratio of the driver transistor to achieve a $V_{OL} = 0.1\text{ V}$. (12 pts)

(c) If the input voltage is "low" for 50% of the inverter’s operation and "high" for the remaining 50%, what is the average static power dissipated by this inverter. (8 pts)

Solution:
Let’s label transistor terminals and the currents, i.e.
Note that $V_{gs} = V_{in}$ and $V_{ds} = V_{out}$. The current flowing through $R$ is $I_R = \frac{5V - V_{out}}{R}$ and $I_R = I_{ds}$. Let's establish the modes of operation for the n-channel driver transistor, i.e.

- $V_{in} < V_{T0}$ => driver transistor is cut-off
- $V_{T0} \leq V_{in} < V_{out} + V_{T0}$ => driver transistor is saturated
- $V_{in} > V_{out} + V_{T0}$ => driver transistor is unsaturated

(a) $V_{OH}$ is determined when $V_{in} = 0$ V. $V_{in} = 0$ V => the driver is cutoff, thus $I_{ds} = I_R = 0$ and $V_{out}$ pulls up to 5 V. Therefore $V_{OH} = 5$V.

(b) $V_{OL}$ is determined when $V_{in} = 5$ V, $V_{in} = 5$ V => the driver is unsaturated. In the unsaturated region $I_{ds} = \beta ((V_{in} - V_{T0})V_{out} - \frac{V_{out}^2}{2}) = KP \frac{W}{L} ((V_{in} - V_{T0})V_{out} - \frac{V_{out}^2}{2})$ where $KP = 8.5 \times 10^{-5}$ A/V$^2 = 85$ µA/V$^2$ and $V_{T0} = 0.7$ V from the SPICE data in TABLE 4.

With $I_R = I_{ds}$ and $V_{T0} = 0.7$ V, $V_{out} = V_{OL} = 0.1$ V when $V_{in} = 5$ V; i.e.

$$\frac{5V - V_{out}}{R} = KP \frac{W}{L} ((V_{in} - V_{T0})V_{out} - \frac{V_{out}^2}{2}) \Rightarrow \frac{5 - 0.1}{10^5} = 8.5 \times 10^{-5} \frac{W}{L} ((5 - 0.7)0.1 - \frac{(0.1)^2}{2})$$

$$4.9 = 8.5 \frac{W}{L} (0.43 - 0.005) \Rightarrow \frac{W}{L} = \frac{4.9}{8.5 (0.43)} = 1.34$$

(c) The current drawn from the power supply in pull-down is $I_{ds} = I_R = \frac{5V - V_{out}}{R}$, where $V_{out} = V_{OL} = 0.1$ V. In pull-up, since the driver transistor is cut-off, no current is drawn from the supply in pull-up. The static power drawn in pull-down is as follows:

$$P_{spull-down} = 5V I_R = 5V \left( \frac{5V - V_{OL}}{R} \right) = 5 (4.9) \times 10^{-5} W = 245 \mu W$$

With the input high 50 % of the time, $P_{sav} = 0.5 P_{spull-down} = 122.5$ mW
3. The unloaded pseudo NMOS inverter Fig. P3a is fabricated in a 1 μm n-well CMOS process. The \( \lambda \) design rules and SPICE data for this process are given in TABLES 4 and 5, on pages 6-8 of the formula/data handout, respectively.

![Figure P3](image)

The layouts for the two transistors are shown in Fig. P3b without labels for mask levels and dimensions.

(a) With \( \lambda = 0.5 \) μm, let the pull-down transistor be a unit transistor. Label the appropriate mask levels in Fig. P3b and provide all the dimensions needed to represent the layout of the minimum size device for which the source, drain can be properly contacted to metal1 (i.e. complies with the design rules in TABLE 5).

(b) The pull-up transistor is to be sized so that \( \beta_n/\beta_p = 7.5 \). Label the appropriate mask levels in Fig. P3b and provide all the dimensions needed to represent the minimum size layout required to properly connect its source, drain to metal1 (i.e. complies with the design rules in TABLE 5).

(c) The SPICE simulation for the pseudo NMOS inverter yielded the following transfer characteristic data:

<table>
<thead>
<tr>
<th>( V_{\text{in}} ) (V)</th>
<th>0.00</th>
<th>1.00</th>
<th>1.10</th>
<th>1.20</th>
<th>1.40</th>
<th>1.60</th>
<th>1.80</th>
<th>2.00</th>
<th>2.20</th>
<th>2.30</th>
<th>4.00</th>
<th>5.00</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{out}} ) (V)</td>
<td>5.00</td>
<td>5.00</td>
<td>4.95</td>
<td>4.85</td>
<td>4.02</td>
<td>3.23</td>
<td>2.37</td>
<td>1.61</td>
<td>0.72</td>
<td>0.62</td>
<td>0.52</td>
<td>0.50</td>
</tr>
</tbody>
</table>

From the data determine \( V_{\text{OL}} \), \( V_{\text{OH}} \) and estimate \( V_{\text{IL}} \), \( V_{\text{IH}} \), and the low and high noise margins.
Solution:
(a) 

(b) From the SPICE data we find that mobilities $\mu_n = 2.5 \mu_p$; thus, to make $\beta_n/\beta_p = 7.5$ we require 

$$\frac{\beta_n}{\beta_p} = \frac{\mu_n C_{ox} (W_n/L_n)}{\mu_p C_{ox} (W_p/L_p)} = \frac{\mu_n (W_n/L_n)}{\mu_p (W_p/L_p)} = \frac{2.5 (3/1)}{7.5} = 7.5 > \frac{W_p}{L_p} = 7.5 = 1$$

To achieve minimum dimensions one might be tempted to make $L_p = W_p = 1 \mu$; however, that sizing would not allow for contacts to source, drain that meet the specified design rules. In (a) we determined that the minimum $W_p$ that permits contacts is $W_p = 3 \mu$. Then for $W_p/L_p = 1$, $W_p = 3 \mu \Rightarrow L_p = 3 \mu$, and the pull-down device layout is as follows:
(c) 

\[
\begin{array}{cccccccccccc}
V_{\text{in}} (V) & 0.00 & 1.00 & 1.10 & 1.20 & 1.40 & 1.60 & 1.80 & 2.00 & 2.20 & 2.30 & 4.00 & 5.00 \\
V_{\text{out}} (V) & 5.00 & 5.00 & 4.95 & 4.85 & 4.02 & 3.23 & 2.37 & 1.61 & 0.72 & 0.62 & 0.52 & 0.50 \\
\end{array}
\]

By inspection $V_{\text{OH}} = 5 \text{ V}$ and $V_{\text{OL}} = 0.5 \text{ V}$. From the data $V_{\text{out}}/V_{\text{in}} = -1$ at $V_{\text{IL}} = 1.1 \text{ V}$ and $V_{\text{IH}} = 2.2 \text{ V}$. The noise margins are

\[
\begin{align*}
NM_{\text{H}} &= |V_{\text{IL}} - V_{\text{OL}}| = |1.1 - 0.5| = 0.6 \text{ V} \\
NM_{\text{L}} &= |V_{\text{OH}} - V_{\text{IH}}| = |5 - 2.2| = 2.8 \text{ V}
\end{align*}
\]

4. The setup in Figure P4a is used to develop delay models for a CMOS two-input NAND gate. The corresponding SPICE delay data is tabulated in Figure P4b.

(a) Determine the gate delay equations, for both rising and falling inputs, in the form of $t_d = t_{\text{internal}} + k \times t_{\text{output}}$. (5 pts)

(b) Determine the effective resistances for the pull-up and pull-down transistors, i.e. $R_p$ and $R_n$ respectively, for the two-input NAND gate simulated in Figure P4. (10 pts)

(c) Determine the internal or intrinsic capacitance for the 2-input NAND gate simulated in Figure P4. (10 pts)

Solution:

(a) From the data $t_{\text{dr}} = 0.500 \text{ ns} + k \times (2.0 \text{ ns/pF})$ and $t_{\text{df}} = 0.400 \text{ ns} + k \times (1.6 \text{ ns/pF})$

(b) Note that for the configuration in Figure P4a, one input is tied high and the other is driven from a source. With one input tied high one of the two parallel p-channel pull-up transistors is OFF and one of the two n-channel pull-down transistors is ON independent of the input.
Consequently, the total effective resistance seen in pull-up is one transistor $R_p$ and total effective resistance seen in pull-down is $2R_n$. For $C_L = 1$ pF, the $R_n$ and $R_p$ can estimated from the extrinsic components of $t_{df}$ and $t_{dr}$, respectively, i.e. $C_L = 1$ pF => $k = 1$

$$C_L R_p = k \times (2.0 \text{ ns/pF}) \Rightarrow R_p = \frac{2 \times 10^{-9}}{1 \times 10^{-12}} = 2 \text{ k}\Omega$$

$$C_L (2R_n) = k \times (1.6 \text{ ns/pF}) \Rightarrow R_n = \frac{1.6 \times 10^{-9}}{1 \times 10^{-12}} = 0.8 \text{ k}\Omega$$

(c) The internal or intrinsic load capacitance is estimated from either the intrinsic component of $t_{dr}$ or $t_{df}$, i.e.

$$C_{\text{intrinsic}} R_p = 0.5 \text{ ns} \Rightarrow C_{\text{intrinsic}} = \frac{0.5 \times 10^{-9}}{2 \times 10^3} = 0.25 \text{ pF}$$

5. The delays for a CMOS inverter, with $V_{\text{DD}} = 5$ V and internal load capacitance $C_d = 0.1$ pF, were modeled from SPICE data as follows:

$t_{dr} = 0.125 \text{ ns} + k \times (1.250 \text{ ns/pF})$ and $t_{df} = 0.100 \text{ ns} + k \times (1.000 \text{ ns/pF})$.

This inverter is driving 6 gates in parallel; where each of the 6 driven gates and routing (to the drive inverter) is comprised of one $10 \mu\text{m} \times 5 \mu\text{m}$ drive transistor, $200 \mu\text{m} \times 1 \mu\text{m}$ of metal1 and a $200 \mu\text{m} \times 1 \mu\text{m}$ of poly.

(a) Determine the total external load capacitance seen by the drive inverter due to the 6 driven gates. (10 pts)

(b) Determine the delay rise and fall times for the drive inverter with the load obtained from (a). (7 pts)

(c) If the input to the fully loaded drive inverter causes the load capacitance to charge and discharge every 100 ns, determine the power dissipated by the drive inverter. (8 pts)

Solution:

(a) $C_L = 6 \left[ C_g + C_{\text{metal1}} + C_{\text{poly}} \right]$

$$= 6 \left[ (10 \times 5) \times 1800 + (200 \times 1) \times 30 + (200 \times 1) \times 50 \right] \times 10^{-18} \text{ F}$$

$$= 6 \left[ 90,000 + 6000 + 10,000 \right] \times 10^{-18} \text{ F} = 0.636 \text{ pF}$$

(b) With $C_L = 0.636 \text{ pF}$

$$t_{dr} = 0.125 \text{ ns} + 0.636 \times (1.250 \text{ ns/pF}) = 0.920 \text{ ns}$$

$$t_{df} = 0.100 \text{ ns} + 0.636 \times (1.000 \text{ ns/pF}) = 0.736 \text{ ns}$$

(c) $P = C_{\text{total}} V_{\text{DD}}^2 f = (C_d + C_L) 25 \left( 1/100 \text{ ns} \right)$

$$= (0.1 \times 10^{-12} + 0.636 \times 10^{-12}) \times 25 	imes 10^7 = 184 \mu\text{W}$$