Lab 6: VGA Controller

Discussion Questions

Due: Monday, April 16, 2012 at 11:59pm (ALL SECTIONS)

For this lab, you will answer several discussion questions that ask you to think about the concepts learned in this lab. You should submit a PDF of your answers on Blackboard. There will be a 10%/day penalty for late submissions. This is an INDIVIDUAL assignment. EACH student must submit their own answers to these questions.

There are eight (8) discussion questions. You are NOT required to submit screenshots.

1) For each situation below, explain whether or not the one-pulse circuit you designed in lab would be applicable. If the one-pulse is applicable, describe why it would be useful and how you would interface it with the design. If the one-pulse is not applicable, explain why it is not needed. Assume a fast clock period (on the order of 10 ns)

   a) A circuit which will play a tone for as long as a button is held down.
   b) A circuit which a tone plays after a button is pressed, and continues to play until the same button is pressed again.
   c) A circuit which bakes a pie if a button is pressed, but will electrocute a child if the same button is pressed three times in succession.

2) Many computers and displays have switched from using VGA connections to either DVI or HDMI. Look up DVI and HDMI. What are some major differences between these and VGA? Why do you think people are starting to prefer them over VGA?

3) The method used to generate the RGB color values in this lab is a purely combinational function (implemented in hardware on the FPGA) that takes the (X,Y) coordinates of the pixel currently being drawn and outputs the 8-bit values of R, G, and B. Would a purely combinational module like this be feasible to use to draw a color screen for a modern computer and operating system (assume delay is not an issue)? Why or why not?

4) In this lab, we use a DCM to divide an input clock by 4. While it is generally good practice to use a DCM to divide a clock, when dividing a clock by a power of 2, it is
usually tempting to implement your own divider, because the logic is usually simpler than figuring out how to use a DCM (thankfully, you have the IP generator available). Using any gates and/or flip-flops you would like, implement a module that divides an input clock frequency by 4.

5) Recall that there exists a “front porch” and a “back porch” in timing for VGA. Why do you think these might exist?

6) There are two kinds of buffers used by your design: BUFG and IBUF. Which should be used to buffer the divided clock output from your answer to question 4? Hint: To see the data sheet, add the two components to a schematic in Xilinx, right-click on the symbol, go to “Symbol”, and “Symbol Info”

7) The output from a "global" buffer is able to handle much higher fan out (number of components an output signal is connected to) than that of a regular buffer, even though both perform the same logical operation (output follows the input). What does one have to change about a regular buffer to make it into a global buffer (that can support large fan out)? You should be as specific as possible, but your answer should be qualitative not quantitative.

8) What components of your design (the VGA controller) would you have to change to make it output for the XGA standard resolution (which you looked up in the pre-lab) instead of the VGA standard? You only need to state the components that would change, not how much they would change by.