Common Emitter (CE) BJT Amplifier

CE BJT Amplifier

CS MOS Amplifier
**The Right Way – Use a “Blocking” Capacitor**

1. Capacitor $C_{in}$ is an OPEN at dc and $v_s, R_S$ do not affect the bias!

2. Capacitor $C_{in}$ is a SHORT at some $f \geq f_{min}$ and $v_B \approx V_B + v_s$

**DESIGN GOAL:** for $f \geq f_{min}$, set the value of $C_{in}$ s.t. the ac base voltage $v_b \approx v_s$.

For convenience lets continue to use the “base bias Thevenin equiv”.

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Kenneth R. Laker, updated 18Sep13 KRL
Blocking Capacitor Selection

Using superposition, for small-signal let \( V_B = V_{CC} = 0 \).

\[
\begin{align*}
V_s & = 1 \text{ V/1 kHz/0 Deg} \\
R_s & = 50 \text{ Ohm} \\
R_B & = 20 \text{ kOhm} \\
R_E & = 4 \text{ kOhm} \\
\beta & = 100 \\
C_{in} & \\
\end{align*}
\]

\[
\begin{align*}
\nu_b & = i_b r_{\pi} + i_e R_E = i_b r_{\pi} + i_b (\beta + 1) R_E \\
r_{bg} & = \frac{\nu_b}{i_b} = r_{\pi} + (\beta + 1) R_E \approx \beta R_E
\end{align*}
\]

Use the small signal equivalent circuit and superposition to estimate the input resistance of the transistor.
Capacitor Selection- continued

The signal source “sees” the 20 kΩ bias source resistance in parallel with $\beta R_E$. So the signal source equivalent circuit is:

Using the voltage-divider relation:

$$v_b = \frac{R_B \| r_{bg} \ v_s}{R_B \| r_{bg} + R_S + \frac{1}{j \omega C_{in}}} \approx \frac{R_B v_s}{R_B + \frac{1}{j \omega C_{in}}}$$

Design objective: for a known $R_B$, determine $C_{in}$ s.t. $v_b \approx v_s$

i.e. $R_B \gg \left| \frac{1}{j \omega C_{in}} \right| \Rightarrow 2\pi f C_{in} R_B \gg 1$

$$r_{bg} \approx 100 R_E = 400 \ k\Omega$$

Therefore:

$$R_B \| r_{bg} = \frac{400}{420} 20 \approx 20 \ k\Omega = R_B$$
Capacitor Selection - continued

\[ 2\pi f C_{in} R_B \gg 1 \implies C_{in} \gg \frac{1}{2\pi f R_B} \]

**FACTOR-OF-10 DESIGN GOAL:** Choose \( C_{in} \) s.t. for a specified min frequency \( f = f_{min} \)

\[ C_{in} = \frac{10}{2\pi f_{min} R_B} \]

Hence

\[ v_b \approx \frac{R_B v_s}{R_B + \frac{1}{j 2\pi f C_{in}}} = \frac{R_B v_s}{R_B + \frac{R_B f_{min}}{10 f}} = \frac{v_s}{1 + \frac{1}{10} \frac{f_{min}}{f}} \]

for \( f = f_{min} \) \( v_b \approx \frac{v_s}{1 + \frac{1}{10}} = 0.91 v_s \)

& for \( f = 10 f_{min} \) \( v_b \approx \frac{v_s}{1 + \frac{1}{100}} = 0.99 v_s \)
Capacitor Selection - continued

Select the LOWEST frequency of interest. This sets the lower bound on $C_{in}$. Using $f_{min} = 20 \text{ Hz}$ frequency for our example circuit:

$$2 \pi f_{min} = 2 \pi 20 \approx 6.28 \cdot 20 = 125.6 \text{ sec}^{-1}$$

$$C_{in} = \frac{10}{2 \pi f_{min} R_B} = \frac{10}{125.6 \cdot 20 \cdot 10^3} = \frac{10^{-6}}{0.25} = 4 \mu F$$

ANY capacitor larger than $4 \mu F$ will also do the job!

Let’s choose $C_{in} = 5 \mu F$
**Quick Review**

\[ A_v = \frac{v_o}{v_s} = ? \]

**DESIGN GOAL:** What is the design goal for setting the value of \( C_{in} \)?
Quick Review

**DESIGN GOAL:** for $f \geq f_{\text{min}}$, set the value of $C_{\text{in}}$ so that the ac base voltage $v_b \approx v_s$.

$$A_v = \frac{v_o}{v_s} = \frac{-R_C}{R_E}$$

$$R_B \gg \left| \frac{1}{j2\pi f C_{\text{in}}} \right|$$
Common Emitter Unity Gain Amplifier

How can we achieve reasonable gain with this circuit?

Solution: Split $R_E$ and use capacitor bypassing.
Bypass for Gain

Procedure:
1. Split the emitter resistor in two. Later, we will show that the voltage gain will be close to \(-\frac{R_C}{R_{E1}}\).

2. Bypass \(R_{E2}\) with a capacitor \(C_{byp}\) that looks like a near “short circuit” at some suitable low frequency \((f = f_{\text{min}})\).

i.e. \(|v_{ZE2}| < |v_{RE1}|\) for \(f \geq f_{\text{min}}\)

\[
Z_{E2} = R_{E2} \parallel \frac{1}{j2\pi f C_{byp}}
\]

\[
v_{RE1} = i_e R_{E1} \quad \& \quad v_{ZE2} = i_e Z_{E2}
\]
Bypass for Gain - continued

Small signal circuit

\[ \beta = 100 \]

Desired circuit for \( f \geq f_{\text{min}} \)

i.e. CONSERVATIVE DESIGN GOAL:
Choose \( C_{\text{byp}} \) s.t.
\[ |v_{ZE2}| = 0.1 \quad |v_{RE1}| \quad \text{for} \quad f \geq f_{\text{min}} \]
Need to develop a design equation for $C_{\text{byp}}$

s.t. DESIGN GOAL: $|v_{ZE2}| << |v_{RE1}|$

where

$$Z_{E2} = R_{E2} \parallel \frac{1}{j2\pi C_{\text{byp}}} = \frac{R_{E2}}{j2\pi f \ C_{\text{byp}} \ R_{E2} + 1}$$

$$\left| \frac{v_{ZE2}}{v_{RE1}} \right| = \left| \frac{Z_{E2} i_e}{R_{E1} i_e} \right| = \left| \frac{R_{E2}/R_{E1}}{j2\pi f_{\text{min}} C_{\text{byp}} \ R_{E2} + 1} \right| = \frac{1}{10}$$

or

Solving for $C_{\text{byp}}$:

$$C_{\text{byp}} = 10 \left( \frac{R_{E2}}{R_{E1}} \right) \frac{1}{2\pi f_{\text{min}} R_{E2}} = \frac{10}{2\pi f_{\text{min}} R_{E1}}$$

a larger value $C_{\text{byp}}$ also works
\[ C_{byp} = \frac{10}{2\pi f_{\text{min}} R_{E1}} = \frac{10}{2\pi \times 20 \times 1000} \quad F = 79.6 \mu F \]

Let's choose \( C_{byp} = 100 \mu F \)

**Final Design**

![Circuit Diagram]

- \( C_{\text{in}} = 5 \mu F \)
- \( R_S = 50 \) Ohm
- \( R_I = 51 \) kOhm
- \( R_C = 4 \) kOhm
- \( R_E1 = 1 \) kOhm
- \( R_E2 = 3 \) kOhm
- \( C_{byp} = 100 \mu F \)
- \( V_s = 1 \) V/1 kHz/0 Deg
- \( V_{cc} = 12 \) V

Kenneth R. Laker, updated 18Sep13 KRL
Mid-band Gain Calculation in Passband

Simple gain calculation:

\[ i_b = \frac{v_s}{R_s + r_{\pi} + (\beta + 1) R_{E1}} \approx \frac{v_s}{(\beta + 1) R_{E1}} \]

\[ v_{out} = -R_C i_c = -R_C \beta i_b \]

\[ v_{out} = \frac{-\beta R_C}{(\beta + 1) R_{E1}} v_s \]

\[ A_v = \frac{v_{out}}{v_s} \approx -\frac{R_C}{R_{E1}} = -4 \]

Mid-band model

\[ f_{\text{min}} \leq f \leq f_{3\text{dBH}} \]

Kenneth R. Laker, updated 18Sep13 KRL
Multisim Simulation

20 Hz Gain

1 kHz Gain
What if $R_E$ is Fully Bypassed?

$$A_v = \frac{v_{out}}{v_s} \approx -\frac{R_C}{R_E} = \infty \ ?$$
What if $R_F$ is Fully Bypassed?

\[
i_b = \frac{V_s}{R_s + r_\pi + (\beta + 1) R_E} = \frac{V_s}{R_s + r_\pi} \approx \frac{V_s}{r_\pi}
\]

\[
V_o = -R_C i_c = -R_C \beta i_b
\]

where \( i_b \approx \frac{V_s}{r_\pi} \)

\[
V_o \approx -\beta R_C r_\pi 
\]

\[
V_s = -\frac{\beta R_C}{\beta/g_m} V_s = -g_m R_C V_s
\]

\[
A_v = \frac{V_o}{V_s} \approx -g_m R_C = -160
\]

Note Temp Sensitivity: \( A_v \approx -\frac{I_C}{V_T} R_C \) where \( V_T = \frac{kT}{q} \)
Two Power Supply Version of Base Bias Scheme

\[ I_C = \beta I_B = \frac{\beta}{R_B + (\beta+1)R_E} (V_B - V_{BE}) \]

\[ I_C = \beta I_B = \frac{\beta}{R_B + (\beta+1)R_E} (V_{EE} - V_{BE}) \]
Some Observations

- Conditions for stabilized voltage source biasing.
  - Emitter resistance, $R_E$, is needed.
  - Base voltage source will have finite resistance, $R_B$, i.e.
    $$(1 + \beta) R_E \gg R_B \gg R_S.$$  
  - Small $R_B$ - relative to $R_S$ - will attenuate input signal.
  - Larger $R_E$ permits larger $R_B$, but results in lower gain.
    - Gain = $-R_C/R_E$ for $R_E \gg r_e$.
  - Split $R_E$ with bypass capacitor increases gain.
    - Requires large bypass capacitor.
    - Limiting case - entire $R_E$ bypassed: Gain = $-g_m R_C$.

- Conservatively use “1/3, 1/3, 1/3” rule. $R_C$ & $R_E$ determine bias and gain.