Common Emitter BJT Amplifier Design

Current Mirror Design
**Design Example**

Design an amplifier to meet the following specifications:

**Electrical specifications:**

- $v_{s\text{--max}} = 0.1 \, V_{pk}$
- $R_s = 50 \, \Omega$
- $V_{cc} = 12 \, V$
- $0 \, C < T < 40 \, C$ → Requires simulation to verify.

**Minimize cost:**

1. Use standard 5% resistors
2. Minimize number of external capacitors

More typical gain spec:

$9.5 \leq |A_v| \leq 10.5$ or $10 \pm 5\

@ midband

$f_{\text{min}} = 20 \, Hz$
Design Step 1 (Set $R_B$ and $R_E$)

Choose an $R_B \gg 10R_S$:

$$R_B = 5000 \, \Omega$$

$$(1 + \beta) R_E \text{ must be } \geq 10R_B :$$

$$R_E = \frac{10 \cdot 5000}{100} = 500 \, \Omega$$

Nearest standard size*: $470 \, \Omega$

$$R_E = 470 \, \Omega$$

*RCA Lab: [http://www.ese.upenn.edu/rca/components/passive/listcomponents.html#resistors](http://www.ese.upenn.edu/rca/components/passive/listcomponents.html#resistors)
Design Step 2 (Set $R_c$)

For a gain of $A_v = -10$:

$$R_c = 10 R_E = 4.7 \, k\Omega$$

Nearest standard size*:

$$R_c = 4.7 \, k\Omega$$

SPEC: $v_{s_{-max}} = 0.1 \, V \, pk$

For a gain of $-10$, the max ac collector voltage $v_{o_{-max}}$ swing is $1 \, V \, pk$; hence, the dc $V_{RC} > 1 \, V$. 

$\beta = 100 \quad R_B = R_1 \parallel R_2 = 5 \, k\Omega$

$R_E = 470 \, \Omega$
Design Step 3 (Set bias point neglecting $I_B$)

Recall $v_{\text{sig-max}} = 0.1 \text{ V pk}$ and $|A_v| = 10$

We have plenty of room - choose the dc collector-resistor voltage conservatively to allow for bias point changes with temperature – let's use:

$$V_{R_C} = 4.7 \text{ V} \approx \frac{V_{CC}}{3}$$

Thus:

$$I_C = \frac{4.7}{4700} = 1 \text{ mA}.$$ 

And (ignoring $I_B$):

$$V_B = V_{BG} \approx I_C R_E + 0.7 = 0.47 + 0.7 = 1.17 \text{ V}.$$
Design Step 4 (Set $R_1$ and $R_2$)

Recall:

$$R_B = R_1 \parallel R_2 = R_1 \frac{R_2}{R_1 + R_2} = 5 \text{ k}\Omega$$

And:

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = 1.17 V$$

Or:

$$\frac{R_2}{R_1 + R_2} = \frac{V_B}{V_{CC}} = \frac{1.17}{12} = 0.098 \approx 0.1$$

$\beta = 100$  
$R_B = 5 \text{ k}\Omega$  
$R_E = 470 \Omega$  
$R_C = 4.7 \text{ k}\Omega$
Design Step 4 cont. (Set $R_1$ and $R_2$)

Substituting:

$$R_1 \| R_2 = R_1 \frac{R_2}{R_1 + R_2} = R_1 \cdot 0.1 = 5 \, k\Omega$$

$$R_1 = 50 \, k\Omega$$

Standard size:

$$R_1 = 47 \, k\Omega$$

Finally:

$$\frac{R_2}{47 \, k + R_2} = 0.1$$

$$0.9 \, R_2 = 0.1 (47k) \Rightarrow R_2 = 5222 \, \Omega$$

Standard size:

$$R_2 = 5.1 \, k\Omega$$

Revised $R_B$:

$$R_B = R_1 \| R_2 = \frac{(47k) \cdot 5.1 \, k}{52.1 \, k} = 4.6 \, k\Omega$$

\[\beta = 100\]

$$R_B = 4.6 \, k\Omega$$

$$R_E = 470 \, \Omega$$

$$R_C = 4.7 \, k\Omega$$

NOTE: $(1 + \beta) \, R_E \approx 47 \, k\Omega \geq 10 \, R_B = 46 \, k\Omega$
**Design Step 5 (set \( C_{in} \)) - Close to the Finish!**

\( I_C = 1 \text{ mA} \)
\( \beta = 100 \)
\( r_\pi = 2.5 \text{ k} \Omega \)

Estimate \( R_{in} \):
\[
r_{bg} = r_\pi + (\beta + 1) R_E \approx 47.5 \text{ k} \Omega
\]
\[
R_B \parallel r_{bg} \approx 4.2 \text{ k} \Omega
\]

\( R_B \) in parallel with \( r_{bg} \) => \( R_B \) dominates.

Estimate \( R_B \parallel r_{bg} \) as 4.2 k \( \Omega \). Coupling capacitor reactance, then, should be about 420 \( \Omega \) at \( f = f_{min} \).

\[
\left| \frac{1}{j 2 \pi f_{min} C_{in}} \right| = 420 \Omega
\]
\[
C_{in} = \frac{10}{2 \pi f_{min} 420 \Omega}
\]

\[
C_{in} = \frac{1}{420 \cdot \frac{2 \pi}{20}} = \frac{1.19 \cdot 10^{-4}}{2 \pi} \approx 19 \mu F
\]

Using the RCA Lab Component List

\[
C_{in} = 22 \mu F
\]
Final Design

\[ C_i n = 22 \mu F \]

\[ R_s = 50 \text{ Ohm} \]

\[ R_1 = 47 \text{ k Ohm} \]

\[ R_2 = 5.1 \text{ k Ohm} \]

\[ V_s \]

\[ R_c = 4.7 \text{ k Ohm} \]

\[ V_o \]

\[ V_{cc} = 12 \text{ V} \]

\[ Re = 470 \text{ Ohm} \]
**Multisim Simulation**

**20 Hz Gain**
Actual \( |A_V(f = 20.7 \text{ Hz})| = 9.27 \approx 9.3 \)

**1 KHz Gain**
Actual \( |A_V(f = 1 \text{ kHz})| = 9.3 < 10 \)
Multisim Oscilloscope Plots
Discussion

1. We neglected $r_e$. Including the internal emitter resistance, the simulated gain becomes:

$$A_V = - \frac{R_C}{R_E + r_e} = - \frac{4700}{470 + 25} = -9.5$$

2. There is some attenuation of the signal voltage at the base. A more accurate calculation of the input attenuation:

$$R_B \parallel r_{bg} = 4.2 \, k\Omega \Rightarrow v_{bg} \approx \frac{R_B \parallel r_{bg}}{R_B \parallel r_{rg} + R_S} = \frac{4200}{4250} v_{sig} = 0.988 v_{sig}$$

Multiplying the two quantities:

$$A_v = -9.5 \cdot 0.988 = -9.4 \text{ Close to 9.3!}$$

This fine-tuning of the estimate may not be all that helpful – since we will be using 5% components to build the circuit!
1. If NO $R_E$ & $C_E$, what is the approx. mid-band voltage gain?

2. If $R_E$ & $C_E$, what is the approx. mid-band voltage gain?

3. What is the purpose of $C_I$?
Common Emitter Amplifier - Current Source Biasing

1. If NO $R_E$ & $C_E$, what is the approx. mid-band voltage gain?
   \[ \frac{v_o}{v_s} = -\frac{R_C}{r_o} \ll 1 \]

2. If $R_E$ & $C_E$, what is the approx. mid-band voltage gain?
   \[ \frac{v_o}{v_s} = -\frac{R_C}{R_E} \]

3. What is the purpose of $C_I$?
   No important purpose.
Common Emitter Amplifier - Current Source Biasing

$I_{REF} = \frac{V_{CC} - V_{BE(Qref)}}{R_{ref}}$

$I_{REF} = \frac{V_{CC} + V_{EE} - V_{BE(Qref)}}{R_{ref}}$
Common Emitter Amplifier - Current Source Biasing

1. The current mirror sets $I_E (I_C)$.

2. $R_B$ serves the purpose to provide a high impedance looking into the base and $I_B = I_E / (\beta + 1)$ and $V_B = -I_B R_B$.

3. $V_B = 0.7V + V_E$ sets the emitter-to-ground voltage $V_E$ and, hence, sets $V_{CE}$ for a given $I_C$.

4. $v_s$ is the signal source.
Bias Setting

1. Since $R_B$ does not interfere with the bias, the signal source can “usually” be connected to the base without need for a blocking capacitor.

2. Choose $R_B$ “large” compared to $R_S$ to avoid attenuating $v_s$. But not too large!

3. Choose $R_{ref}$ to set $I_E$. 
Bias Setting - Continued

For dc bias set $v_s = 0$

Choose:

$\begin{align*}
I_C &\approx I_E \approx I_{\text{REF}} = 1 \text{ mA} \\
V_{CC} &= I_{\text{REF}} R_{\text{ref}} + V_{BE(\text{Qref})} - V_{EE} \\
I_{\text{REF}} &= \frac{V_{CC} + V_{EE} - 0.7}{R_{\text{ref}}} \\
R_{\text{ref}} &= \frac{23.3}{10^{-3}} = 23.3 \text{ k} \Omega \\
\end{align*}$

Choose standard size: (RCA Lab Comp List)

$R_{\text{ref}} = 22 \text{ k} \Omega$
Bias Setting - Completed

With the base $I_B \approx 0$ through $R_B$:

$$V_E = V_{EB(Qamp)} \approx -0.7V$$

$$V_{CC} = V_{RC} + V_{CE(Qamp)} + V_E$$

This implies that there is about an 12.7 V drop to split across $R_C$ & $V_{CE}$.

Let's choose $V = 5.6V$ & $V = 7.1V$.

$$R_C = \frac{V_{RC}}{I_C} = \frac{5.6}{10^{-3}} = 5.6k\Omega$$

Choose standard size: $R_C = 5.6k\Omega$

(RCA Lab Comp List)
Gain Setting

1. Connect the source to the base.

2. Provide a path for the small signal emitter current.

3. Choose $R_E$ for the desired gain $(A_v = -\frac{R_C}{R_E})$.

4. $C_E$ is nearly a short circuit for $f \geq f_{\text{min}}$

Calculate $C_E$ s.t. $\left| \frac{1}{j2\pi f C_E} \right| \ll R_E$ at $f \geq f_{\text{min}}$. 
Gain Setting - Continued

Design for $|A_V| = 20$:

Choose the nearest standard size resistors for $R_C$ and $R_E$.

$$R_E = \frac{R_C}{20} = \frac{5600}{20} \approx 270 \, \Omega$$

Gain check:

$$i_b = \frac{v_s}{R_S + (\beta + 1)(r_e + R_E)}$$

$$v_o = -R_C i_c = -R_C \beta i_b$$

$$|A_V| = \left| \frac{v_o}{v_s} \right| \approx \frac{\beta}{\beta + 1} \frac{R_C}{r_e + R_E} \approx \frac{5600}{295} = 19 \text{ or } 25.57 \, \text{dB}$$
\[ R_E \text{ and } C_E \]

\[ \left| \frac{1}{j 2 \pi f C_E} \right| \ll R_E \Rightarrow \frac{1}{2 \pi f_{\text{min}} C_E} = \frac{R_E}{10} \Rightarrow C_E = \frac{10}{2 \pi f_{\text{min}} R_E} \approx 300 \mu F \quad @ f_{\text{min}} = 20 \text{ Hz} \]

\[ C_E = 300 \mu F \text{ too large; too conservative!} \]
Complete the Design

\[
\left| \frac{1}{j 2 \pi f C_E} \right| \ll R_E \Rightarrow \frac{1}{2 \pi f_{\text{min}} C_E} = \frac{R_E}{10} \Rightarrow C_E = \frac{10}{2 \pi f_{\text{min}} R_E} \approx 300 \, \mu F \quad @ f_{\text{min}} = 20 \, \text{Hz}
\]

\[C_E = 300 \, \mu F \text{ too large!!}\]

Less Conservative Design:

\[C_E = \frac{1}{2 \pi f_{\text{low}} R_E}\]

where \( f_{\text{low}} \approx f_{\text{low} - 3dB} \)

\[C_E = \frac{1}{2 \pi f_{\text{low}} R_E} \approx 30 \, \mu F \quad \text{for} \quad f_{\text{low}} = 20 \, \text{Hz}
\]

If we choose next largest standard size (RCA Lab Comp List):

\[C_E = 33 \, \mu F \quad \Rightarrow \quad f_{\text{low}} = 12.5 \, \text{Hz}\]
$C_E = 33 \, \mu F$

20 Hz Gain  \hspace{1cm} \text{Actual } |A_V(f = 20.5 \, Hz)| = 22.63 \, dB

1 kHz Gain  \hspace{1cm} \text{Actual } |A_V(f = 1 \, kHz)| = 25.52 \, dB (18.88)

Spec. \hspace{1cm} 18 \leq |A_V| \geq 22
What if $R_E = 0 \, \Omega$?

Due to $C_E$:

$A_v = \frac{v_o}{v_s} \approx \frac{-R_C}{r_e}$

small ac @ midband

dc
What About Interface to the Output Load ($R_L$)?

Is the above interface to $R_L$ OK?
What About Interface to the Output Load ($R_L$)?

Is the above interface to $R_L$ OK? - No

1. Need $C_L$ to block dc bias on $v_C$, i.e. $v_o$ is small signal only.
2. For ac ($f \geq f_{min}$) $R'_L = R_C || R_L$ Unless $R_L >> R_C$, $R_L$ alters $A_v$. 

Kenneth R. Laker, update 15Oct13 KRL
Multi-Stage Amplifier

Stage 1

Stage 2

\[ A_v = \left( \frac{v_{o1}}{v_s} \right) \left( \frac{v_{o2}}{v_{o1}} \right) = \frac{v_{o2}}{v_s} = \left( - \frac{R_{C1}}{R_E} \right) \left( - \frac{R_{C2}}{R_E} \right) \]