Common Base BJT Amplifier

Common Collector BJT Amplifier

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Basic Single BJT Amplifier Features

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CE BJT amplifier => CS MOS amplifier
CC BJT amplifier => CD MOS amplifier
CB BJT amplifier => CG MOS amplifier
Common Collector (Emitter Follower) Amplifier

In the emitter follower, the output voltage is taken between emitter and ground. The voltage gain of this amplifier is nearly one – the output “follows” the input - hence the name: emitter “follower.”
**DC Bias**

\[
V_{cc} / 2 = \frac{R_B}{R_1 + R_2}
\]

\[
R_B = R_1 \parallel R_2
\]

\[
V_{in} = V_B
\]

\[
i_C = \frac{v_O}{R_E}
\]

\[
r = \frac{50 \text{ k Ohm}}{5.1 \text{ k Ohm}}
\]
Follower Small Signal Analysis - Voltage Gain

Circuit analysis:

\[ v_s = (R_s + r_\pi) i_b + R_E i_e = (R_s + r_\pi + (\beta + 1) R_E) i_b \]

Solving for \( i_b \):

\[ i_b = \frac{v_s}{R_s + r_\pi + (\beta + 1) R_E} \]

\[ v_o = R_E i_e = R_E (1 + \beta) i_b \]

for Current Bias Design

replace \( R_E \) with \( r_o \parallel r_o = r_o / 2 >> R_E \)

\[ A_V = \frac{v_o}{v_s} = \frac{R_E \parallel r_o}{R_s + r_\pi + (\beta + 1) R_E} \approx 1 \]
Small Signal Analysis – Voltage Gain - cont.

\[
\frac{v_o}{v_s} = \frac{R_E}{R_s + r_\pi + R_E}
\]

Since, typically:

\[
\frac{R_s + r_\pi}{(\beta + 1)} \ll R_E \quad (\text{or } r_o || r_o = r_o/2)
\]

\[
A_V = \frac{v_o}{v_s} \approx \frac{R_E}{R_E} = 1
\]

Note: \(A_V\) is non-inverting.
Of What value is a Unity Gain Amplifier?

**CC Amplifier**
- Voltage Gain ($A_v$)  low (about 1)
- Current Gain ($A_i$)  High ($\beta + I$)
- Input Resistance  high ($R_B || \beta R_E$)
- Output Resistance  low ($r_e$)  

VCVS  Or Buffer
Emitter Follower Small Sig. Output Resistance

\[ i_x = -i_e = -(1 + \beta) i_b \Rightarrow i_b = \frac{-i_x}{1 + \beta} \]

\[ v_x = -i_b (R_s + r_{\pi}) = \frac{R_s + r_{\pi}}{1 + \beta} i_x \quad \text{where} \quad r_{\pi} \gg R_s \]

\[ R_{\text{out}} = \frac{v_x}{i_x} = \frac{R_s + r_{\pi}}{1 + \beta} \approx \frac{r_{\pi}}{1 + \beta} = r_e \approx \frac{1}{g_m} = \frac{V_T}{I_C} \]

Assume:

\[ I_C = 1 mA \Rightarrow r_{\pi} = \frac{V_T}{I_B} = \beta \frac{V_T}{I_C} = 2500 \Omega \]

\[ \beta = 100 \quad R_s = 50 \Omega \]

Recall \[ R_{\text{in}} = r_{bg} = r_{\pi} + (\beta + 1) R_E \]

\[ R_{\text{out}} \approx r_e = \frac{2550}{100} = 25.5 \Omega \]
Multisim Verification of $R_{\text{out}}$

Thevenin equivalent for the short-circuited emitter follower.

If $\beta = 200$, as for most good NPN transistors, $R_{\text{out}}$ would be lower - close to $12 \ \Omega$.

Multisim short circuit check ($\beta = 100$, $v_s = v_{oc}$):

\[
R_{\text{out}} = \frac{v_{oc}}{i_{sc}} = \frac{v_{s(rms)}}{i_{sc(rms)}} = \frac{1 \text{ V}}{39.61 \text{ mA}} = 22.25 \ \Omega
\]
Emitter Follower Power Gain

Consider the case where a $R_L = 50$ Ω load is connected through an infinite capacitor to the emitter of the follower. Using its Thevenin equivalent:

\[
\begin{align*}
\nu_o &= \frac{R_L \parallel R_E}{R_L \parallel R_E + R_{out}} \cdot \frac{A_v \nu_s}{75} = \frac{50}{75} \nu_s = \frac{2}{3} \nu_s \\
i_o &= \frac{A_v \nu_s}{R_{out} + R_L \parallel R_E} = \frac{\nu_s}{75} \\
p_o &= \nu_o i_o = \frac{2}{225} \nu_s^2
\end{align*}
\]

@ midband where $A_v = 1$

\[
\begin{align*}
i_s &= i_b = \frac{\nu_s}{R_{in}} \approx \frac{\nu_s}{(\beta + 1) R_L \parallel R_E} \approx \frac{\nu_s}{101 \cdot 50} \approx \frac{\nu_s}{5000} \\
R_E \parallel R_L &= 5.1 \, k \, \Omega \parallel 50 \, \Omega \approx 50 \, \Omega \\
p_s &= \nu_s i_s \approx \frac{1}{5000} \nu_s^2 \\
A_{pwr} &= \frac{p_o}{p_s} = \frac{2(5000)}{225} = 44.4 \gg 1
\end{align*}
\]
Then, choose/specified $I_E$, and the rest of the design follows:

$$R_E = \frac{V_E}{I_E} = \frac{V_{CC} / 2 - 0.7}{I_E}$$

For a specified $\beta = 100$

As with CE bias design, stable op. pt.

$$\Rightarrow \quad R_B \ll (\beta + 1) R_E \quad \text{i.e.}$$

$$R_B = R_1 || R_2 = \frac{R_1}{2} = \frac{(\beta + 1)}{10} R_E \approx 10 R_E$$

$$R_1 = R_2 = 20 R_E$$

Split bias voltage drops about equally across the transistor $V_{CE}$ (or $V_{CB}$) and $V_{Re}$ (or $V_B$).

For simplicity, choose:

$$V_B = \frac{V_{CC}}{2} \Rightarrow R_1 = R_2$$
Typical Design - Cont.

Given: \( R_{\text{out}} = r_e = 25 \ \Omega \)
\( V_{CC} = 12 \ V \)

And the rest of the design follows:

\[ I_E \approx I_C = \frac{V_T}{r_e} = 1 \ mA \]

\[ R_E = \frac{V_E}{I_E} = \frac{12/2 - 0.7}{10^{-3}} = 5.3 \ k\Omega \]

Use standard sizes:

\[ R_E = 5.1 \ k\Omega \]
\[ R_1 = R_2 = 100 \ k\Omega \]
Use the base current expression:

\[ i_b = \frac{v_{bg}}{r_{\pi} + (\beta + 1) R_E} \]

This transistor input resistance \( r_{bg} \) is in parallel with \( R_B = 50 \, k\Omega \);

\[ v_{bg} = \frac{R_B}{R_B || r_{bg}} \cdot \frac{v_s}{v_{bg}} = \frac{1}{R_B || r_{bg} + R_s + \frac{1}{2 \pi f C_{in}}} \]

Ideally we want \( v_{bg} = v_s \) for \( f \geq f_{\min} \).
Choose $C_{in}$ such that its reactance is $\leq 1/10$ of $R_B$ at $f_{min}$:

$$\frac{1}{2\pi f C_{in}} = \frac{R_B}{10}$$

$$C_{in} \geq \frac{10}{2\pi f_{min} R_B}$$

Assume $f_{min} = 20$ Hz

with $R_B = 50 \text{ k}\Omega$

$$C_{in} \geq \frac{10}{2\pi \cdot 20 \cdot 50 \cdot 10^3} = 1.59 \mu F$$

Pick $C_{in} = 3.3 \mu F$, the nearest standard value in the Detkin Lab.

We could be (unnecessarily) more precise and include $r_{bg}$ and $R_s$ as part of the total resistance in the loop.
Final Design

\[ C_{in} = 3.3 \, \text{uF} \]

\[ R_S = 50 \, \text{Ohm} \]

\[ R_1 = 100 \, \text{kOhm} \]

\[ R_2 = 100 \, \text{kOhm} \]

\[ R_E = 5.1 \, \text{kOhm} \]

\[ V_{CC} = 12 \, \text{V} \]
**Multisim Simulation Results**

**20.74 Hz Data**  \[ A_v = 0.989 \]

**1 kHz Data**  \[ A_v = 0.995 \]
Quick Review

Voltage Gain ($A_V$)?

Current Gain ($A_I$)?

Input Resistance?

Output Resistance?
Quick Review

CC Amplifier
- Voltage Gain \( (A_v) \) low (about 1)
- Current Gain \( (A_i) \) high \((\beta + 1)\)
- Input Resistance high \((r_\pi + \beta R_E)\)
- Output Resistance low \(r_e\)

VCVS
Or Buffer
The Common Base Amplifier

### Voltage Bias Design

![Voltage Bias Design Diagram]

### Current Bias Design

![Current Bias Design Diagram]
Common Base Configuration

Both voltage and current biasing follow the same rules as those applied to the common emitter amplifier.

Insert a blocking capacitor in the input signal path to avoid disturbing the dc bias.

The common base amplifier uses a bypass capacitor – or a direct connection from base to ground to hold the base at ground for the signal only!

RECALL: The common emitter amplifier (except for $R_E$ feedback) holds the emitter at signal ground, while the common collector circuit does the same for the collector.
We keep the same bias (1/3, 1/3, 1/3) that we established for the gain of 10 common emitter amplifier.

All that we need to do is pick the capacitor values and calculate the circuit gain.
Mid-band Small Signal Analysis

For mid-band let $C_b = C_{in} = \infty$

\[ Z_{in} = \frac{v_{Re}}{i_s} = r_e \parallel R_E \approx r_e = \frac{V_T}{I_C} \]

Current Gain

\[ A_i = \frac{i_c}{i_e} = \alpha \approx 1 \]

Voltage Gain

\[ v_o = -R_C i_c = -\alpha R_C i_e = \frac{1}{\alpha} \frac{R_C}{R_S + r_e \parallel R_E} v_s \]

\[ A_v = \frac{v_o}{v_s} = \frac{1}{\alpha} \frac{R_C}{R_S + r_e} \] (non-inverting)

Note: $i_s = -i_e$

\[ R_E \gg r_e \]

\[ Z_{in} = \infty \]

\[ R_B \text{ is shorted by } C_b = \infty \]
**Common Base Small Signal Analysis -** $C_{in}$

**Diagram:**

- $i_b$ (base current)
- $v_o$ (output voltage)
- $R_C$ (4.7 k Ohm)
- $R_s$ (50 Ohm)
- $C_{in}$
- $R_E$ (470 Ohm)
- $v_{Re}$ (referred input voltage)
- $v_s$ (input voltage)
- $r_e$ (emitter resistance)

**NOTE:** $C_b$ is short ckt

**Determine $C_{in}$:** (let $C_b = \infty$)

\[
\frac{v_{Re}}{v_s} = \frac{R_E \parallel r_e}{R_E \parallel r_e + R_s + \frac{1}{j2\pi f C_{in}}} \approx \frac{r_e}{r_e + R_s} v_s
\]

**Ideally**

\[
\frac{v_{Re}}{v_s} = \frac{R_E \parallel r_e}{R_E \parallel r_e + R_s + \frac{1}{j2\pi f C_{in}}} \approx \frac{r_e}{r_e + R_s} v_s
\]

for $f \geq f_{min}$

\[
1 = \frac{1}{2\pi f_{min} C_{in}} \Rightarrow 1 = \frac{1}{2\pi f_{min} C_{in}} \Rightarrow \frac{1}{2\pi f_{min} C_{in}} \Rightarrow C_{in} = \frac{10}{2\pi f_{min}(R_s + r_e)}
\]

**Equations:**

- $C_{in} = 10 / (2\pi f_{min}(R_s + r_e))$
Determine $C_{\text{IN}}$ cont.

A suitable value for $C_{\text{IN}}$ for a $20 \text{ Hz} f_{\text{min}}$ with $r_e = 25 \Omega$ and $R_s = 50 \Omega$:

$$2\pi f_{\text{min}} C_{\text{IN}}(R_s + r_e) \gg 1 \Rightarrow C_{\text{IN}} \geq \frac{10}{2\pi f_{\text{min}}(R_s + r_e)} = \frac{10}{2\pi 20 \cdot 75} F$$

\[
C_{\text{IN}} = \frac{10}{125.6 \cdot 75} \approx 1061 \mu F
\]

TOO LARGE; NOT PRACTICAL

Choose $C_{\text{IN}} = 220 \mu F$ (largest standard value in Detkin Lab)

$$X_{C_{\text{IN}}} = \frac{1}{2\pi f_{\text{min}} C_{\text{IN}}} \approx 36 \Omega$$
Small-signal Analysis - $C_b$

Determine $C_b$ : (let $C_{in} = \infty$)

\[
\begin{align*}
\nu_{Re} &= \frac{R_E \parallel (r_e + \frac{1}{j 2 \pi f C_b (\beta + 1)})}{R_E \parallel (r_e + \frac{1}{j 2 \pi f C_b (\beta + 1)}) + R_S} \nu_s \\
\text{ideally} \quad \nu_{Re} &= \frac{R_E \parallel r_e}{R_E \parallel r_e + R_S} \nu_s \quad \text{for} \quad f \geq f_{\text{min}}
\end{align*}
\]

\[
\frac{1}{2 \pi f_{\text{min}} C_b (\beta + 1)} \ll r_e \Rightarrow \frac{1}{2 \pi f_{\text{min}} C_b (\beta + 1)} = \frac{r_e}{10} \Rightarrow C_b = \frac{10}{2 \pi f_{\text{min}} r_e (\beta + 1)}
\]
Determine - \( C_B \) cont.

Choose (conservatively):

\[
C_b = \frac{10}{2\pi f_{\text{min}}((\beta + 1)r_e)} F
\]

for \( f_{\text{min}} = 20 \text{ Hz} \)

i.e.

\[
C_b = \frac{10}{2\pi 20((100)(25))} = 31.8 \mu F
\]
Multisim Simulation

\[ A_v = \frac{v_o}{v_s} = \frac{1}{\alpha} \frac{R_C}{R_s + r_e} \approx \frac{R_C}{R_s + r_e} = \frac{4700}{50 + 25} = 62.7 \]
Multisim Frequency Response

19.3 Hz response \( A_{v(sim)} = 61.8 \)

1 kHz Response \( A_{v(sim)} = 63.3 > A_{v(theory)} = 62.7 \)

vertical axis is a linear scale

\( \delta < 1\% \)