1. Two phase clock generator: Build and simulate in SPICE the two-phase clock generator shown below. Drive it with a 100MHz square wave (VPULSE).

   (a) include plot of SPICE simulation in writeup
   (b) explain the operation of the circuit
   (c) explain how you can modify the circuit to adjust the non-overlap period

   (You will use this for problem 4 and likely need it for Project 2.)

2. Gate-based latch: Build and simulate in SPICE a gate-based latch.

   (a) Explain operation
   (b) Characterize in SPICE; in writeup describe how the delays are related to the circuit.
      i. the setup time – how long before \( \phi \) transitions from 1→0 must the input arrive in order for it to be held on the output once \( \phi \) is 0?
      ii. hold time – how long after \( \phi \) transitions from 1→0 must the input remain stable in order for it to be held on the output once \( \phi \) is 0?
      iii. clk→q delay for the latch – how long after \( \phi \) transitions from 0→1 before the input will be seen on the output (load with another latch for clk→q measurement)

   Answers should be for worst-case data values (transitions).
3. Pass transistors-based register: Build, size, and simulate in SPICE a register based on a pass transistor-based latch:

(a) Explain how it works
(b) Size transistors so that the design will work
(c) Identify the benefits and limitations of this design
(d) Compare this register to a master-slave register built from two of the gate-based latches from the previous problem (total area (transistor width), setup time, hold time, clk→q delay (load with another one of these registers for comparison measurement), load on clock)

4. Explore Register Operation

(a) Using your pass transistor register from the previous problem, connect a 4 element long shift register and demonstrate proper operation on the input sequence: (first) 0 1 0 0 1 1 0 0 0 0 (last). (You may want to use a SPICE VPWL to supply the input.) [include schematic and waveform(s) demonstrating correct operation in turnin]
(b) Connect your register from (a) with a chain of three inverters so that the output of the register toggles on every clock cycle.
   i. How fast can you clock this design before it fails? (use SPICE to search for the frequency where the register just fails)
   ii. Explain what happens when it does fail.
   iii. At the highest frequency for correct operation, show how the clock cycle breaks down into clk→q delay, logic propagation delay through the inverter chain, and setup time before the clock. Show waveforms from SPICE simulation, mark where transitions occur, and report the associated delays.
VPWL is one of the SPICE circuit elements you can insert in your Electric schematic. You control its behavior with the PWL string, which you can specify in Electric. The string is defined in Section 4.1.4 in the ngspice26 manual. It is a list of time voltage pairs. The signals is ramped linearly between the voltage at successive time points. The specification:

- 0ns 0 1ns 0 2ns 0.8 4ns 0.8 5ns 0 10ns 0.1 15ns 0.4 18ns 0.4 19ns 0.8 24ns 0.8 24.01ns 0 30ns 0

defines the following waveform: