Due: Thursday, December 4, 10:00PM

1. “Inductive Noise and Crosstalk” Lab (Monday Nov. 17, 2014) summary and post-lab questions:
   
   (a) Summarize raw data collected
   
   (b) Working individually, describe your observations (each answer should be 2–3 sentences; most answers must be qualitative, but one or two of these might benefit from an equation connected to the material covered in the lectures following the lab).
      
      i. Impact of bypass capacitors?
      ii. Impact of crosstalk on driven vs. undriven signals?
      iii. Level of crosstalk on ribbon cable versus PCB?
      iv. Impact of conductor shielding (intermediate (B) grounded wire) on ribbon cable signal crosstalk?
      v. Impact of adjacent wire length on signal crosstalk?

   The observations and insight should come out of your team data collection and discussion. Nonetheless, this writeup should be done independently and expressed in your individual words.
2. Simulate crosstalk between on-chip wires:
   Assume:
   • Wire capacitance of 2pF/cm (assume this is to substrate/ground)
   • Metal Aspect ratio (height/width): 1.8
   • Metal width: 32nm
   • Metal spacing: 32nm
   • Approximate wire-to-wire adjacent capacitance as parallel plate with effective
dielectric constant \( \epsilon = 4 \times 10^{-13} \text{F/cm} \)
   • Buffer is \( W_n = 5, W_p = 5 \)
   • You may use lumped wire capacitances for this problem.

(a) What is the capacitance between adjacent wires that run in parallel for 100µm?
(b) Just based on the wire-to-ground and wire-to-wire capacitance, what is the maximum percentage of noise one wire can induce on an adjacent wire?
(c) Place a driver and receiving buffer at each end of the two lines (both wires driven same direction, so drivers on the same end of each line). Simulate (SPICE) this arrangement. Switch one line while the other is driven low.
   i. What is the delay for the switched line to drive the input to the receiving buffer?
   ii. Identify the level of noise induced on the non-switching line.
   iii. Include the SPICE plot.
(d) Simulate just the single line in isolation and identify the delay to drive a buffer on the far end of the line.
(e) Returning to the adjacent wire arrangement, simulate the two wires switching simultaneously in opposite directions.
   i. What is the delay for the switched line to drive the input to the receiving buffer?
   ii. Include the SPICE plot.

Plot the 3 transition cases above (c, d, e) on a single graph to directly compare the impact of capacitive coupling and simultaneous switching on delay.
3. Simulate Off Chip I/O Signalling: Consider the following I/O pin and board model signalling between two chips.

![Diagram of I/O pin and board model signalling between two chips]

<table>
<thead>
<tr>
<th>$L_{pin}$</th>
<th>$C_{pin}$</th>
<th>$R_{pin}$</th>
<th>$C_{wire}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nH</td>
<td>1pF</td>
<td>0.3Ω</td>
<td>3pF</td>
</tr>
</tbody>
</table>

To roughly model the fact that you will have $N$ output drivers per power/ground pair (e.g. in the 74X04 example used in Lab 2, you had $N = 6$ outputs sharing a single I/O pair):

- $L_{ppin} = N \times L_{pin}$, $R_{ppin} = N \times R_{pin}$, $C_{ppin} = \frac{C_{pin}}{N}$

The current per pin is actually larger ($I_{shared} = N \times I_{single}$). But you want to just simulate one pin, so this pushes that factor into the power/ground pin L, R, C parameters to model the effect.

(a) Using SPICE and the 22nm PTM model, size inverter 1 to minimize the delay from A to a settled value at D for $N = 6$.

- Only consider D settled when it stays within $1/4 \ V_{dd}$ of its final value (i.e. below $1/4 \ V_{dd}$ or above $3/4 \ V_{dd}$).

(b) Can you make the inverter too large? why?

(c) Can you make the inverter too small? why?

(d) At your selected inverter size, what fraction of the delay is associated with: (i) wire rise time, (ii) settling; include an annotated SPICE transient simulation plot showing these times on your simulation.
4. “Transmission Line” Lab (Friday, Nov. 21nd) summary and post-lab calculations:

(a) Provide a summary of your answers to in-lab questions.

(b) Working individually, answer the following questions:

   i. Using the result from in-lab-2(b), what is the propagation speed of signals along the coaxial cable?

   ii. What does in-lab-3(a) tell you about the impedance of the coaxial cable?

   iii. Use the reflection equation to explain the resistance found in in-lab-3(d).

       [If you were unable to achieve the one-half magnitude positive reflection, explain the maximum magnitude reflection you were able to observe and why it was not possible to achieve the one-half magnitude reflection with the potentiometer you were given.]

   iv. Use reflection equations and transmission line behavior to explain your observations for in-lab-6(a).

       Note: You should have the building blocks to do this after lecture on Monday. However, we won’t do an example in class like it until Wednesday lecture.
5. Communication over a distance.

For this problem, you want to send a signal across 1 cm of an integrated circuit chip.

- 22nm Low Standby Power Process (LP)
- $\gamma = 1$
- $V_{dd} = 630$ mV
- nominal $V_{thn} = -V_{thp} = 410$ mV
- $C_0 = 1.2 \times 10^{-17}$ F (for $W = 1$ device)
- $I_{d, sat} = 12 \mu A$ (for $W = 1$ device)
- $R_{wire} = 700$ K$\Omega$/cm
- $C_{wire} = 1.7$ pF/cm

(a) What is $R_0$ and $\tau$ for this technology?

(b) What is the delay to send a bit from one end of the wire to the other on an unbuffered wire driven by a minimum size ($W = 1$) inverter?

(c) If you buffered the wire with a $W_{buf} = 70$ every $L_{seg} = 0.02$ mm and try to drive the wire with minimum delay, what is the delay to send a bit from one end of the wire to the other, starting from a minimum size inverter as the input? Describe all the buffers you add to drive the wire and their size and placement.

(d) Consider transmitting the bit for the 1 cm distance by sending it off chip through a $Z = 50\Omega$ transmission line on a PCB with $\epsilon_r = 4$, $\mu_r = 1$. Your design should include the circuitry for driving and terminating the transmission line with minimum delay starting from a minimum size inverter (describe your circuitry as part of your answer). What is the delay to send a bit from this inverter, through the output driver, across 1 cm on the PCB, through a receiver back onto the IC, including any settling time necessary? (you do not need to worry about package inductance for this problem.)

(e) What is the energy per bit transmitted for each of the three scenarios. For the transmission line scenario, assume the pulse width is equal to the delay calculated.