ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Day 26: October 31, 2014
Synchronous Circuits

Today

• Managing Timing
• Reusing Circuits
• Latches
• Registers, clocking

Preclass 1, 2

• Worst-case delay to output?
• Shortest delay to output?

Preclass 3

• New set of inputs every 20T_
  – How does it behave?

Preclass 3

• When does Carry In reach bit 17 of final adder?
• After insertion of new input at 20T_
  how early can A or B input to final adder change?

Challenge

• Logic paths have different delays
  – E.g. different output bits in an adder
• Delay of signal data dependent
  – E.g. length of carry
• Delay is chip dependent
  – E.g. Threshold Variation
• Delay is environment dependent
  – E.g. Temperature
**Challenge**
- Logic paths have different delays
- Delay of signal data dependent
- Delay is chip dependent
- Delay is environment dependent
- Proper behavior depends on inputs being coordinated
  - Match the inputs that should interact

**Logic Reuse**
- How do we fix this?
  - Make it possible to input a new value every $20T_{\text{lat}}$?

**Discipline**
- Add circuit elements to
  - hold values
  - and change at coordinated point
    - Control when changes seen by circuit
- Only have to make sure to **wait long enough** for all results
- Decouple
  - timing of signal change
  - from timing of signal usage

**Latch**
- $\phi=1 \Rightarrow \text{Out}=/\text{In}$
- $\phi=0 \Rightarrow \text{Out}=$Out
- $\phi$ transitions $0\rightarrow1$ Out holds value
- How would a latch help us here?

**Synchronous Discipline**
- Add state elements (registers, latches)
- Compute
  - From state elements
  - Through combinational logic
  - To new values for state elements

**Midterm 2 Topics**
- Sizing
- Tau-model
  - Estimation and optimization
- Elmore-delay
  - Estimation and optimization
- Energy and power
  - Estimation and optimization
  - Dynamic and static
- Logic
  - CMOS
  - Ratioed
  - Pass transistor
- Regions of operation
- Scaling
- Noise Margins and restoration
- **No clocking**
  - Except to motivate delay targets and power calculations
Latch

- \( \phi = 1 \rightarrow \text{Out} = \neg \text{In} \)
- \( \phi = 0 \rightarrow \text{Out} = \text{Out} \)
- \( \phi \) transitions 1\( \rightarrow \)0 Out holds value

- How build latch from CMOS logic?

Latch from Combinational Logic

- \( \phi = 1 \rightarrow \text{Out} = \neg \text{In} \)
- \( \phi = 0 \rightarrow \text{Out} = \text{Out} \)
- \( \phi \) transitions 1\( \rightarrow \)0

What is the difference?

- How build latch from pass transistors?
  - (short hold)

MuxL Level Restorer ("Staticizer")

Without level restorer
With level restorer

Level Restore

• What issue arises here?

Latch with Level Restore

Latch

• \( \phi = 1 \Rightarrow \) Out=/In
• \( \phi = 0 \Rightarrow \) Out=Out
• \( \phi \) transitions 1\( \rightarrow \)0 Out holds value

• How build latch from pass transistors?
  – (long hold)

Static Latch

Typical Static Latch

Advantages:
• Static
• Full Rail
• Fast

Isolation inverters:
• Input Cap
• Input/Output Noise
• State Node Noise
Latch Timing Issues

- What timing constraints do latches impose?
  - When can $\phi$ change?
  - How long must $\phi$ be high?
  - Delay when $\phi$ is high?

Shift Register

- How do you make a shift register out of latches?

Two Phase Non-Overlapping Clocks

- What happens when $\phi_0$ is high?
- What happens when $\phi_1$ is high?

Two Phase Non-Overlapping Clocks

- When does the action happen?

Two Phase Non-Overlapping Clocks

- What could go wrong if the overlap?
Two Phase Non-Overlapping Clocks

- What timing constraints do we have?

Clocking Discipline

- Follow discipline of combinational logic broken by registers
- Compute
  - From state elements
  - Through combinational logic
  - To new values for state elements
- As long as clock cycle long enough,
  - Will get correct behavior

Ideas

- Synchronize circuits
  - to external events
  - disciplined reuse of circuitry
- Leads to clocked circuit discipline
  - Uses state holding element
  - Prevents
    - Combinational loops
    - Timing assumptions
    - (More) complex reasoning about all possible timings

Admin

- Exam Monday
  - No class at noon – office hour
  - Exam 7—9pm in Towne 309
- Daylight savings time ends Sunday 2am
  - Get an extra hour to study for exam!
    • (or catchup on sleep)
- Review Sunday Ketterer
  - (make sure you account for time change!)