Today

- 5T/6T SRAM
  - Writing
  - Charge sharing
  - Precharge
- DRAM

Memory Core: Part 1

- 5T SRAM
  - Writing
  - Charge sharing
  - Precharge

**Write (preclass 1)**

- Assuming properly select only one WL, what does write circuit look like?
  - What transistors are ON when writing a 0 over a cell that holds a 1?
  - Drive with inverter at BL
    - Width $W_{\text{write}}$
    - Voltage written?

**Write (preclass 1)**

- Assuming properly select only one WL, what does write circuit look like?
  - Voltage written?

\[
\frac{R_{\text{access}} + R_{\text{write}}}{R_{\text{access}} + R_{\text{write}} + R_{\text{buf}}} = \frac{1}{W_{\text{access}}} + \frac{1}{W_{\text{write}}} + \frac{1}{W_{\text{buf}}}
\]
Write Conclude?

- Writing into cell is a ratioed operation.

\[
\frac{1}{W_{\text{access}}} + \frac{1}{W_{\text{write}}} = \frac{1}{W_{\text{buffer}}} \]

Write (preclass 2)

- Assuming properly select only one WL, what does write circuit look like?
  - How different when writing a 1 over a cell holding a 0?

6T Cell

- How does 6T make it easier to perform writes?

Preclass 3

- Initially
  - A @ 1V
  - B @ 0V
- Close switch
- Voltage at A?

Consider (preclass 4)

- Read: What happens to voltage at A when WL turns from 0→1?
  - Assume \( W_{\text{access}} \) large
  - \( W_{\text{access}} >> W_{\text{pu}} = 1 \)
  - BL initially 0
  - A initially 1
Voltage After enable Word Line

- $Q_{BL} = 0$
- $Q_A = (1V)(\gamma(2+W_{access})C_0)$
- $C_{BL} >> C_A = (\gamma(2+W_{access})C_0)$
- After enable $W_{access}$ ($W_{access}$ large)
  - Total charge $Q_{BL} + Q_A$ roughly unchanged
  - Distributed over larger capacitance $\sim C_{BL}$
  - $V_A = V_{BL} \sim C_A/C_{BL}$

Larger Resistance?

- What happens if $W_{access}$ small?
  - $W_{access} < W_{pu}$
- Takes time to move charge from A to BL
- Moves more slowly than replenished by pu

Simulation: $W_{access} = 100$

Charge Sharing

- **Conclude**: charge sharing can pull down voltage
Consider

• What happens to voltage at A when WL turns from 0→1?
  – Assume \( W_{\text{access}} \) large

Simulation \( W_{\text{access}} = 20 \)

Charge Sharing

• Conclude: charge sharing can lead to read upset
  – Charge redistribution adequate to flip state

How might we avoid?

• Charge bitlines to \( V_{dd}/2 \) before begin read operation
  • Now charge sharing doesn’t swing to opposite side of midpoint
Pre-Charge

- Use one phase of clock to charge a node to some initial value before operation

Precharge Transistor Can be large

Compare

- Both $W_{access} = 20$; vary precharge

Simulation $W_{access} = 20$
(precharge Vdd/2, reading 0)

Simulation $W_{access} = 20$
(with precharge Vdd/2)

Pre-Charge

- Use one phase of clock to charge a node to some initial value before operation

Precharge Transistor Can be large
5T/6T SRAM Questions?

Idea

- Memory can be compact
- Demands careful sizing

Admin

- HW7 due tomorrow
- Project 2 out
  - Due 2 weeks from tomorrow
    - Tuesday before Thanksgiving