University of California at Berkeley
Department of Electrical Engineering and Computer Science
Reconfigurable Computing Seminar

CS294-7, Spring 1997 Tentative Lectures and Reading Tuesday, January 21

Intro:

1. **First Class/Motivation:** What's RC and Why is it interesting?
   - **Goal:** Give people an idea of what course is about and why its important.
   - **Reading:** The Case for Reconfigurable Processors
   - *other materials:* Course description, calendar, terminology
2. Computing requirements, VLSI Area, scaling, capacity
   - **Goal:** Start with fresh view of computing requirements and identify key pieces; put components in perspective for remainder of course; Provide background necessary to compare and evaluate computing technologies and to appreciate trends.
   - **Reading:** Chapter 14 and 15 of [DeH96], [DGY+74], [Boh95b], [Boh95a]
3. Instructions and GP architecture space
   - **Goal:** Understand impact of instruction organization on architecture; understand cost of instruction distribution and storage.
   - **Reading:** [DeH96] chapters 8-9
4. FPGA intro/tutorial (including FPGA tool sequence)
   - **Goal:** Make sure everyone understands what an FPGA looks like and how they are traditionally used and programmed.
   - **Reading:** [BR96] [Tri93]
   - **Additional Reading:** [Tri92]† [Bro95]
5. Dig into one or two CCMs (Perle-1, Cheops)
   - **Goal:** See everything involved in a CCM: arch, programming, performance, runtime, pains and limitations.
   - **Reading:** [VBR+96] [BW95]
   - **Additional Information:** PAM `<http://pam.devinci.fr/documentation.html>`, Cheops `<http://tvot.www.media.mit.edu/projects/TVOT/Agenda95-2/Cheops.html>`
6. Dig into an application (SPLASH sequence matching)

- **Goal:** See computing style, programming style, and results.
- **Reading:** [GHK$^+$91], [BAK96] chapter 8
- **Additional Information:** `<http://www.super.org:8000/FPGA/fpga.html>`, `<http://pequod.ee.vt.edu/>`

7. Comparing computing devices
   - **Goal:** Understand how various styles stack up, when they are used well and when they are not.
   - **Reading:** [DeH97]
   - **Additional Reading:** Chapters 4-6 of [DeH96], [ACC96], [ACC94a], [ACC94b], [MVBL96]†

Spatial Computing:

1. Systolic Architectures and Algorithms
   (traditional filter and matrix operations here)
   - **Goal:** Understand style and philosophy of systolic architectures.
   - **Reading:** [Kun82], [LM85]
   - **Additional Reading:** [JHS93]
2. Sampling of Systolic Structures
   - **Goal:** Familiarize everyone with a broader set of systolic solutions; after these two lectures, should be able to categorize related problems and design systolic solutions for them.
   - **Reading:** [Lei79], [KL79], [GKT79]
3. Cellular Automata
   - **Goal:** Understand style; see representative problems; appreciate class of problems and algorithms amenable to cellular solution.
   - **Reading:** [Min67]?, [RMA84]†, [RR87]
4. Bit Serial Processing
   - **Goal:** Understand style, mapping, area-time implications, and sample solutions.
   - **Reading:** TBD

Interconnect:

1. Interconnect (relative area, delay, capacity, growth, Rent, Sea-of-Gates)
   - **Goal:** Understand how interconnect requirements can be analyzed, how they scale, and their significance in reconfigurable architectures.

- **Reading:** [DeH96] Ch 7, [LR71], [Gam81], perhaps others

2. Traditional FPGA Interconnect (Xilinx, Altera, Brown+Rose, Lewis)
   - **Goal:** Become familiar with traditional interconnect styles used in FPGAs and relate structures to general metrics and goals.
   - **Reading:** collection of diagrams from Xilinx, Altera, [RB91], [AL94]
3. VLSI interconnect structures
   - **Goal:** Become familiar with typical building blocks at the silicon level and their tradeoffs.
   - **Reading:** [DHG95] and others....
4. Partitioning and Placement
   - **Goal:** Understand Routing problem and conventional solutions; relate mapping issues to interconnect architecture.
   - **Reading:** [KGV83], [FM82]
5. Routing
   - **Goal:** Understand Routing problem and conventional solutions; relate mapping issues to interconnect architecture.
   - **Reading:** global route - Locus [Ros90]†, detail route - [BLK96]

Compute:

1. Memory as a programmable element; LUTs+interconnect as an alternate to one big memory.
   - **Goal:** Understand how memory blocks may act as programmable elements, when they are efficient and inefficient, and how adding programmable interconnect helps in common cases.
   - **Reading:** assemble notes from Ch4 of [DeH96] and material written on TN#123, ([RFLC90] and [SRCL92]) or ch4 of [BFRV92]
2. LUT Mapping
   - **Goal:** Understand, basically, how LUT mapping is performed.
   - **Reading:** [BFRV92] 3.2.1-2, Flowmap [CD94a]† [CD94b]†
3. Alternatives to LUTs: ULMs, PLAs
   - **Goal:** Appreciate how ULMs relate to LUTs; Understand relative strengths and weaknesses of PLAs.
   - **Reading:** [KG92], A good ULM paper? (maybe [ZV96]), maybe [KB96]?
4. ALU bits, fast carry logic, and conventional CLBs (special case interconnect: (a) cascading LUTs, (b)segmentable/combinable LUTs)

- **Goal:** Understand how ALU bit-slices differ from pure LUTs and how conventional, commercial devices are a combination of the two.
- **Reading:** [Woo95]

Retiming:

1. Fine-grained retiming – heavy pipelining, delay minimization, c-slow
   - **Goal:** Understand the role of retiming to maximize throughput, and known algorithms for automating the task.
   - **Reading:** [LR93]
2. Coarse-grain – bit-serial, fifo, video stream; VLSI structures and costs for retiming (*e.g.* flip-flops, shift-registers, register files, fifos, SRAM, DRAM)
   - **Goal:** See how memory is used to perform retiming in various scenarios. Become familiar with the various VLSI structures used for retiming and when each is preferred.
3. Retiming as behavioral optimization (minimize function usage, memory intermediates)
   - **Goal:** Understand behavioral optimizations which reduce compute and memory requirements.
   - **Reading:** [Ben94] [PR90], [GFvS$^+$93]

Other:

1. Control (where data affects the instruction (operation performed) and/or istream) – FSMs
   - **Goal:** Understand role and integration of control in general-purpose architectures.
   - **Reading:** Sections 8.5 and 10.6 of [DeH96]
2. Binding time and specialization
   - **Goal:** Classify binding times and understand specialization opportunities and benefits.
   - **Reading:** [Cha93], [VSCZ96], [DeH95]?
3. Programming styles (single lecture overview)
   - **Goal:** Become exposed to various styles possible for programming reconfigurable devices.
4. Reuse/sharing

- **Goal:** Understand why we might want to share and reuse resources and the techniques for doing so.
- **Reading:** Excerpts from Chapter 10 of [DeH96], [VSCZ96], probably others...
- **Additional Reading:** [JOSV95], [WH95], [WH96], [EH94], [LSC96]

† – denotes references which look promising, but which André hasn't reviewed, yet.

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