CS294-7: Reconfigurable Computing

Day 13: Tuesday, March 4

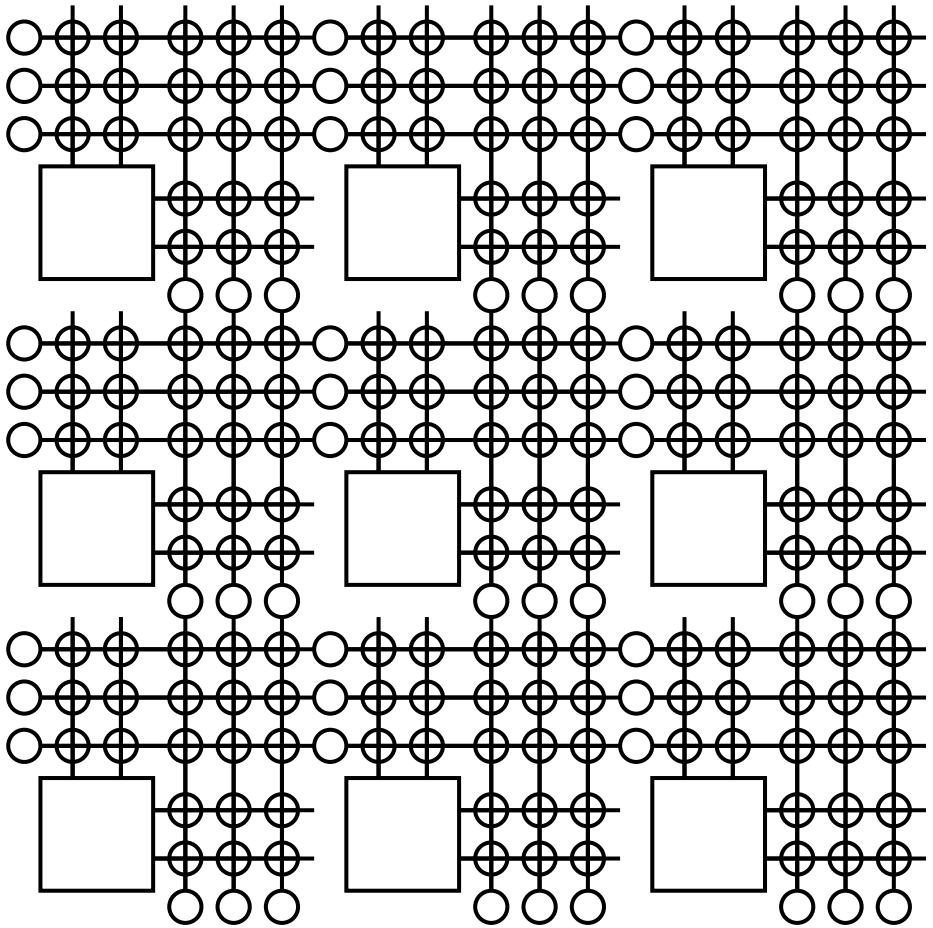
Interconnect

- Admin
- Traditional FPGA Interconnect

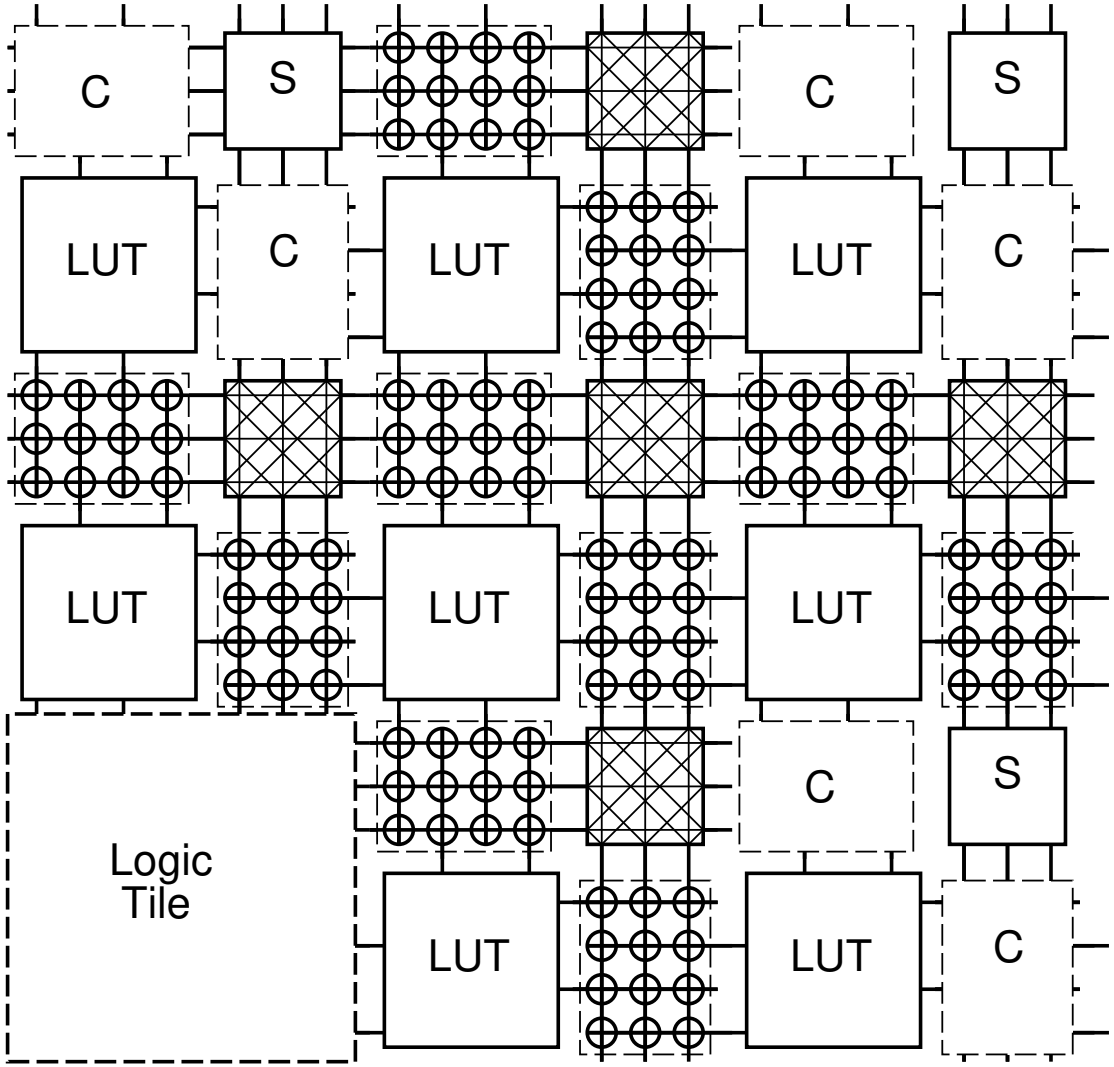
Admin

- Jason Cong – FPGA Mapping, Retiming, and Pipelining – W5pm, Hogan Room
- Project 1
  - Due Tuesday (3/11)
  - Netlist request

From Thursday

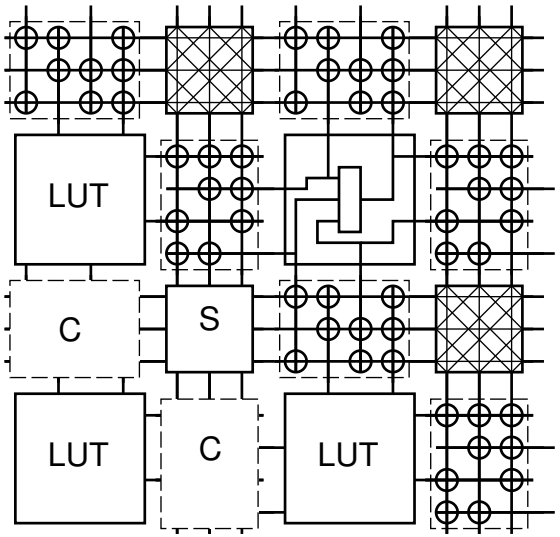


Toronto "Symmetric" FPGA Model



Parameterization

- T – number of sides on which a pin is available
- W – tracks / channel
- F_s – connections offered per incoming wire
- F_c – number of channel wires connected to each logic pin



Formulation

- Pack Logic blocks into minimal sized array
- Global routing tells us W
- Look for F_c and F_s which achieve good routability

Channel Width

Donath:

$$\overline{L} = \begin{cases} O(\log(N)) & p < 0.5 \\ O(N^{p-0.5}) & p > 0.5 \end{cases}$$

El Gamal:

$$W = \begin{cases} O(\log(N)) & \overline{L} \leq O(\log(N)) \\ O(\overline{L}) & \overline{L} > O(\log(N)) \end{cases}$$

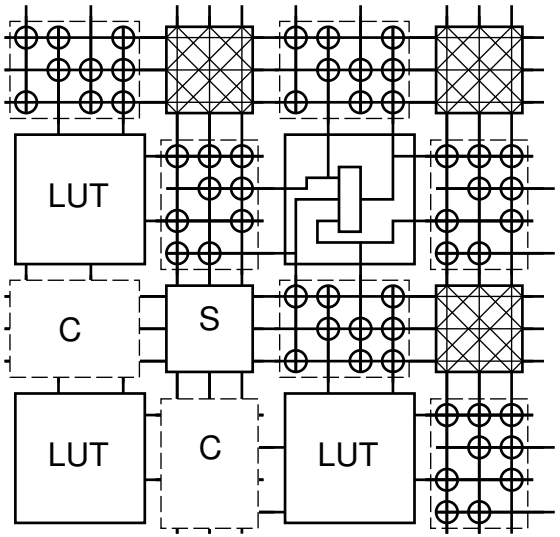
$$W = \begin{cases} O(\log(N)) & p < 0.5 \\ O(N^{p-0.5}) & p > 0.5 \end{cases}$$

Connection Sides

$T = 2$

Claims:

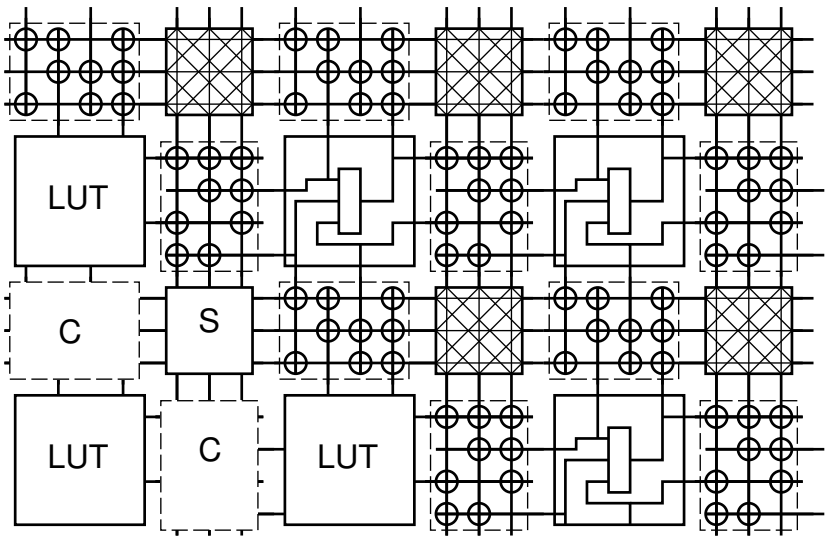
- $T = 2$ **less tracks than** $T = 1$
  (*n.b.* $2F_c$ input switches/logic inputs)
- $T > 2$ **diminishing returns**
- $T = 2$ **similar to LUT input permutability?**



What switches do we need?

Assume $F_C = W$:

- **which wire in channel irrelevant**
- **each input needs to connect to one of wires on each of the three adjacent channels**

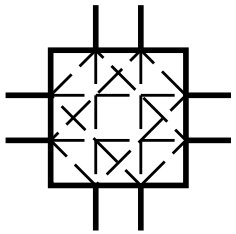


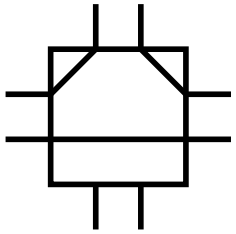
What switches do we need?

- *Universal* **switchbox can connect any set of inputs to their target output channels simultaneously**
- *Universal* **switchbox buildable with** $F_s = 3$ **(**$6W$ **switches)**
- **Xilinx switchbox is** $6W$ **switches but not universal**
- **Brown and Rose Anti-symmetric, close but also not universal**

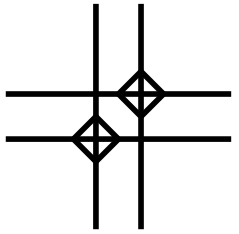
Universal Switch Box

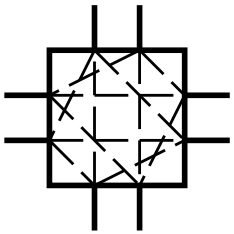
Universal





Xilinx





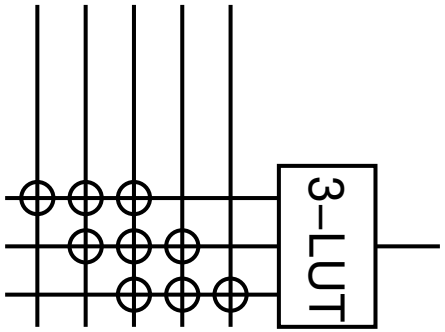
can't route
(or rotations)

Universal: Chang/Wong/Wong FPGA'96

Depopulating Input Connections

K-LUT – inputs equivalent

W choose $K \rightarrow$ only need $W - K + 1$ connections per input



$W \approx 10$, $K = 4 \rightarrow Fc = 7$

($F_c \approx 8$, fully populate output)

Guaranteed Routing Values

F_s = 3

F_c = $W - K + 1$ (inputs)

F_c = W (output)

Circuit Sizes Used

	N	connections	W
BUSC	109	392	11
DMA	224	771	12
BNRE	362	1257	14
DFSM	401	1422	13
Z03	586	2135	13

Brown and Rose Results (1)

Figure 6 from paper.

Brown and Rose Results (2)

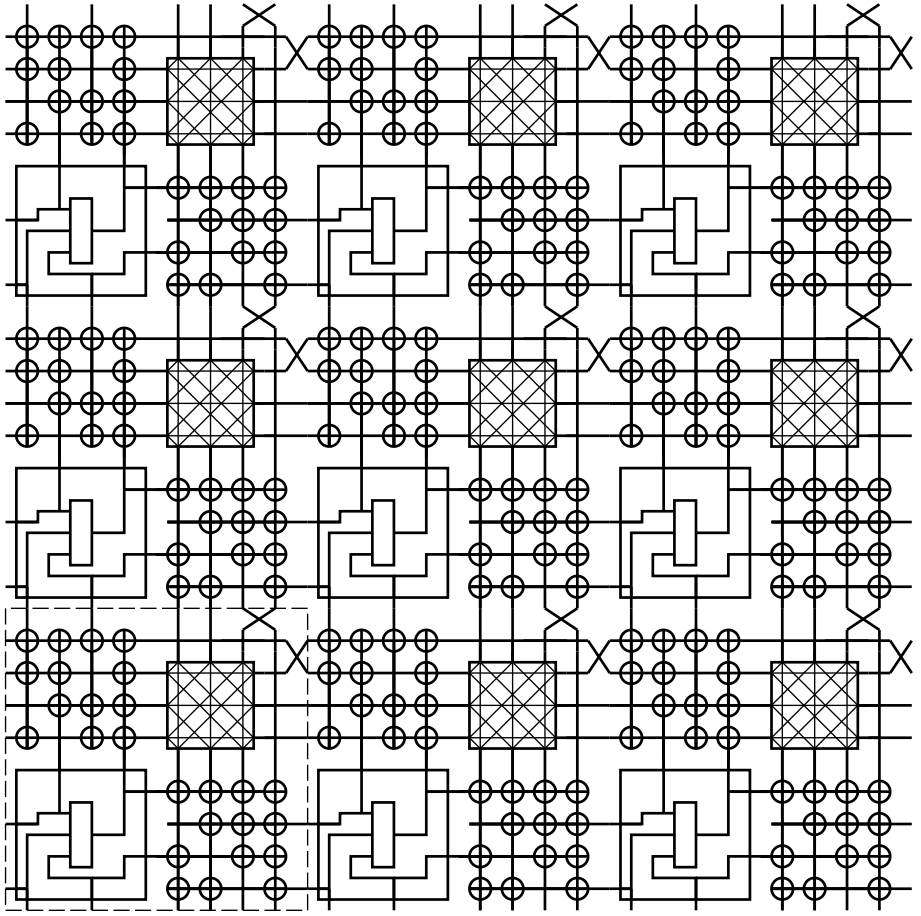
Figure 7 from paper.

Recommendations

- $3 \leq F_s \leq 4$
- $0.7 \leq F_c/W \leq 0.9$
- (commensurate with guaranteed values derived above)
- *N.B.* **not using** *Universal* **switch box topology**

Note: 231 switches/LUT, minimum configuration

Revise Model – Add Segments



Results

Claim:

- marginal/no benefit for 4+ length segments?

100	8.3										
90	8.4	8.2									
80	8.4	8.1	8.0								
70	8.6	8.3	8.0	7.9							
60	9.0	8.5	8.2	7.9	7.7						
50	9.5	8.9	8.4	7.9	7.7	7.6					
40	10.3	9.5	8.7	8.2	7.9	7.5	7.5				
30	11.1	10.1	9.4	8.7	8.2	7.7	7.5	7.4			
20	11.9	11.0	10.2	9.3	8.6	8.0	7.7	7.4	7.5		
10	12.4	11.7	10.9	10.1	9.2	8.3	7.9	7.6	7.4	7.5	
0	12.8	12.5	11.8	10.8	9.9	9.0	8.4	7.9	7.5	7.4	7.5
	0	10	20	30	40	50	60	70	80	90	100

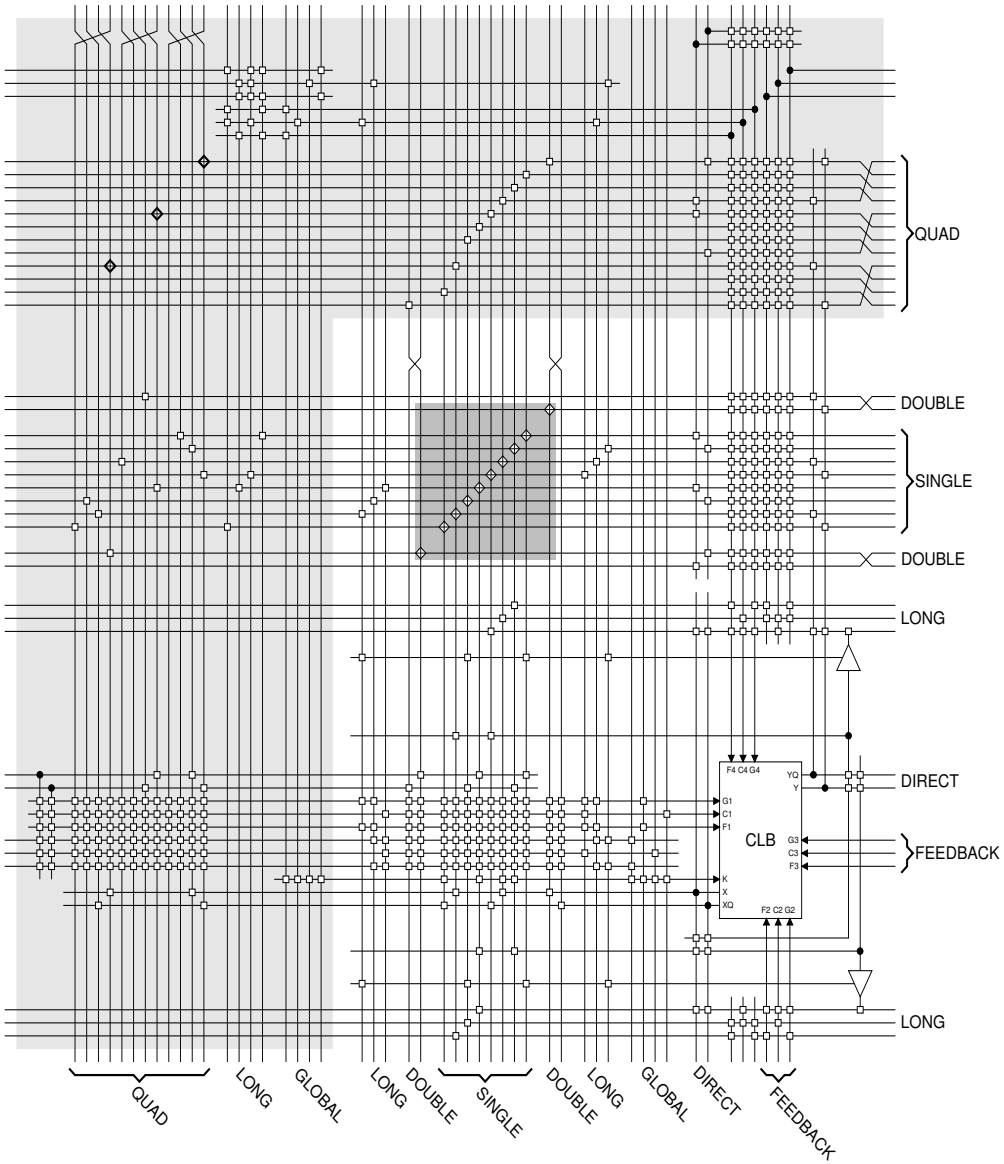
Vertical Axis
Percent length 2

Percent length 3 -->

[Khellah/Brown/Vranesic CICC'94]

Note: "Average" interconnect delay – not design critical path delay.

Xilinx 4K

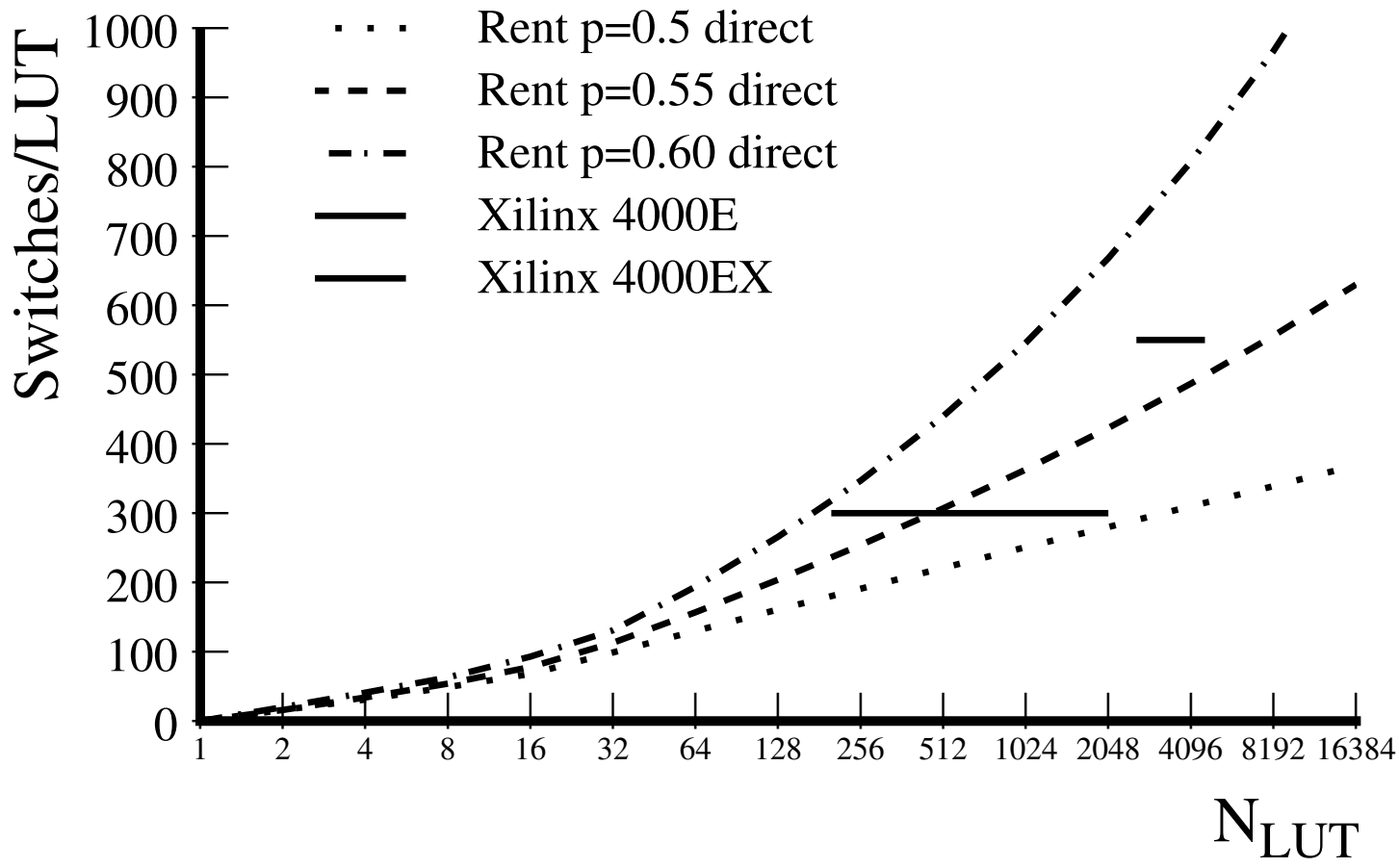


Common to XC4000E and XC4000EX

XC4000EX only

Programmable Switch Matrix

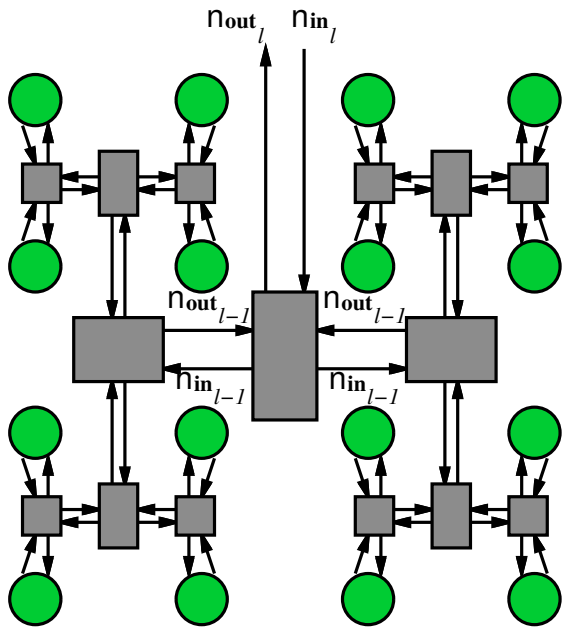
Xilinx 4K Switches



XC4000E ≈ 300; XC4000EX ≈ 550;

Hierarchical FPGA

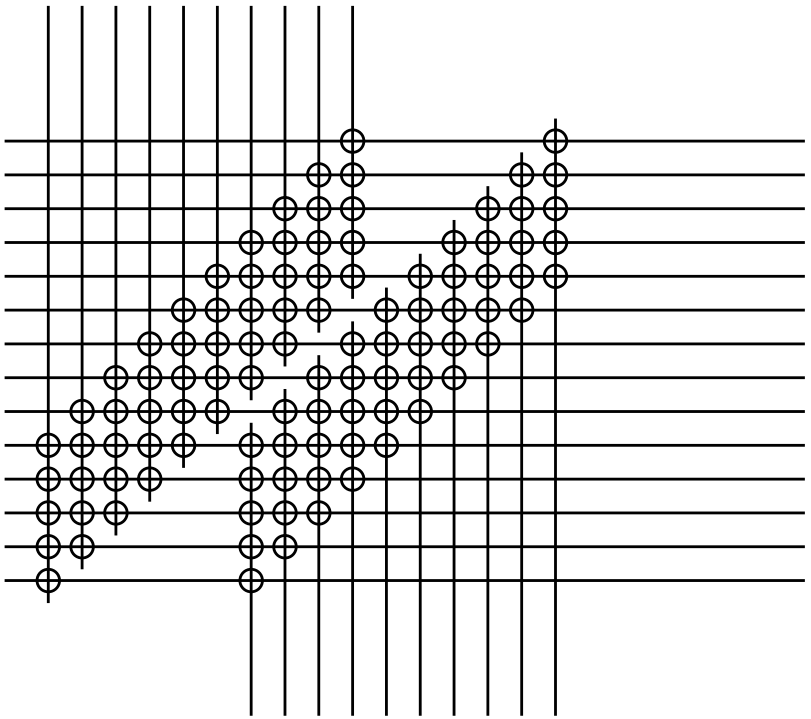
- close to model we saw on Day 12
- Aggarwal/Lewis – similar study to Brown/Rose
  - Channel sizes from global route
  - Look at switchbox population



Hierarchical FPGA Switch Depopulation

Flexibility in channel assignment:

- n **choose** m
- **2-ary** $\rightarrow Cn^p \times C(2n)^p$



Hierarchical FPGA Switch Depopulation

- n **choose** m **2-ary** $\rightarrow Cn^p \times C(2n)^p$

Again: $n - m + 1$ **switches or** $\left(2^p Cn^p - Cn^p + 1\right)$
Considering: $Cn^p \times 2^p Cn^p$ **switch box**

$$\frac{\left(2^p Cn^p - Cn^p + 1\right) \times Cn^p}{\left(2^p Cn^p \times Cn^p\right)} \rightarrow \frac{2^p - 1}{2^p}$$

p	$\frac{2^p-1}{2^p}$
$p = 0.5$	**30%**
$p = 0.6$	**34%**
$p = 0.7$	**38%**

Hierarchical FPGA

Aggarwal and Lewis

- **Don't give channel widths**
- **Suggest F_C =3 lower levels, 3-5 upper**
- **60% switches in symmetric (length 1 lines only)**
- **Log switching delay (worst-case)**

N.B. Chan/Lewis FPGA'96 – deal with delays.

Review

- Symmetric, mesh routing topology
- Hierarchical routing topology
- Routing Model
- Requirements to route
- Opportunities to depopulate switches
- Compare commercial FPGA routing topology