CS294-7: Reconfigurable Computing

Day 14: Thursday, March 6

Interconnect

- Admin
- Interconnect Delays in VLSI

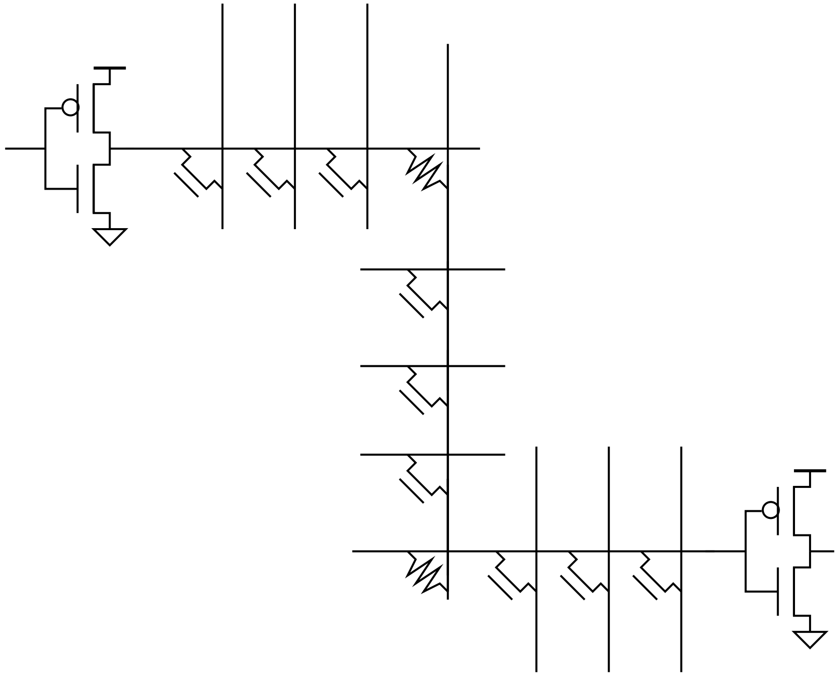
Admin

- Project 1
  - Due Tuesday (3/11)
  - Netlist request

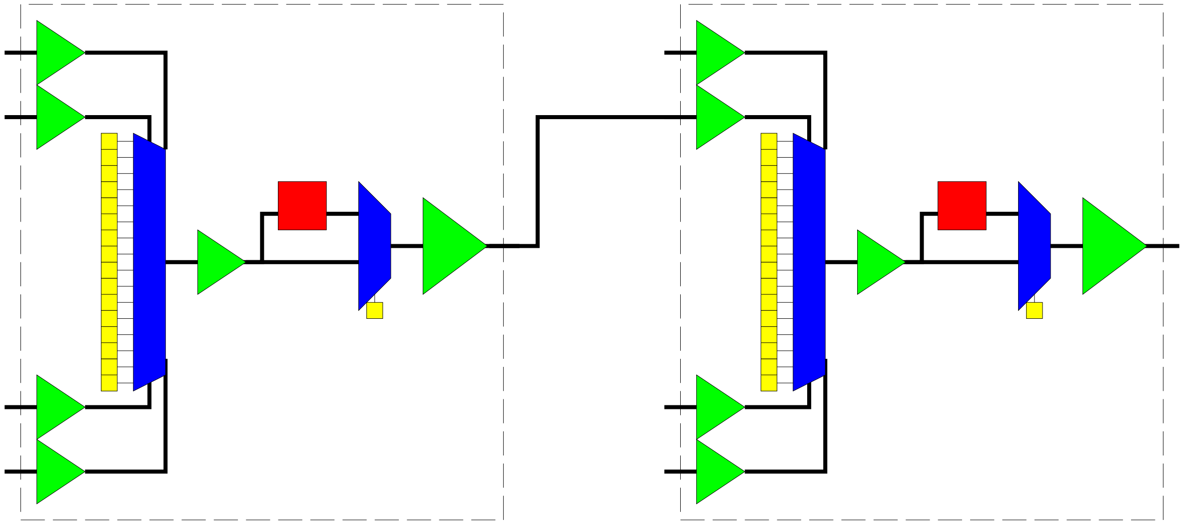
Interconnect Delay

What makes configurable interconnect slow:

- long lines
- capacitive stubs
- resistive switches

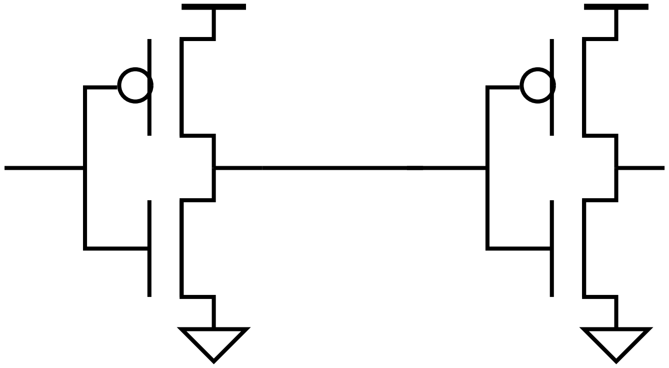


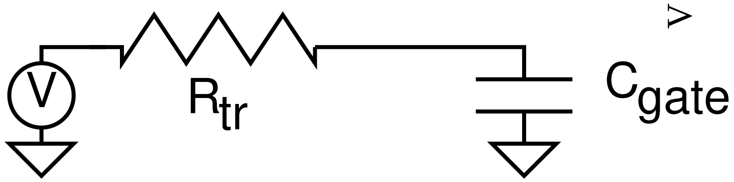
Driver/Reciever

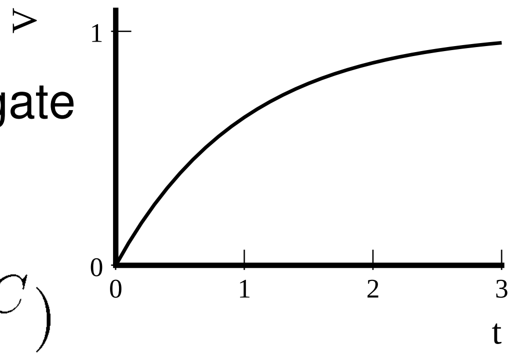


Driver/Reciever

- Drive transitor – model as resistance to source rail
- Recieving gate – presents input capacitance







$$V_{out} = V_{signal}(1 - e^{-t/RC})$$

50% at $t = 0.7RC$**, 90% at** $t = 2.3RC$

Driver/Reciever

HP CMOS 14 (0.6μ):

N: @ $\frac{W}{L} = \frac{10}{0.6}$, $V_{ds} = 3.3$**V,** $I_{ds} = 4$**mA.** $\rightarrow R_{tr}$ **= 13.75K**Ohm $\left(\frac{L}{W}\right)$

P: @ $\frac{W}{L} = \frac{10}{0.6}$, $V_{ds} = -3.3$**V,** $I_{ds} = 2$**mA.** $\rightarrow R_{tr}$ **= 27.5K**Ohm $\left(\frac{L}{W}\right)$

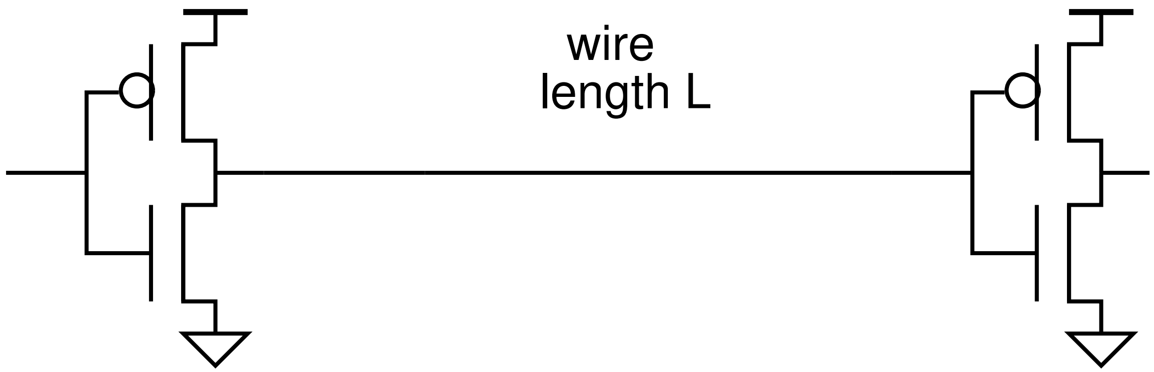
$C_{gate} \approx (W \times L) C_{OX}$ $\quad$ $C_{OX} = 3.8 \times 10^{-3} pF/\mu\text{m}^2$

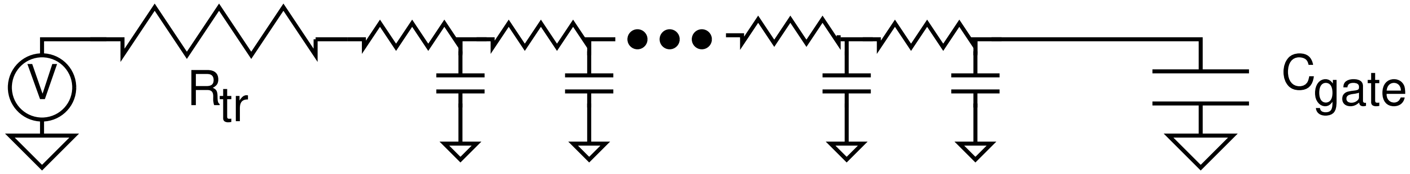
$L = 0.6\mu\text{m}$

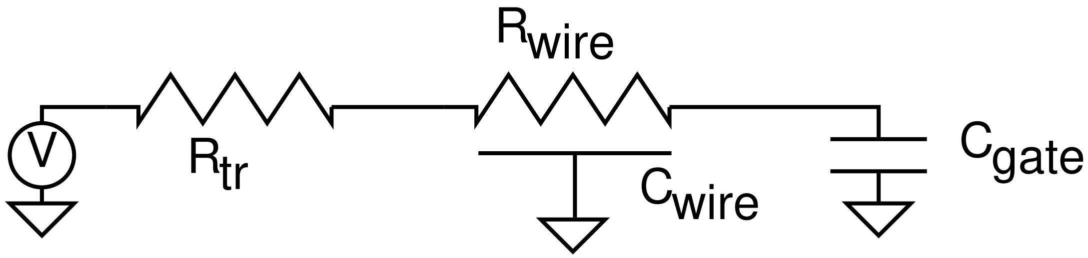
Assume:	**Driver**	**Receiver**
	$W_n = 6\mu$	$W_n = 3\mu$
	$W_p = 12\mu$	$W_p = 6\mu$

$R_{tr} = 1.38$**K**Ohm**,** $C_{gate} = 0.041$pF $\rightarrow RC = 0.056$**ns**

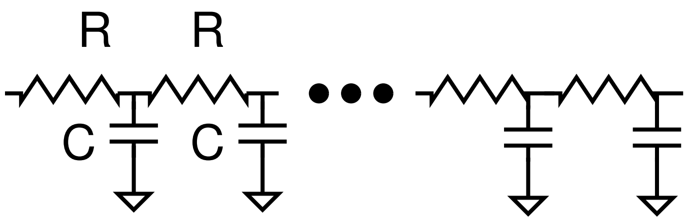
Wire







Distributed RC



$$RC + 2RC + 3RC + \ldots = \frac{k(k+1)}{2}(RC) \approx \frac{1}{2}\left(RCk^2\right)$$

Response:

50% at $t = 0.4RC$**, 90% at** $t = 1.0RC$

Wire

Wires (HP CMOS 14):

$R_\square = 70$mOhm

Dense metal 1μ **trace and space:**

$C_{m1} \approx 250$aF$/\mu$m **(**$C_{m2} \approx 150$aF$/\mu$m**)**

$C_{m1\square} \approx 250$aF **(**$C_{m2\square} \approx 150$aF**)**

$R_{wire} = \left(L/1\mu\text{m}\right) R_\square$**,** $C_{wire} = \left(L/1\mu\text{m}\right) C_\square$

Logic Block $\approx$ **1K**$\lambda \times$ **1K**λ

Say 300 squares per logic block crossed.

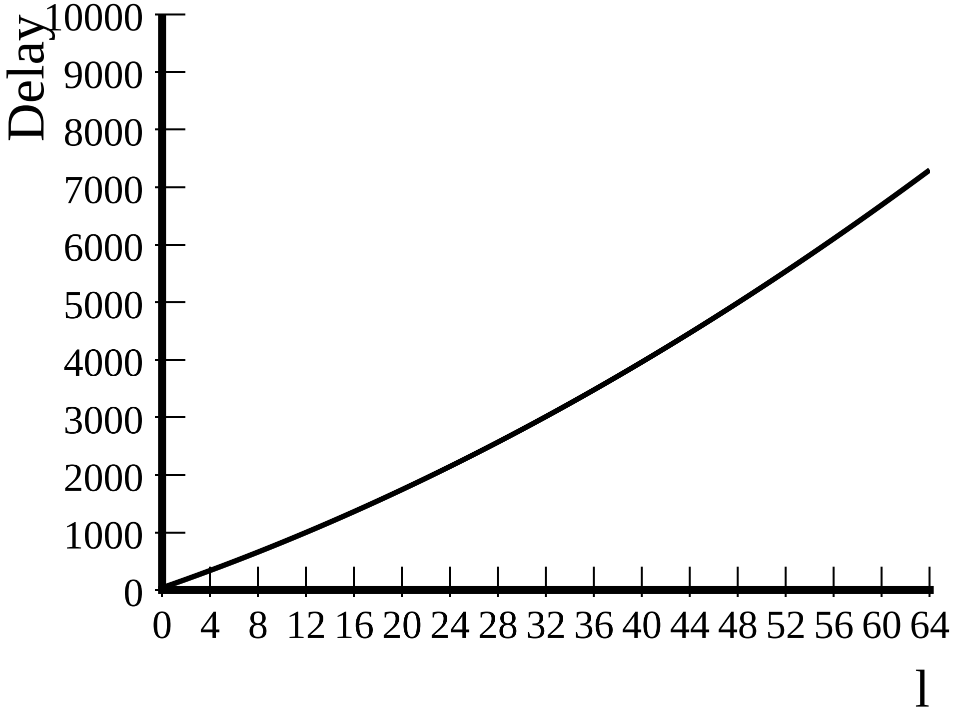
$$R_{lb} = 300 R_\square = 21\text{Ohm}$$

$$C_{lb} = 300 C_\square = 75\text{fF}$$ **m1**

$$RC_{lb} = 1.6$$**ps**

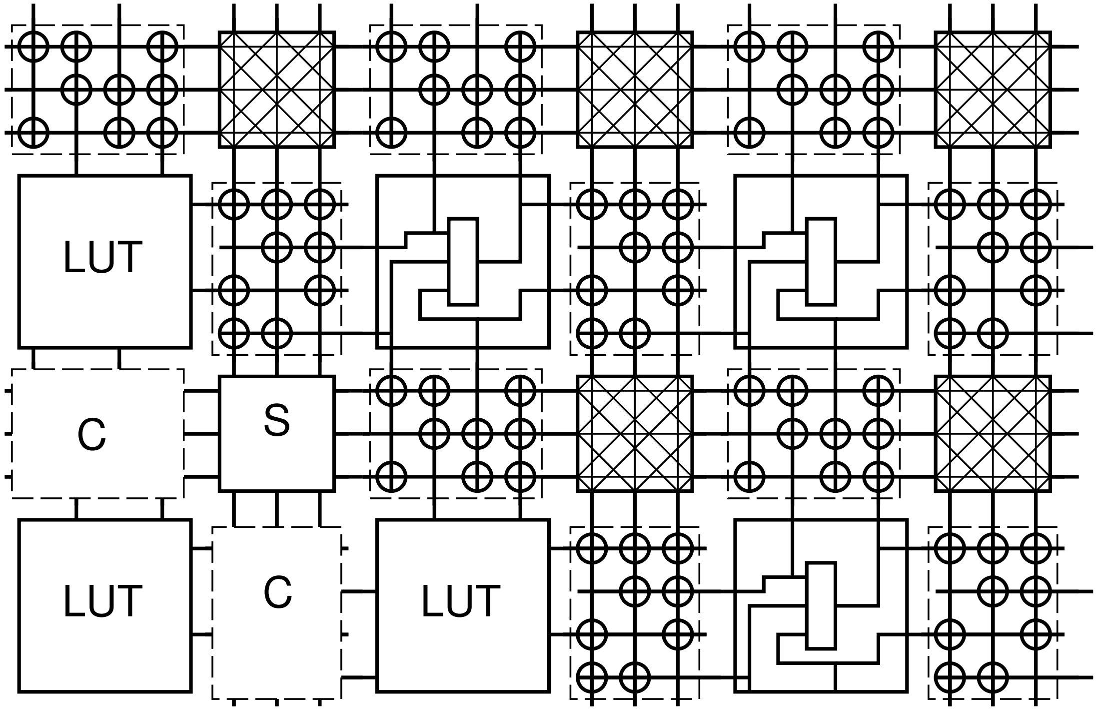
Wire Delay

$$T = 0.4\left(l^2 \cdot RC_{lb}\right) + 0.7\left(l \cdot R_{tr}C_{lb} + R_{tr}C_{gate} + l \cdot R_{lb}C_{gate}\right)$$

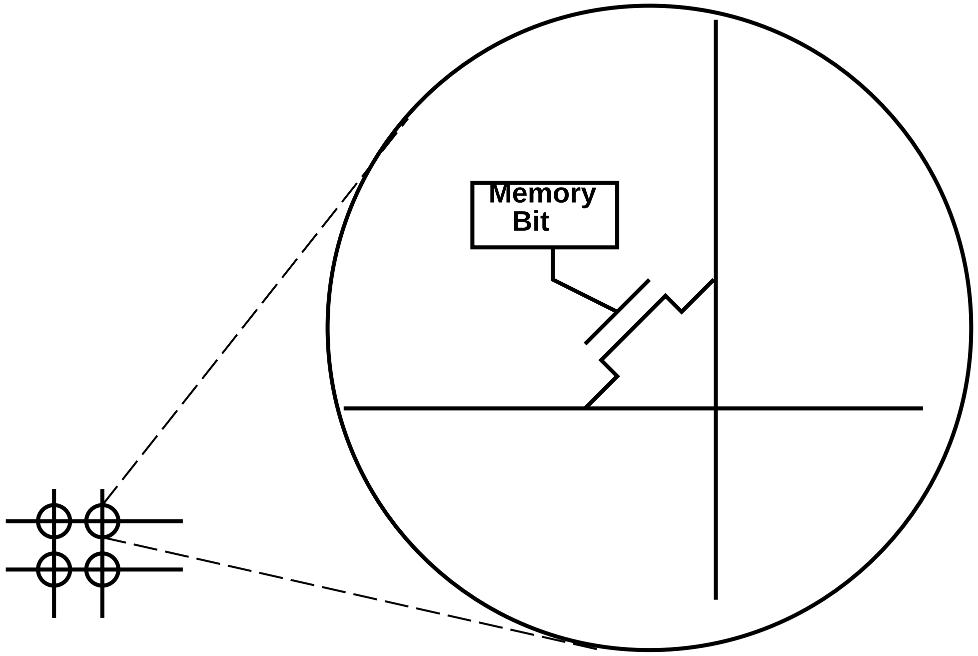


(*N.B.* 4025 is 32×32; Max Manhattan 64)

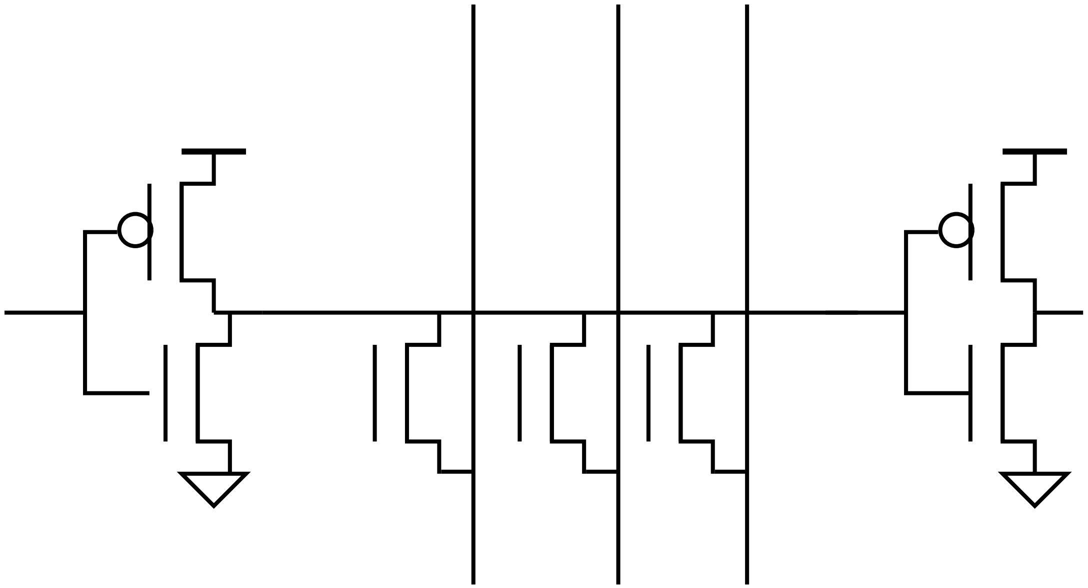
Switch Points



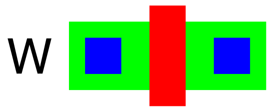
Switch Points Up Close



Switch Stubs



Switch Stubs



L_{diff} = 0.2+0.8+0.6=1.6um

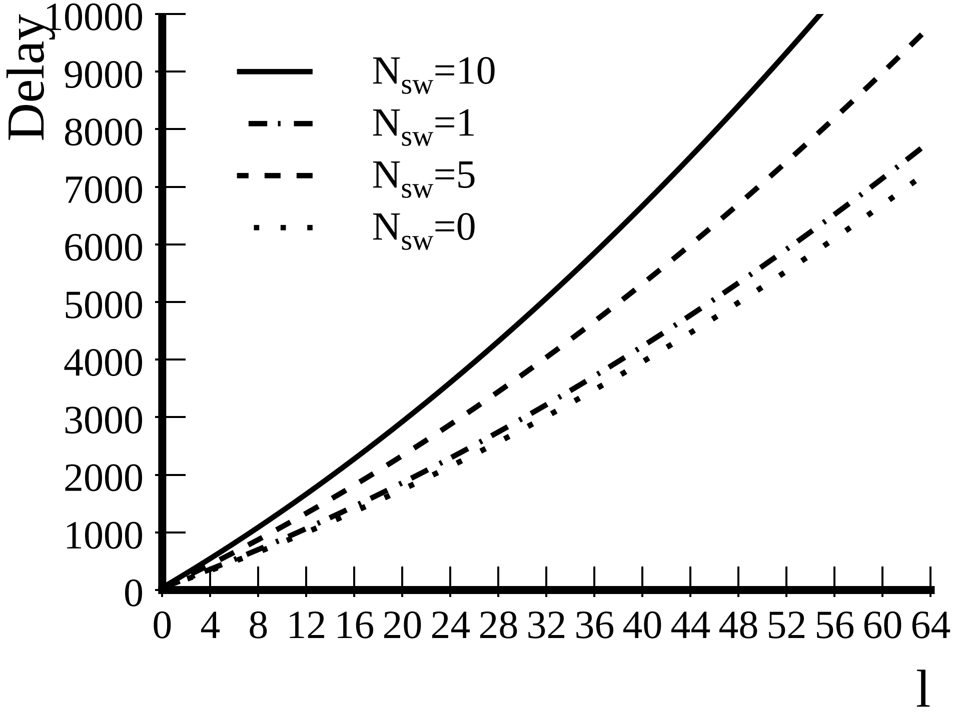
$$
\begin{aligned}
C_{drain} &= W L_{diff} C_J + 2(W + L_{diff}) C_{JSW} \\
C_J &= 470\text{aF}/\mu\text{m}^2 \\
C_{JSW} &= 320\text{aF}/\mu\text{m} \\
L_{diff} &\approx 1.6\mu\text{m}
\end{aligned}
$$

Assume $W = 3\mu$m**:**

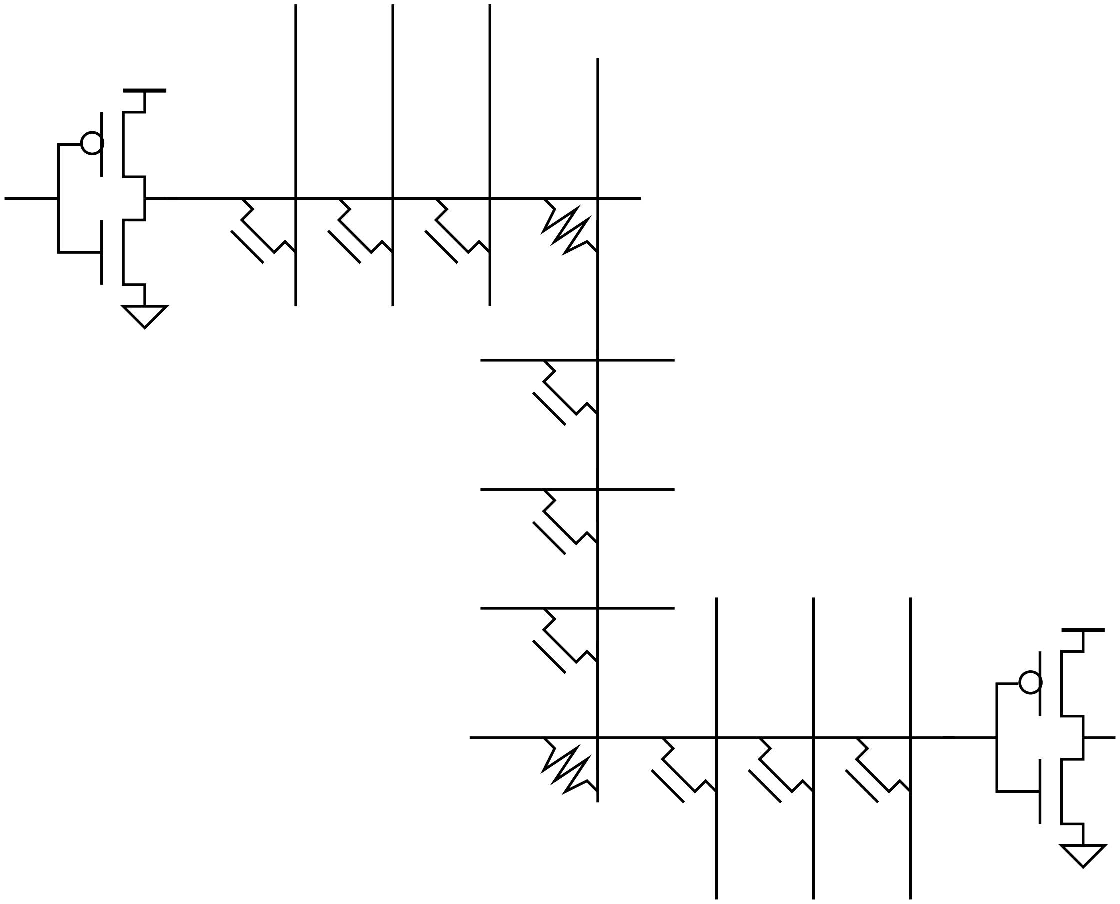
$$C_{drain} = 5.2\text{fF}$$

Wire+Stub Delay

$$T = 0.4\left(l^2 \cdot RC_{lb} + l^2 \cdot N_{sw/ch} R_{lb} C_{drain}\right) + 0.7\left(R_{tr}\left(l \cdot C_{lb} + l \cdot N_{sw/ch} \cdot C_{drain} + C_{gate}\right) + l \cdot R_{lb} C_{gate}\right)$$



Switches are Resistive



with Switches

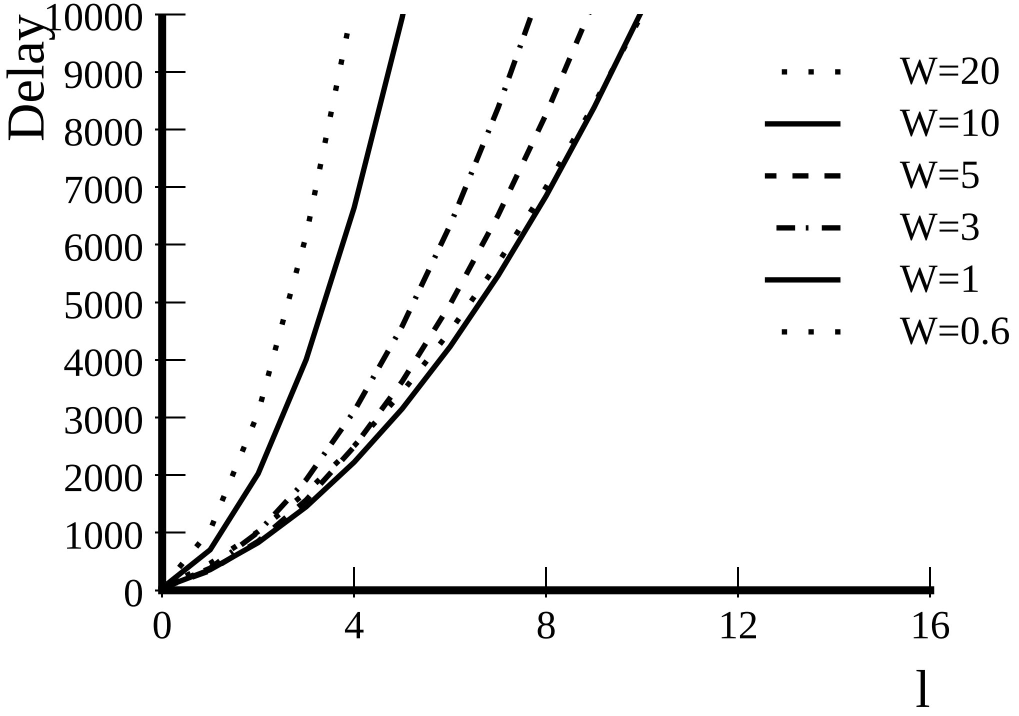
$$T = 0.4\begin{pmatrix} l^2 \cdot RC_{lb} + l \cdot N_{sw}R_{sw}C_{lb} + l \cdot N_{sw}R_{sw}N_{sw/ch}C_{drain} \\ + l^2 \cdot N_{sw/ch}R_{lb}C_{drain} \end{pmatrix}$$

$$+ 0.7\begin{pmatrix} R_{tr}\left(l \cdot C_{lb} + l \cdot N_{sw/ch} \cdot C_{drain} + C_{gate}\right) \\ + (l \cdot R_{lb} + N_{sw}R_{sw})C_{gate} \end{pmatrix}$$

with Switches

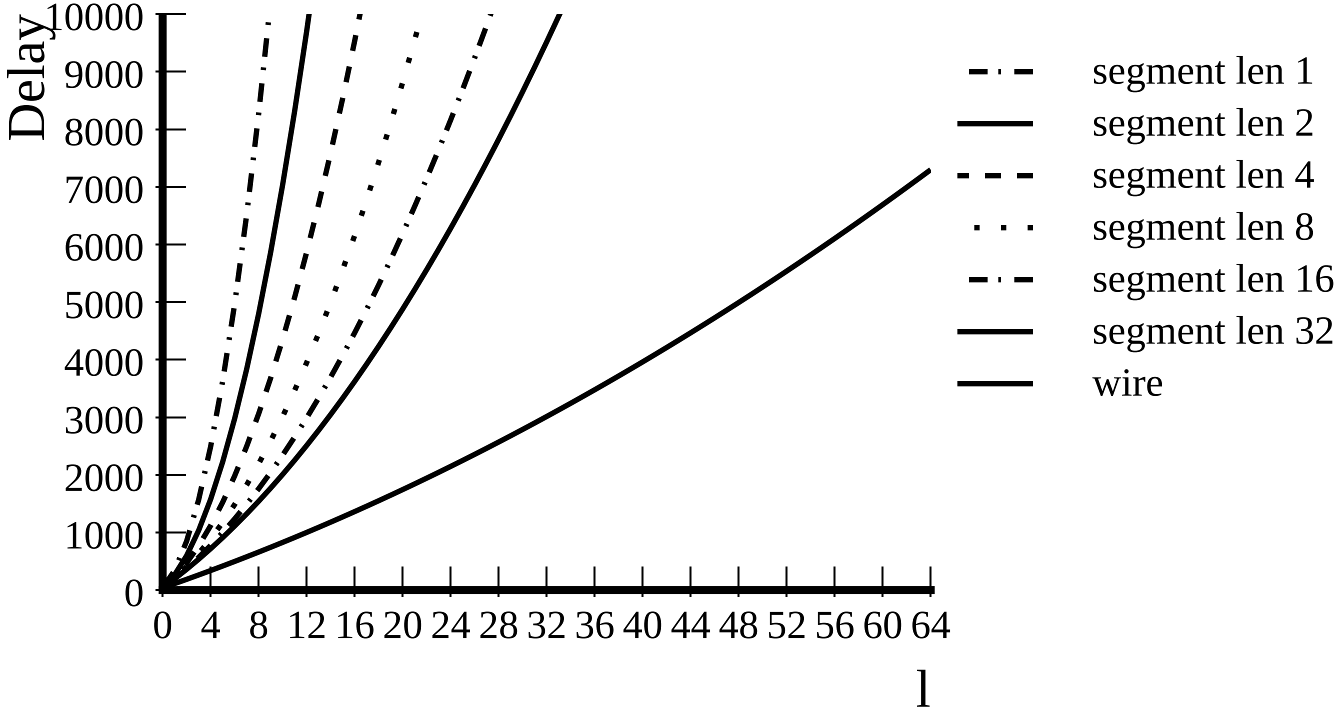
$N_{sw/ch} = 10$, **one switch per logic block** ($N_{sw} = l$)

Varying W ($W \uparrow \Rightarrow C \uparrow R \downarrow$)



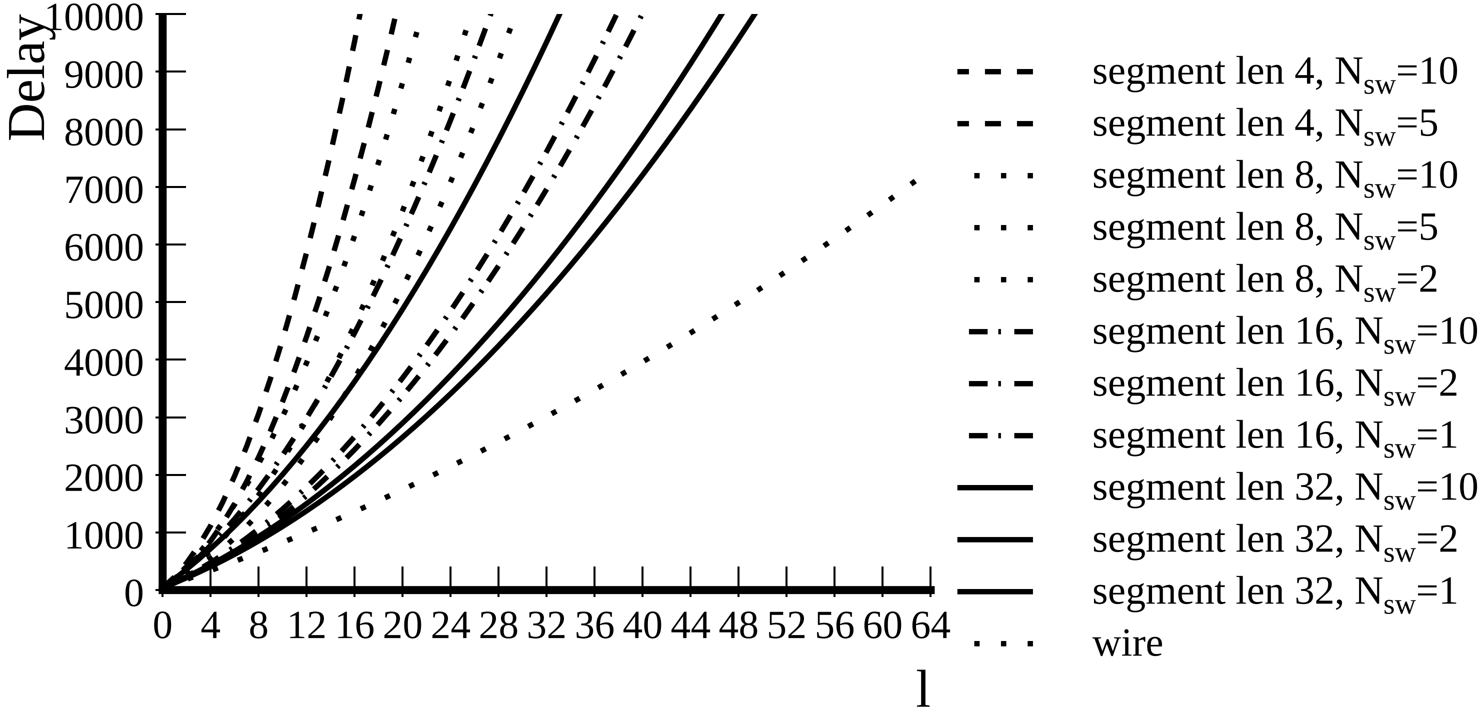
Segmentation

$W = 5$, $N_{sw/ch} = 10$



Segmentation

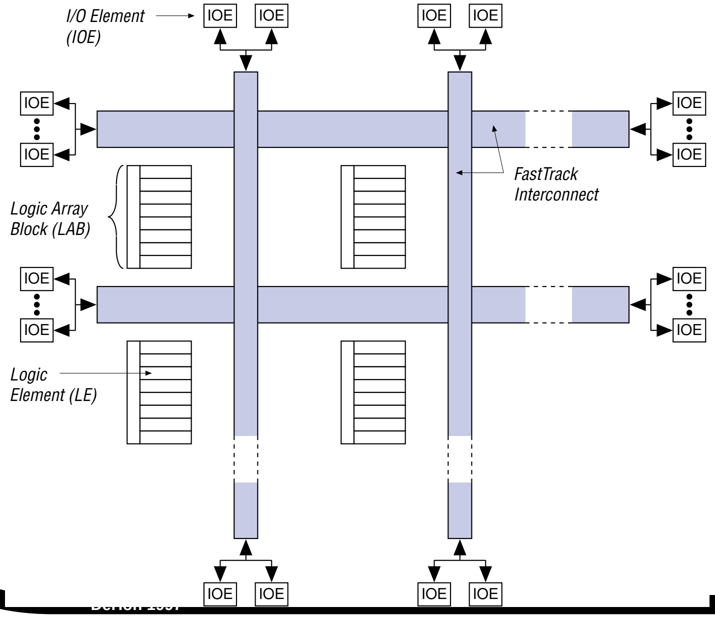
$W = 5$, $N_{sw/ch}$ **varying**

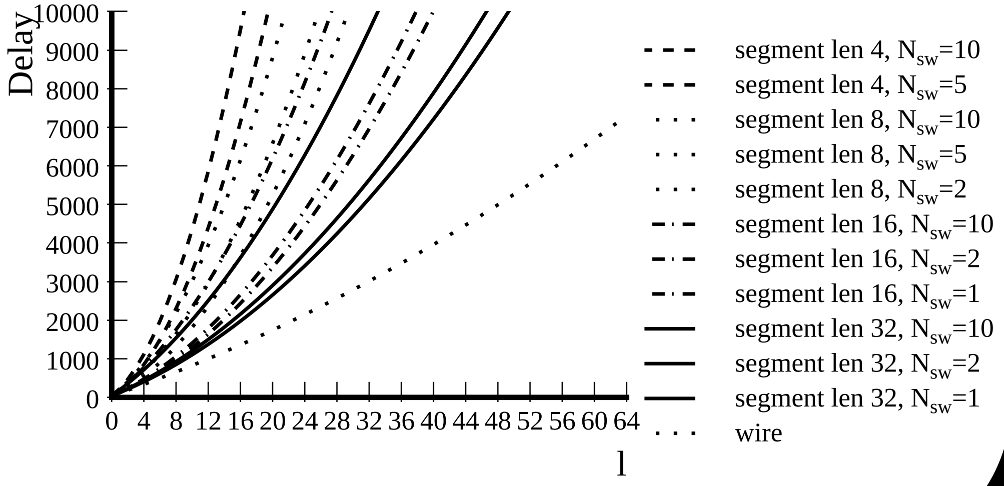


Altera Interconnect Delay

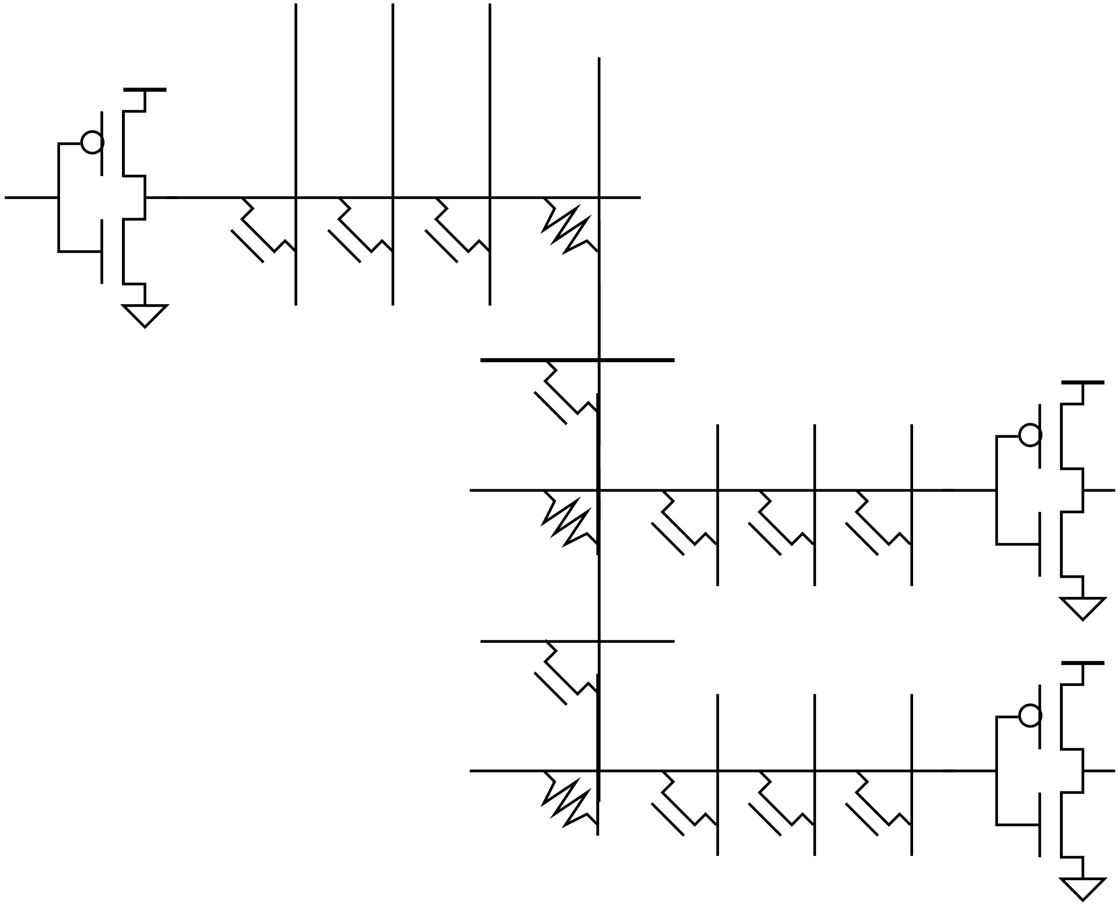
10K10-3 (576 4-LUTs) 10K100-3 (4,992 4-LUTs)

LUTs	Distance	10K10 Delay (ps)	10k100 Delay (ps)
8	same LAB	400	400
24(52)×8	same row	2600	3700
8×3(12)	same column	3500	5500
576 (4,992)	different rows	6100	9200



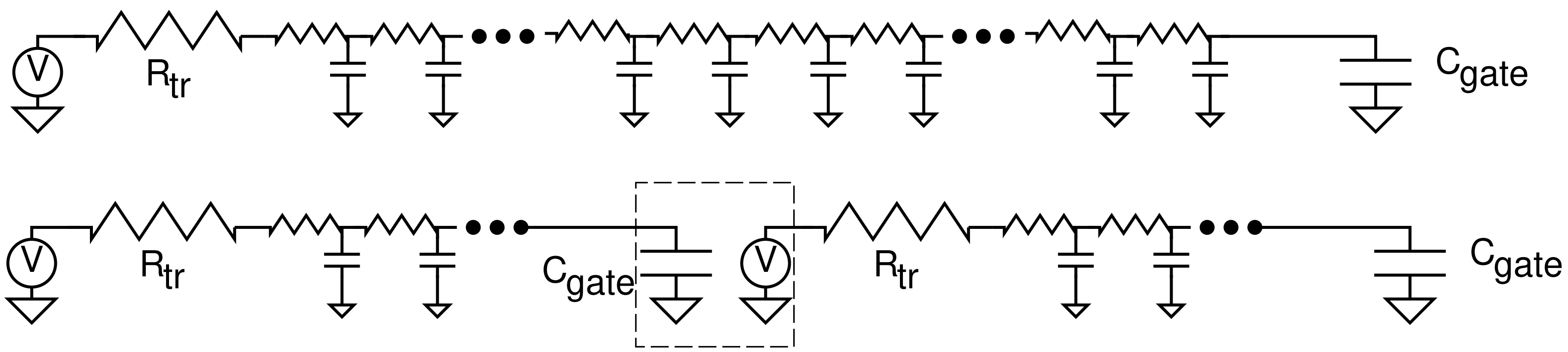


Branches caused by Fanout



Buffering

Consider buffering at each switch:



Buffering

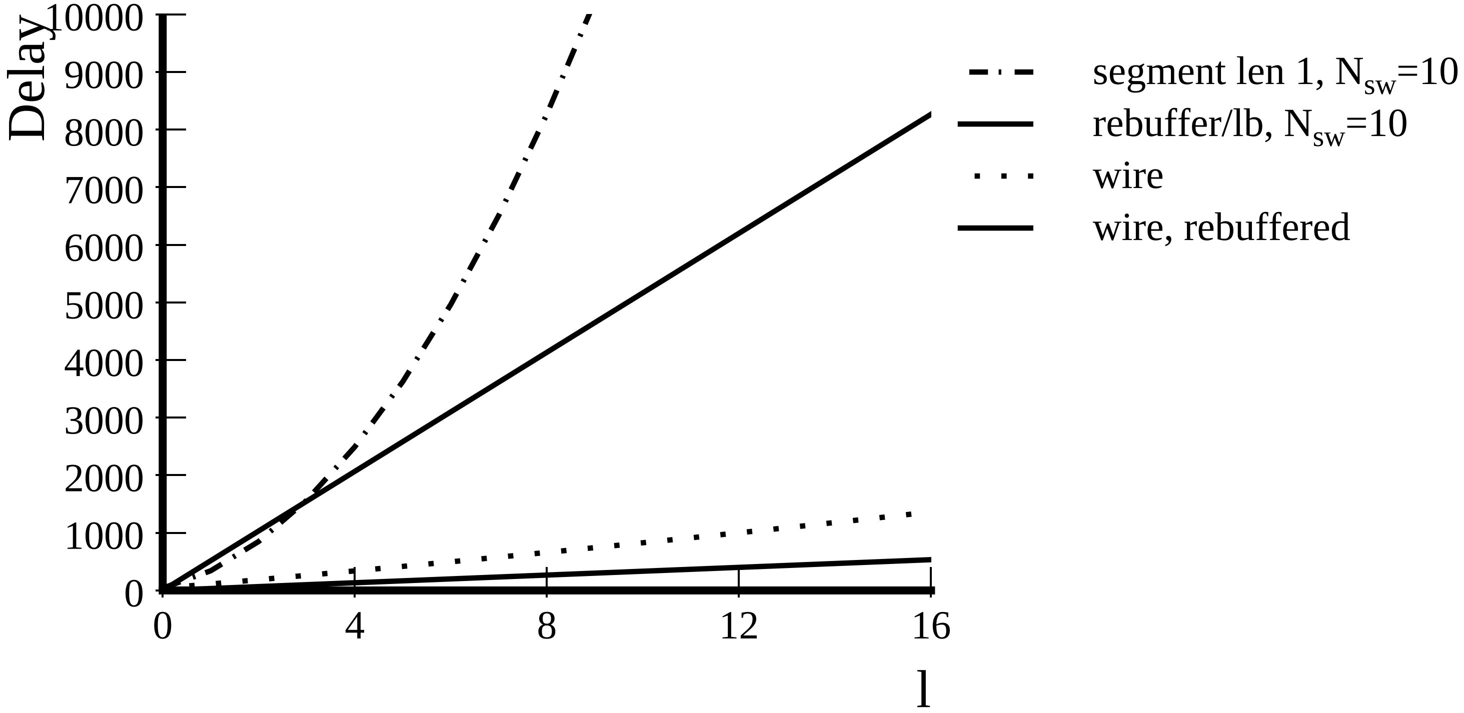
$$T = 0.4\left(l^2 \cdot RC_{lb} + l \cdot N_{sw}R_{sw}C_{lb} + l \cdot N_{sw}R_{sw}N_{sw/ch}C_{drain} \right.$$
$$\left. + l^2 \cdot N_{sw/ch}R_{lb}C_{drain} \right)$$
$$+ 0.7\left(R_{tr}\left(l \cdot C_{lb} + l \cdot N_{sw/ch} \cdot C_{drain} + C_{gate}\right) \right.$$
$$\left. + (l \cdot R_{lb} + N_{sw}R_{sw})\, C_{gate} \right)$$

becomes:

$$T = l\left(0.4\left(RC_{lb} + N_{sw/ch} \cdot R_{lb}C_{drain}\right) \right.$$
$$\left. + 0.7\left((R_{tr} + R_{sw})\left(C_{lb} + N_{sw/ch} \cdot C_{drain} + C_{gate}\right) + R_{lb}C_{gate}\right) \right)$$

Avoids quadratic delay accumulation

Buffering



Delay
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
4
8
12
16
l
segment len 1, N_{sw}=10
rebuffer/lb, N_{sw}=10
wire
wire, rebuffered

Wire Delay

$$T = 0.4\left(l^2 \cdot RC_{lb}\right) + 0.7\left(l \cdot R_{tr}C_{lb} + R_{tr}C_{gate} + l \cdot R_{lb}C_{gate}\right)$$

$$T_{buf} = k\left(0.4\left(\frac{l^2}{k^2} \cdot RC_{lb}\right) + 0.7\left(\frac{l}{k} \cdot R_{tr}C_{lb} + R_{tr}C_{gate} + \frac{l}{k} \cdot R_{lb}C_{gate}\right)\right)$$

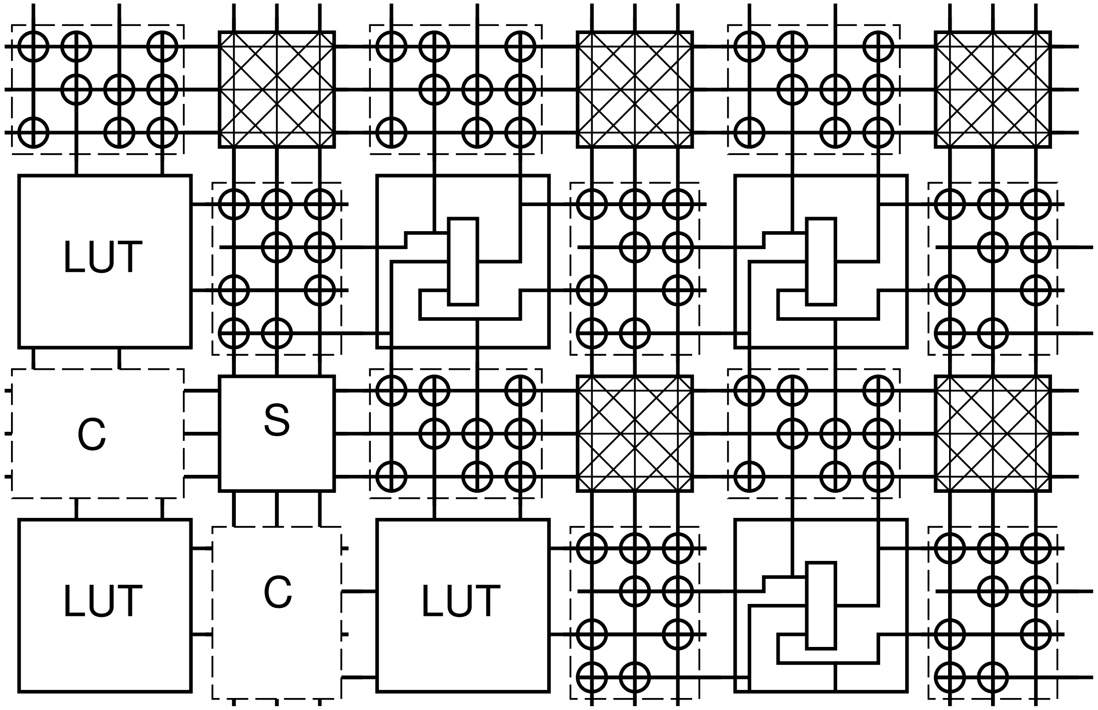
$$T_{buf} = \left(0.4\left(\frac{l^2}{k} \cdot RC_{lb}\right) + 0.7\left(l \cdot R_{tr}C_{lb} + kR_{tr}C_{gate} + l \cdot R_{lb}C_{gate}\right)\right)$$

$$\frac{\partial T_{buf}}{\partial k} = 0 = \left(-0.4\left(\frac{l^2}{k^2} \cdot RC_{lb}\right) + 0.7\left(R_{tr}C_{gate}\right)\right)$$

$$0.4\left(\frac{l^2}{k^2} \cdot RC_{lb}\right) = 0.7\left(R_{tr}C_{gate}\right)$$

$$k = \sqrt{\frac{0.4l^2 \cdot RC_{lb}}{0.7R_{tr}C_{gate}}}$$

Where put buffers?



Summary

- It's the wires (and the switches)
- Wire RC's add up
- Quadratic delay build up without buffering
- Switchpoints add capacitance
- Transistor switches add resistance
- All adds up $\rightarrow$ big interconnect delays
- Segmentation helps $\rightarrow$ reduce switch R's
- Isolating capacitive stubs on long wires helps
- Buffering allows linear delay with distance
- For buffering, need directional wires