CS294-7: Reconfigurable Computing

Day 18: Thursday, March 20

Compute Blocks

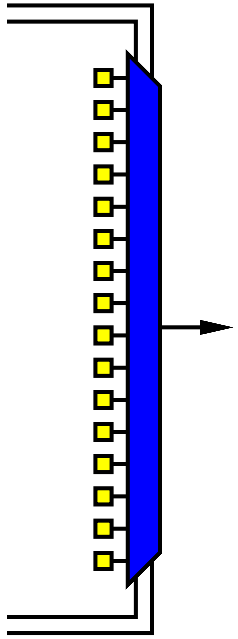
- Admin
- Look-Up Tables (LUTs)

Admin

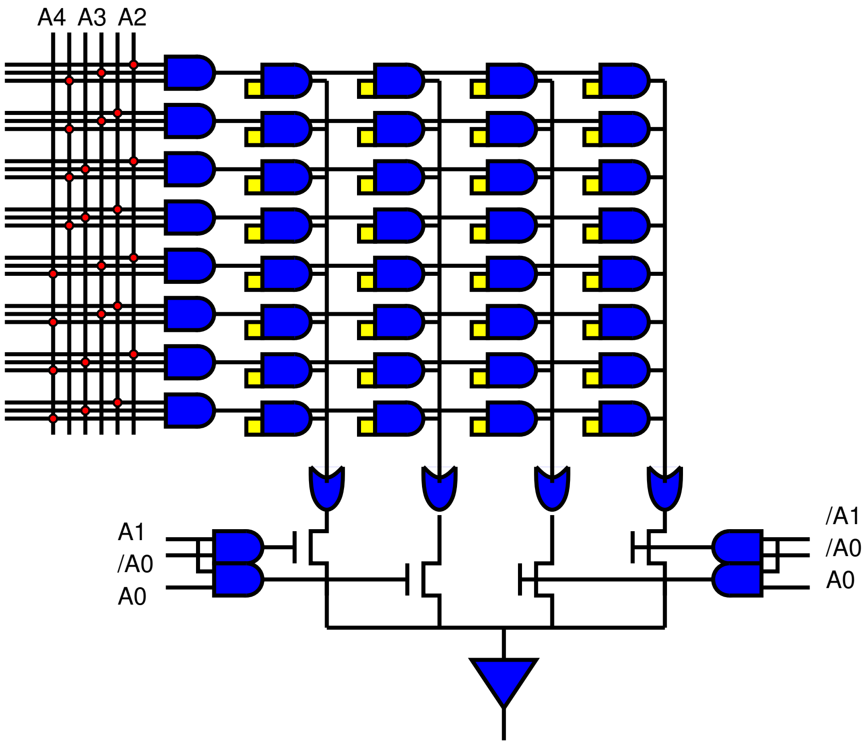
- **FCCM pre-registration due 3/25**
  `<http://www.fccm.org>`
- **Spring Break next week**

Look Up Table

- setup: preload bits into table
- operation: table provides translation from inputs to output(s)



Look Up Table



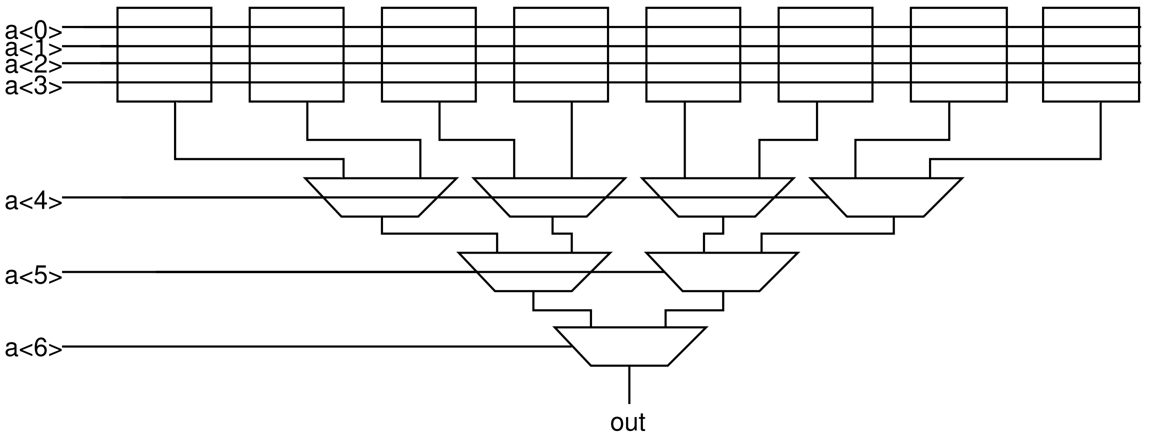
LUT for Computation

- color transform
- texture mapping
- initial guess or approximation
- encryption function
- character translation
- multiply, multiply modulo n

How much?

How much computation can be performed in a table lookup?

Upper Upper Bound:



$$M\textbf{-LUT} \leq 2^{M-4} + \left(2^{M-4} - 1\right) \leq 2^{M-3} \textbf{ 4-LUTs}$$

How much?

How much computation can be performed in a table lookup?

Lower Upper Bound: 2^{2^M} functions in M-LUT

Need n 4-LUTs to cover:

$$\begin{aligned}
\left(2^{2^4}\right)^n &\geq 2^{2^M} \\
n\log\left(2^{2^4}\right) &\geq \log\left(2^{2^M}\right) \\
n2^4\log(2) &\geq 2^M\log(2) \\
n2^4 &\geq 2^M \\
n &\geq 2^{M-4}
\end{aligned}$$

Adding Upper Bound:

$$2^{M-4} \leq n \leq 2^{M-3}$$

Comparing Memories and LUTs

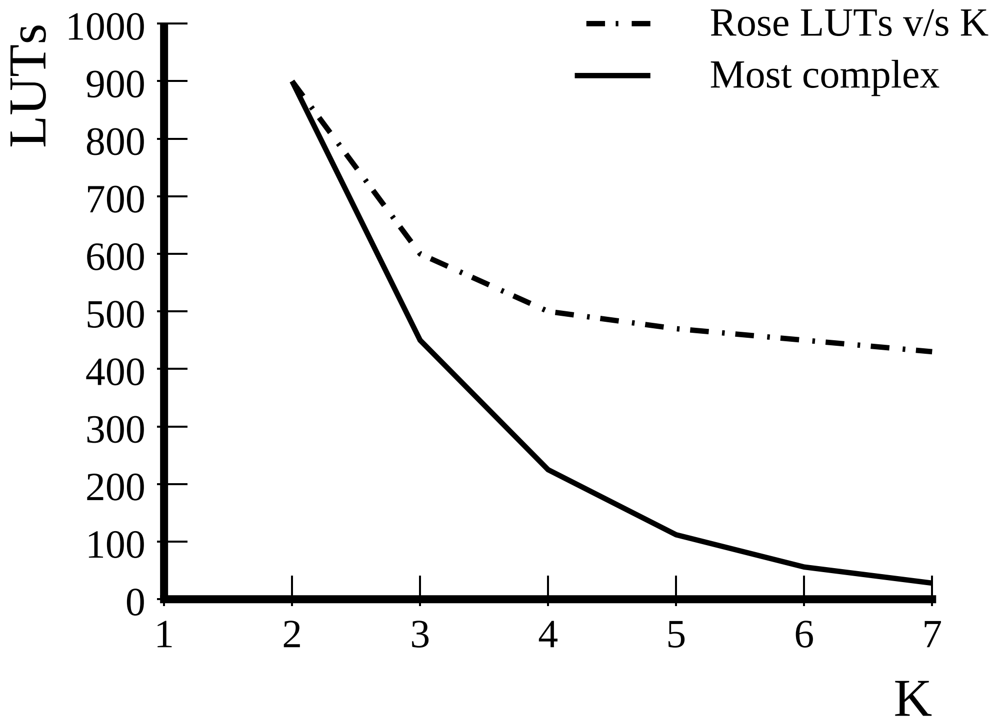
For most complex functions $\approx 2^{M-4}$ 4-LUTs in an M-LUT.

- **SRAM 32K$\times$8, $\lambda = 0.6\mu$, 170Mλ^2, 21 ns latency**
  $8 \cdot 2^{11} =$ **16K 4-LUTs**
- **XC3042, 288 4-LUTs, $\lambda = 0.6\mu$, 180Mλ^2, 13 ns CLB delay**
- **15-bit parity:**
  - **5 4-LUTs ($<$2% of XC3042)**
  - **entire 32K$\times$8 SRAM**
- **7-bit add:**
  - **14 4-LUTs ($<$5% of XC3042)**
  - **entire 32K$\times$8 SRAM**

LUT + Interconnect

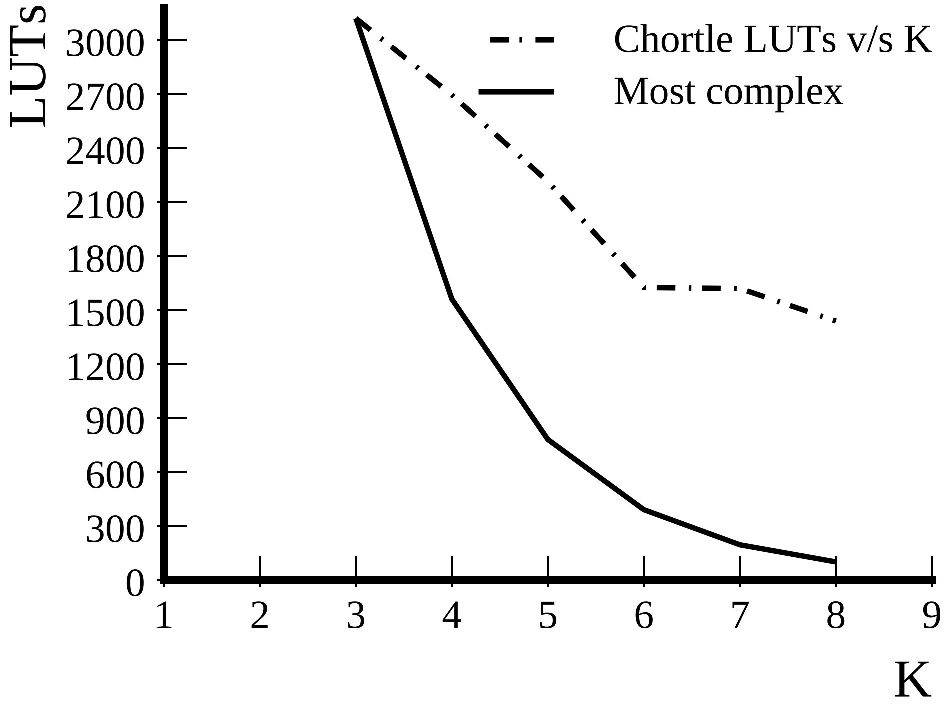
- Interconnect allows us to exploit structure in computations.
- Already know $A_{LUT} << A_{interconnect}$ on an FPGA
  $\rightarrow A_{FPGA}(M\text{-LUT}) >> A_{M-LUT}$
- Complexity of most M-input functions $<< 2^M$

LUTs v/s K



Rose LUTs v/s K
Most complex
LUTs
1000
900
800
700
600
500
400
300
200
100
0
1
2
3
4
5
6
7
K

LUTs v/s K

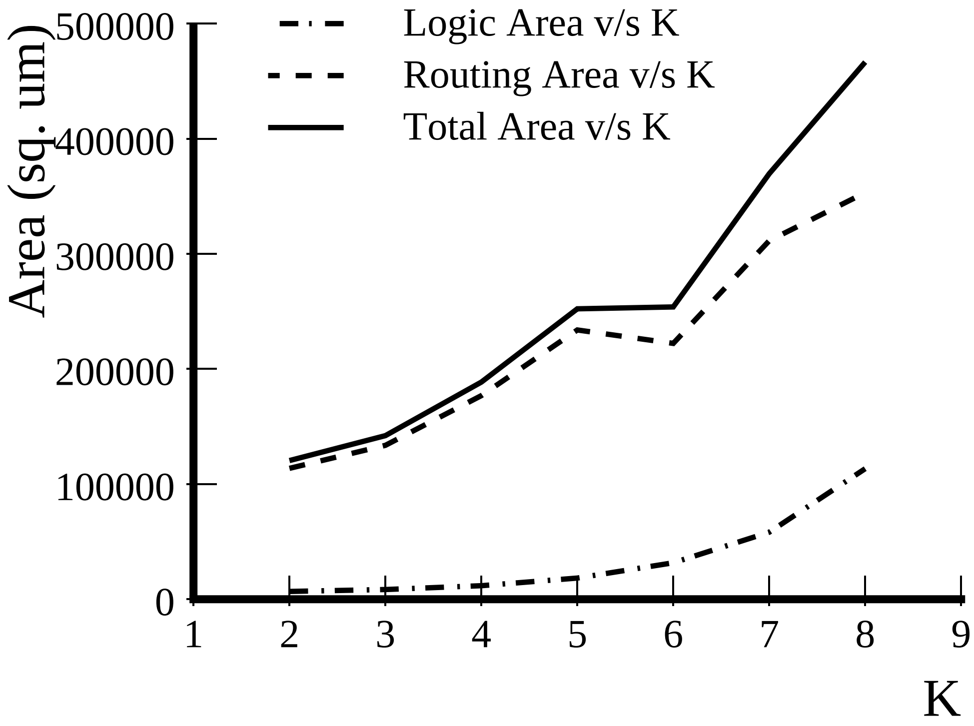


(for DES MCNC Benchmark)

LUT Area

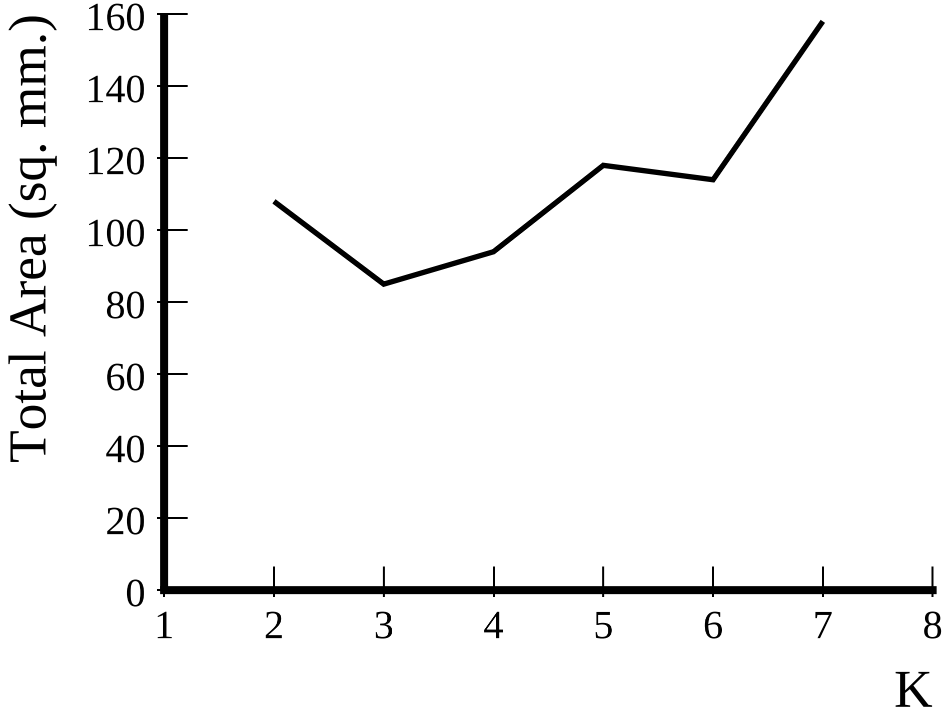
After K-LUT Mapping,
Route to determine W.

LUT area v/s K



Routing Area roughly linear in K

LUT area v/s K

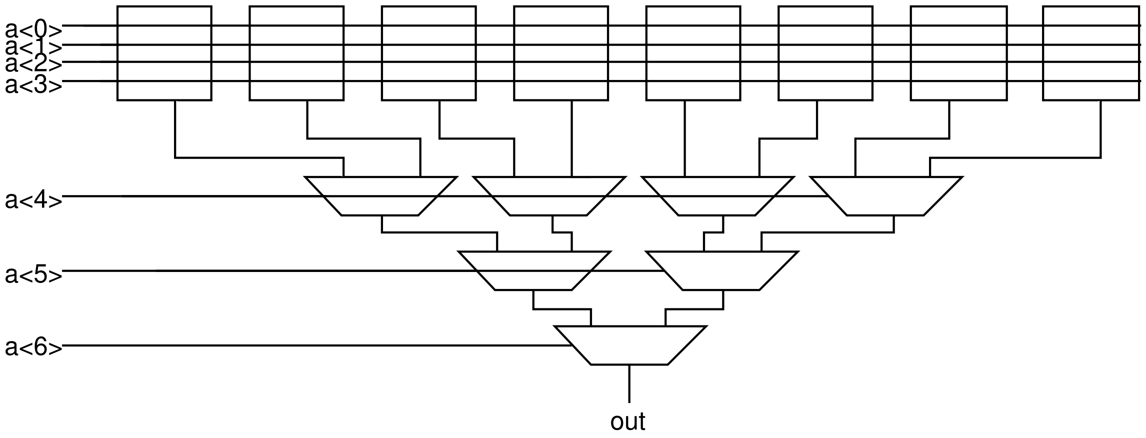


N.B. odd case w/ minimum at $k = 3$

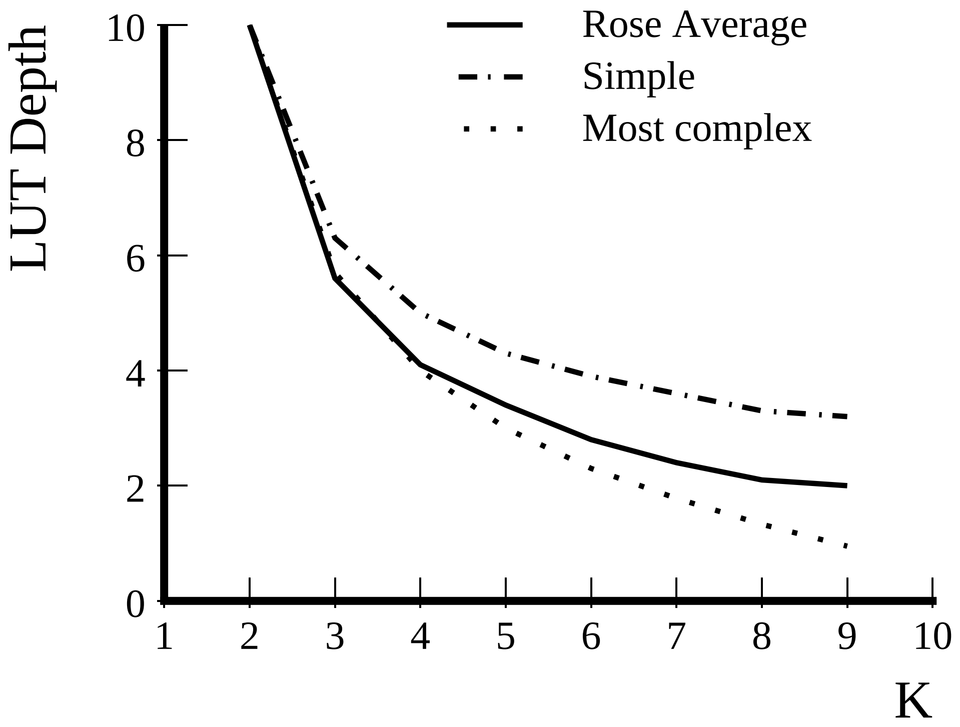
What about Delay?

Also depends on function complexity:
Circuit depth:

- **Simple functions (**M**-**`and`**):** $\lceil \log_k(M) \rceil$
- **Complex function:** $\left\lceil \frac{(n-k)}{\log_2(k)} \right\rceil$ **to** $\left\lceil \frac{(n-k)}{\log_2(k-\log_2 k)} \right\rceil + 1$



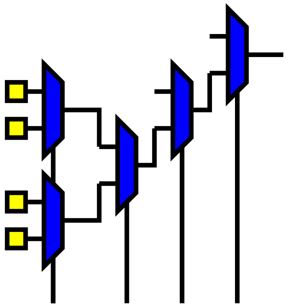
Circuit Depth v/s K



LUT Delay v/s K

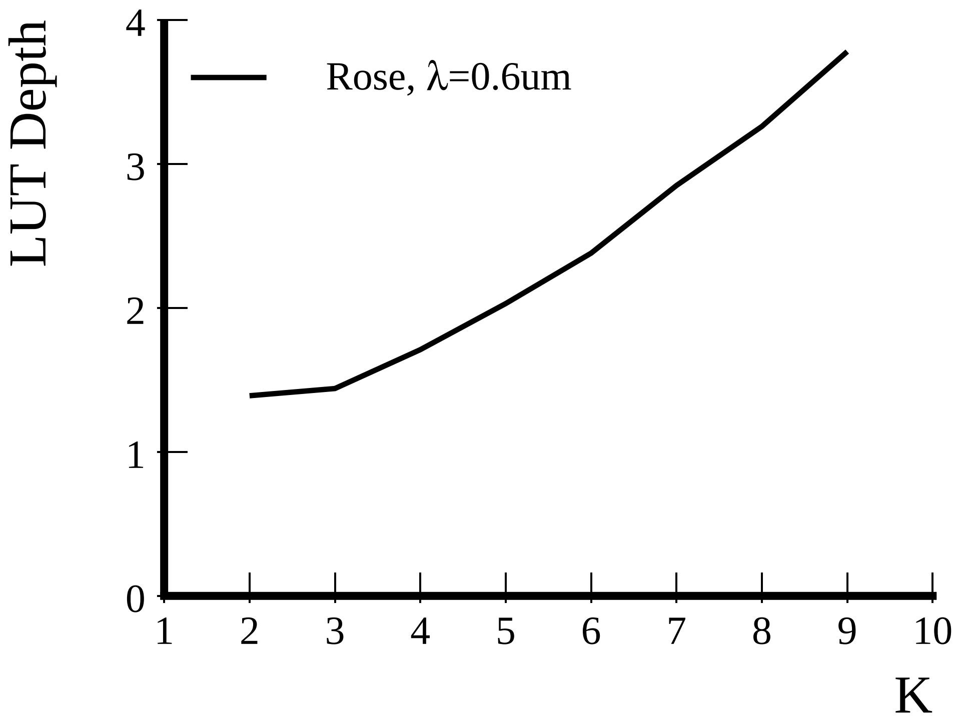
For small LUTs:

$$t_{LUT} \approx c_0 + c_1 \cdot k$$



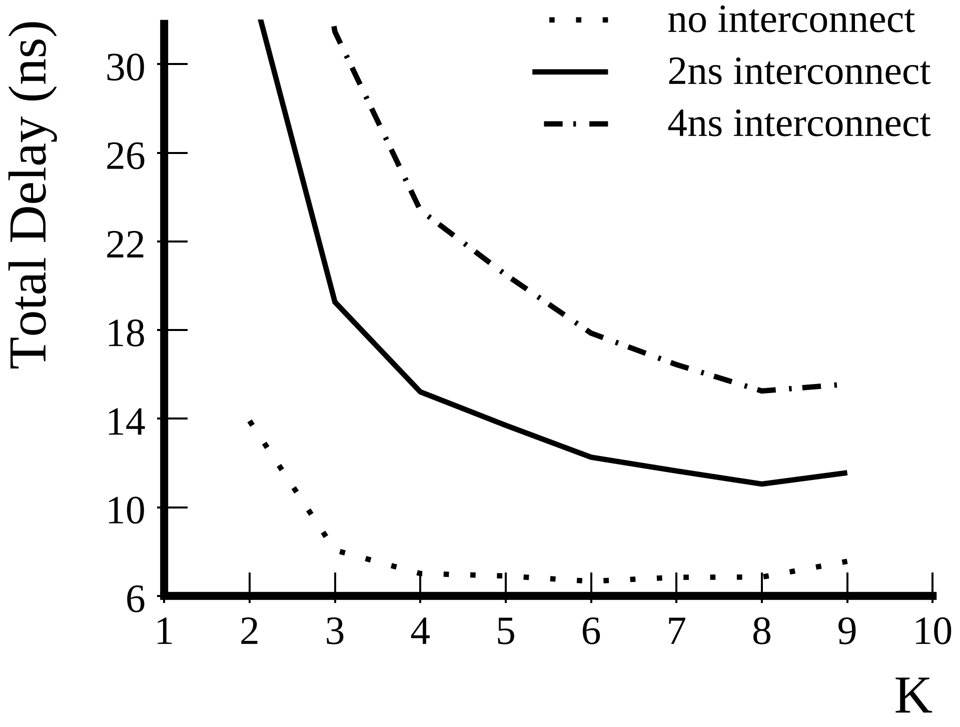
Large LUTs: length term $c_2 \cdot \sqrt{2^k}$
Plus Wire delay: $\sqrt{\text{area}}$, W

LUT Delay v/s K



(yes, this slide was missing in lecture)

Delay v/s K



no interconnect
2ns interconnect
4ns interconnect
Total Delay (ns)
30
26
22
18
14
10
6
1
2
3
4
5
6
7
8
9
10
K

Summary

- Memory most dense programmable for most complicated functions
- Memory scales poorly for structured tasks
- Most tasks have structure
- Interconnect allows us to exploit task structure

Summary

- Area
  - LUT count decreases with K, slower than exponential
  - LUT size increases with K
    exponential logic area, $\approx$ linear routing area
  - minimum area around $K = 4$
- Delay
  - LUT depth decreases with K, logarithmic
  - LUT delay increases with K
    linear + large fixed term
  - minimum delay around $K =$5-6