CS294-7: Reconfigurable Computing

Day 2: Thursday, January 23

- Computing Requirements
- VLSI Scaling

Scaling – Why?

Issue: We are in the midde of rapidly advancing VLSI technology.

Need to be able to reason about changes and trends for the future.

Need to be able to re-evalute existing, previous solutions given technology at time X.

Scaling

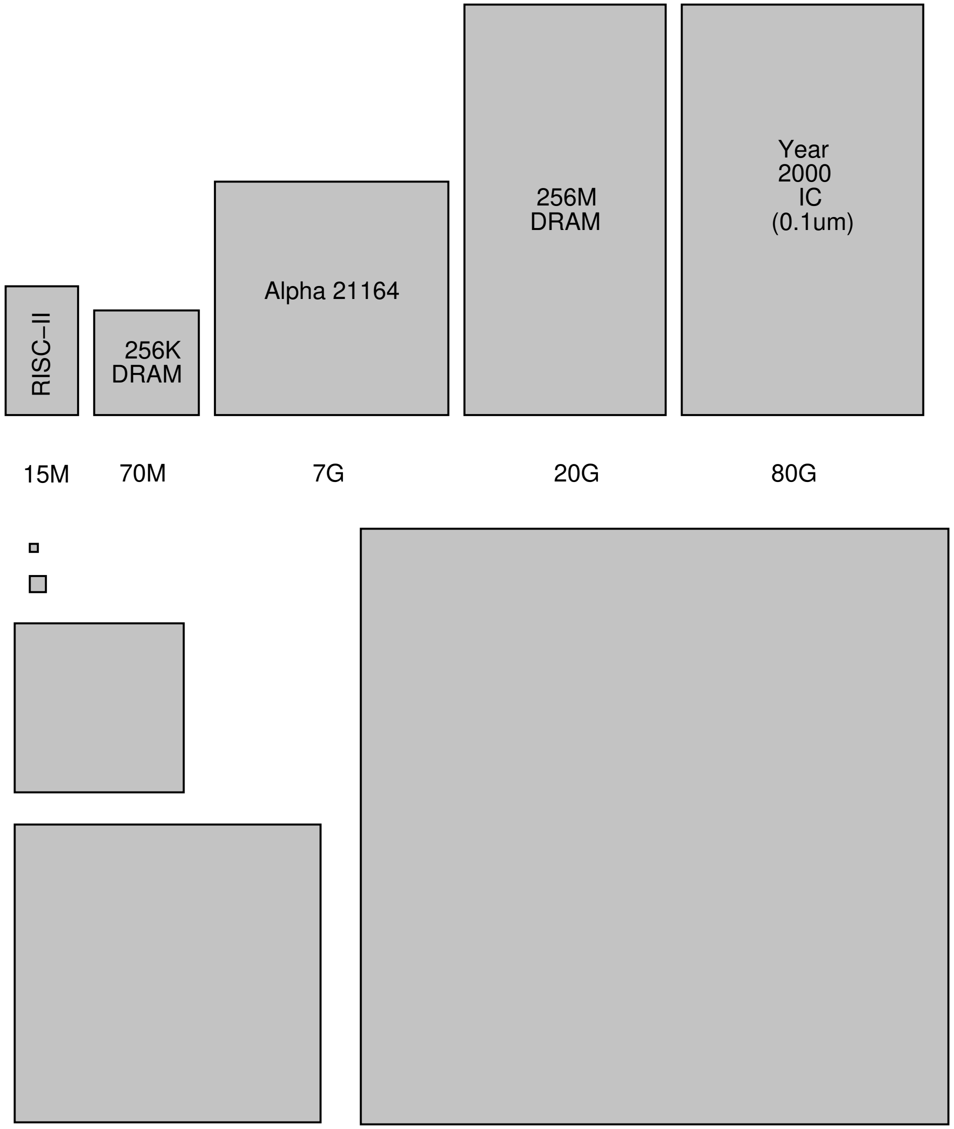
Basic premise: Scale features "uniformly" so everything gets better in a predictable manner.

Dennard	$1/\kappa$
Bohr	**S**
Mead and Conway (class)	λ

Scaling

Direct features		
	Channel Length (L)	$\frac{1}{\kappa}$
	Channel Width (W)	$\frac{1}{\kappa}$
	Oxide Thickness (t_{OX})	$\frac{1}{\kappa}$
	Doping (N_a)	κ
	Voltage (V)	$\frac{1}{\kappa}$
Consequences		
	Capacitance C	
	Threshold V_{th}	
	Current (I_d)	
	Gate Delay τ_{gd}	
	Wire Delay τ_{wire}	
	Power P_d	

Area effects



Capacitance

Before:

$$C_{OX} = \frac{\epsilon_{\mathrm{SiO_2}}}{t_{OX}}$$

After:

$$\begin{aligned} C'_{OX} &= \frac{\epsilon_{\mathrm{SiO_2}}}{t_{OX}/\kappa} \\ &= \kappa\left(\frac{\epsilon_{\mathrm{SiO_2}}}{t_{OX}}\right) \\ &= \kappa C_{OX} \end{aligned}$$

Capacitance

Before:

$$C_{gate} = C_{OX} \cdot A$$

After:

$$C'_{gate} = C'_{OX} \cdot A'$$
$$C'_{gate} = \kappa C_{OX} \cdot \frac{L}{\kappa} \cdot \frac{W}{\kappa}$$
$$C'_{gate} = \frac{C_{OX} \cdot A}{\kappa}$$
$$C'_{gate} = \frac{C_{gate}}{\kappa}$$

Thershold

Before:

$$V_{th} = \frac{1}{C_{OX}}\left(-Q_{eff} + \left(2\epsilon_{\mathrm{Si}} q N_a \left(\phi_s + V_{\text{s-sub}}\right)\right)^{1/2}\right) + \left(W_f + \phi_s\right)$$

$$\left(W_f + \phi_s\right) \approx 0$$

adjust $V_{\text{s-sub}}$ **so** $\left(\phi_s + V_{\text{s-sub}}\right) \rightarrow \frac{\left(\phi_s + V_{\text{s-sub}}\right)}{\kappa}$

After:

$$V'_{th} = \frac{1}{\kappa C_{OX}}\left(-Q_{eff} + \left(2\epsilon_{\mathrm{Si}} q \kappa N_a \frac{\left(\phi_s + V_{\text{s-sub}}\right)}{\kappa}\right)^{1/2}\right)$$

$$V'_{th} \approx \frac{V_{th}}{\kappa}$$

Current

Before:

Saturation $I_d = \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)(V_{gs} - V_{th})^2$

After:

Saturation
$$\begin{aligned} I'_d &= \frac{\mu C'_{OX}}{2}\left(\frac{W'}{L'}\right)\left(V'_{gs} - V'_{th}\right)^2 \\ &= \frac{\mu \kappa C_{OX}}{2}\left(\frac{W/\kappa}{L/\kappa}\right)(V_{gs}/\kappa - V_{th}/\kappa)^2 \\ &= \frac{I_d}{\kappa} \end{aligned}$$

Gate Delay

Before:

$$\tau_{gd} = \frac{CV}{I}$$

After:

$$\begin{aligned} \tau'_{gd} &= \frac{C'V'}{I'} \\ &= \frac{C/\kappa \cdot V/\kappa}{I/\kappa} \\ &= \frac{\tau_{gd}}{\kappa} \end{aligned}$$

Wire Delay

Before:

$$\tau_{wire} = R_L C$$

After:

$$\begin{aligned}
R'_L &= \rho \frac{L'}{W' \cdot t'} \\
&= \rho \frac{L/\kappa}{W/\kappa \cdot t/\kappa} \\
&= \kappa R_L \\
\tau'_{wire} &= R'_L C' \\
&= \kappa R_L \frac{C}{\kappa} \\
&= 1
\end{aligned}$$

Power Dissipation (Resistive)

Before:

$$P_r = VI$$

After:

$$\begin{aligned} P_r' &= V'I' \\ &= \left(\frac{V}{\kappa}\right)\left(\frac{I}{\kappa}\right) \\ &= \frac{P_r}{\kappa^2} \end{aligned}$$

Power Dissipation (Charging)

Before:

$$P_c = \frac{1}{2} C V^2 f$$

After:

$$\begin{aligned} P_c' &= \frac{1}{2} C' V'^2 f \\ &= \frac{1}{2} \frac{C}{\kappa} \left(\frac{V}{\kappa}\right)^2 f \\ &= \frac{P_c}{\kappa^3} \end{aligned}$$

Scaling

Direct features

Channel Length (L)	$\frac{1}{\kappa}$
Channel Width (W)	$\frac{1}{\kappa}$
Oxide Thickness (t_{OX})	$\frac{1}{\kappa}$
Doping (N_a)	κ
Voltage (V)	$\frac{1}{\kappa}$

Consequences

Capacitance C	$\frac{1}{\kappa}$
Threshold V_{th}	$\frac{1}{\kappa}$
Current (I_d)	$\frac{1}{\kappa}$
Gate Delay τ_{gd}	$\frac{1}{\kappa}$
Wire Delay τ_{wire}	1
Power P_d	$\frac{1}{\kappa^2}$
Power P_c	$\frac{1}{\kappa^3}$

Take Home Message for Scaling

As $\lambda_0 \rightarrow \lambda_1$:

- $\left(\frac{\lambda_1}{\lambda_0}\right)^2 A_0$
- $\tau_{gd} \rightarrow \left(\frac{\lambda_1}{\lambda_0}\right) \tau_{gd}$
- Circuit delay scales less than $\left(\frac{\lambda_1}{\lambda_0}\right)$ since
  - wire delays not scaling down
  - larger circuits usually imply longer wires
- Adding wire layers helps some