CS294-7: Reconfigurable Computing

Day 4: Thursday, January 28

- Admin
- What's an FPGA?
- How program?

Source for Xilinx and Altera component diagrams is their respective databooks.

Admin

- Anyone not signup for scribe?
- Room now: Soda 505
- Tuesday, February 11
  $\Rightarrow$ reschedule class to 5:00 PM in 405

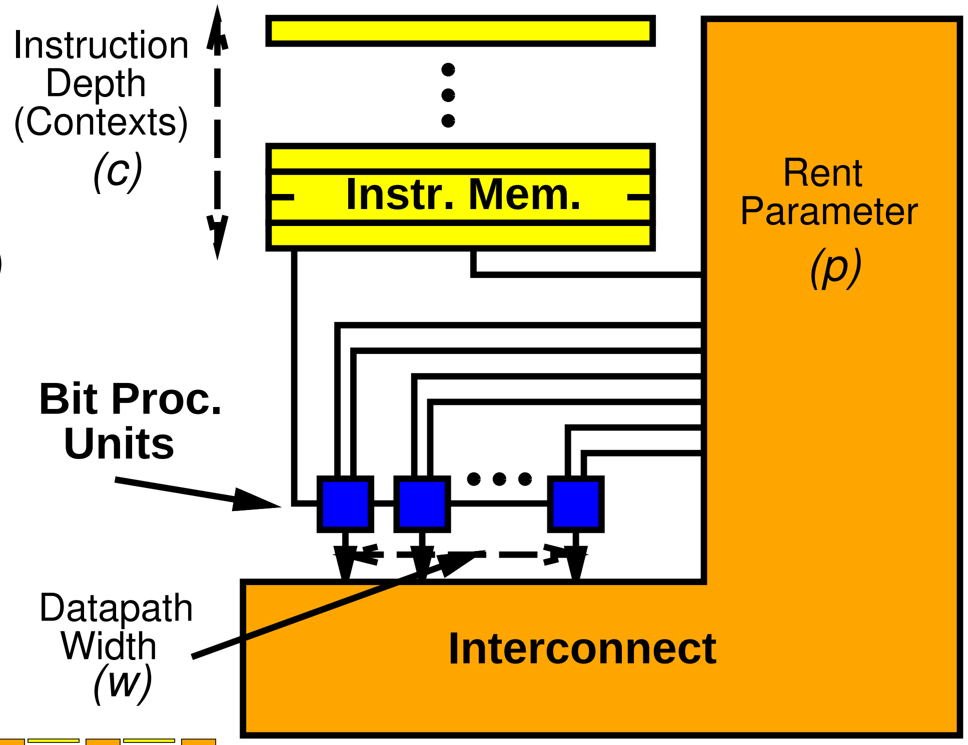
Today's Purposes

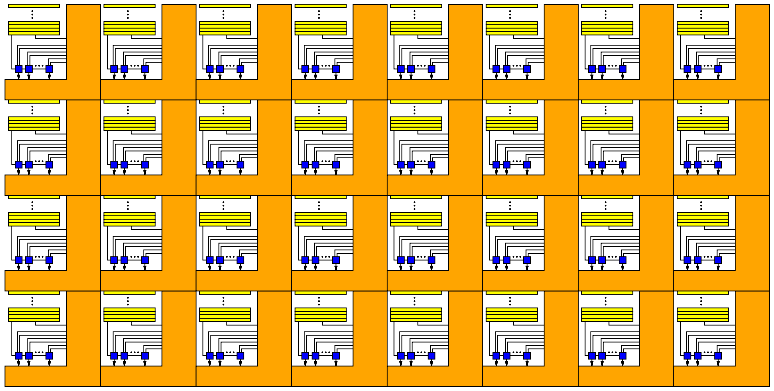
- Leveler — make sure everyone really knows what an FPGA is
- Preparation for Assignment 1 (assigned next class)
- Preparation for the next two lectures on FCCMs
  - PAM
  - SPLASH
- Concrete background before we dig into architecture details

Computing Device Composition $\Rightarrow$ FPGA

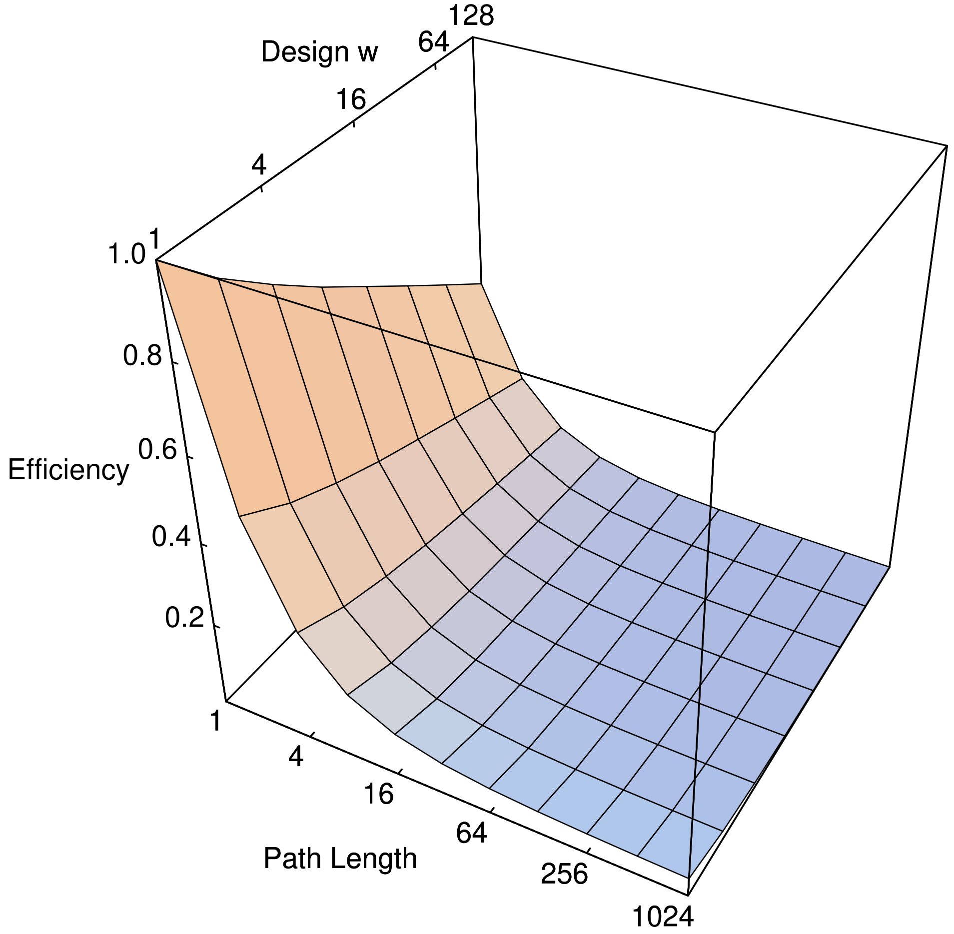
Composition:

- **Bit Processing Units**
  (4-LUT, $k = 4$, $w = 1$)
- **Interconnect**
  - **Spatial ($p = 0.5$?)**
  - **Temporal ($d = 1$)**
- **Instr. Memory ($c = 1$)**





FPGA Efficiency

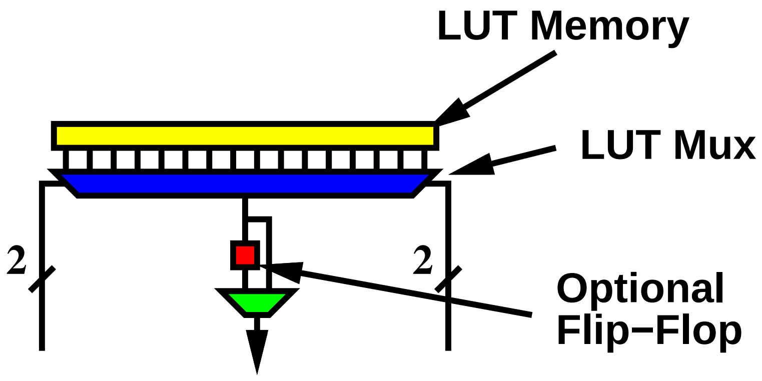


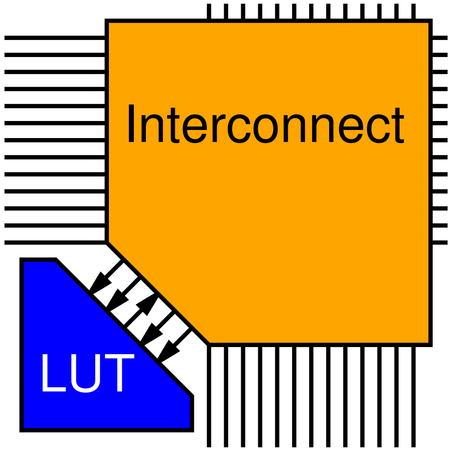
$$c = d = 1,\ w = 1$$

(at 16K Bit Processing Elements)

FPGA Compute

- 4-LUT (LUT = Look Up Table, $k = 4$)
- Optional FF on each output

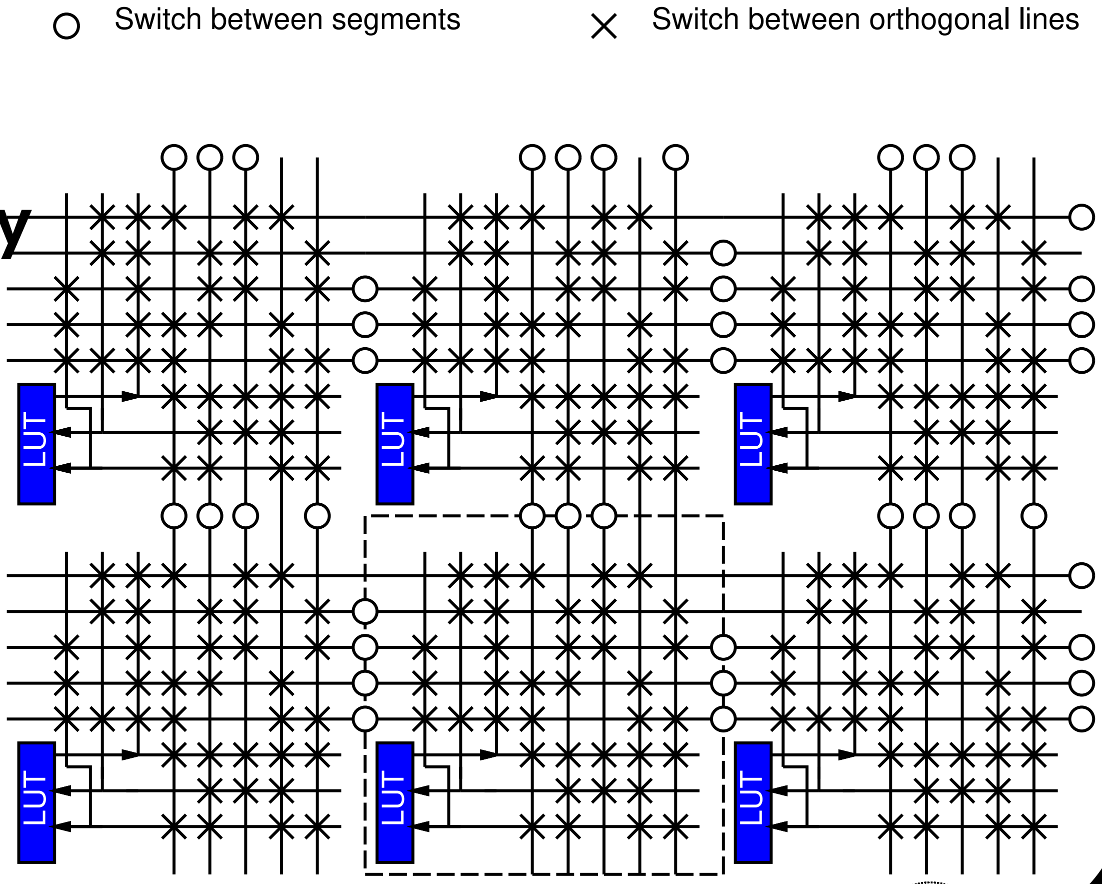




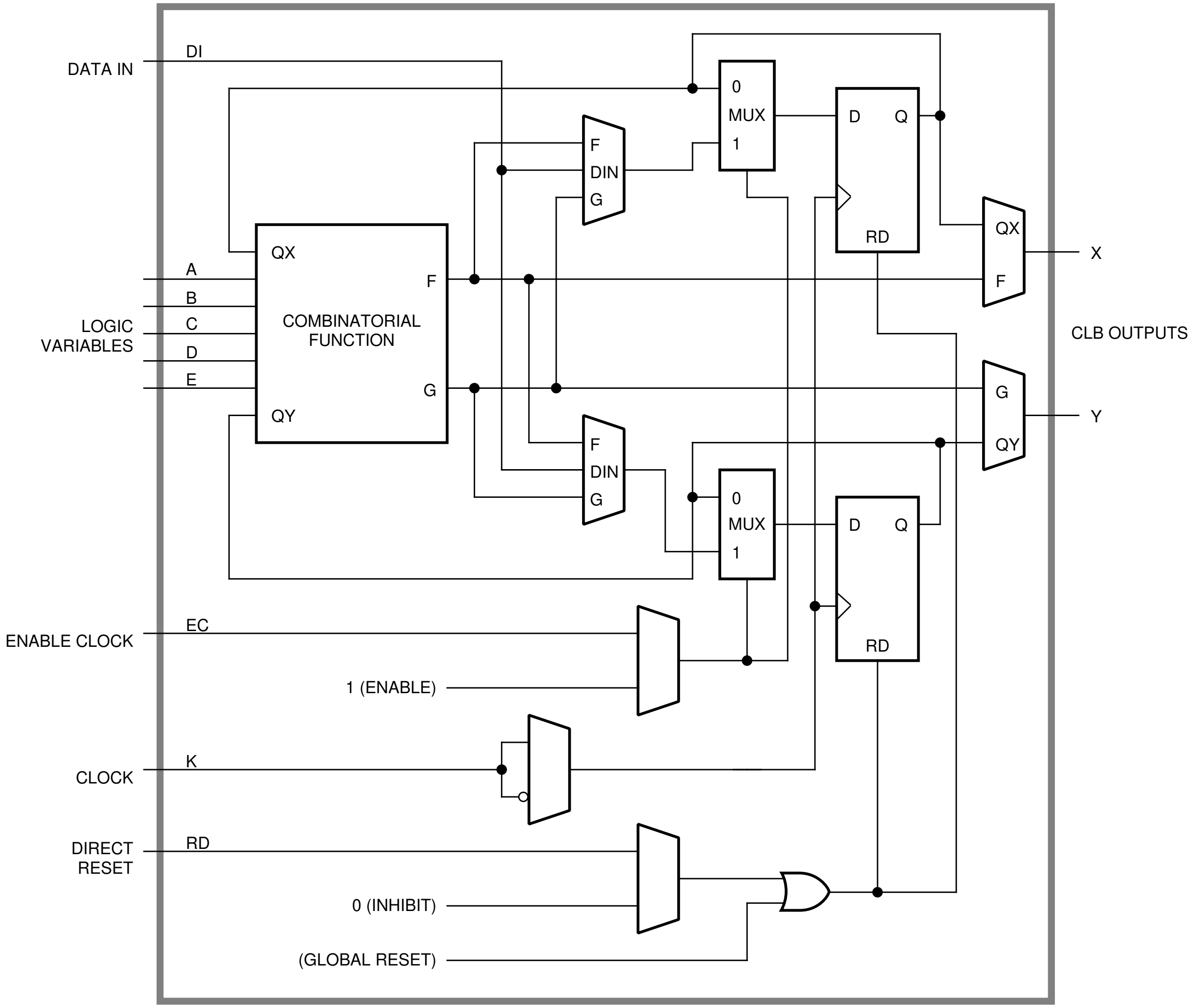
FPGA Interconnect

Interconnect has mix of:

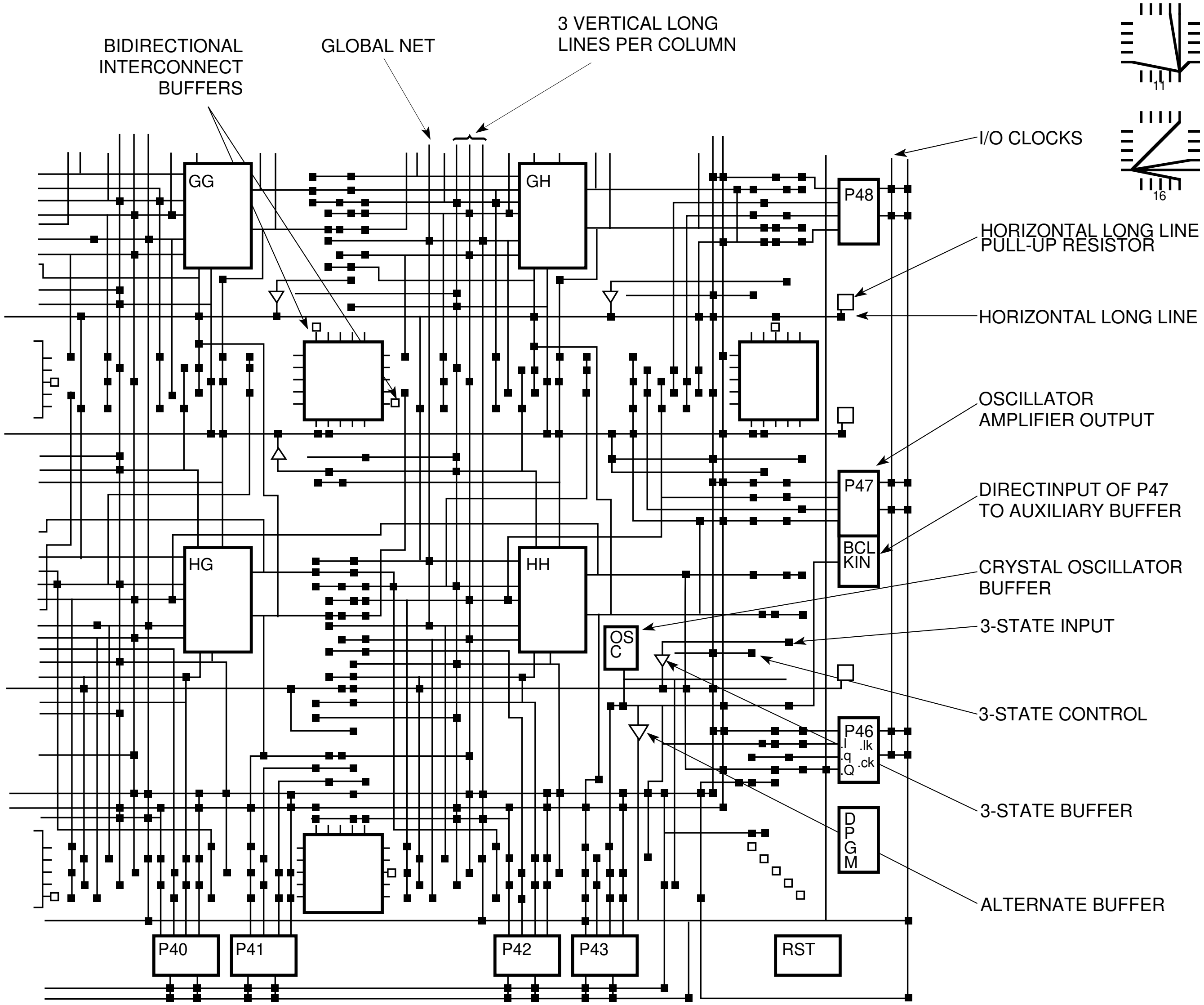
- short, local connections
- Hierarchical longer connections
- (limited) opportunity for corner turns
- opportunity to join segments

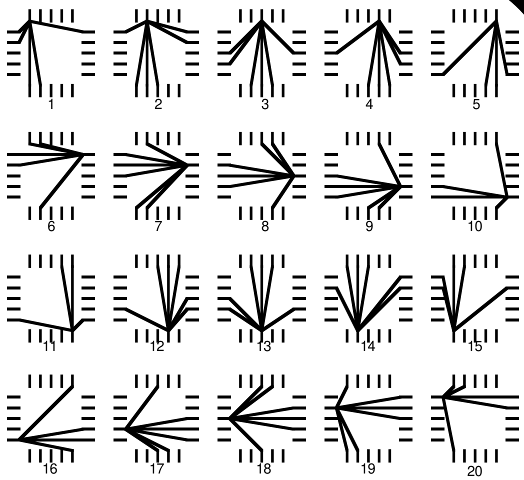


XC3000 Logic Block



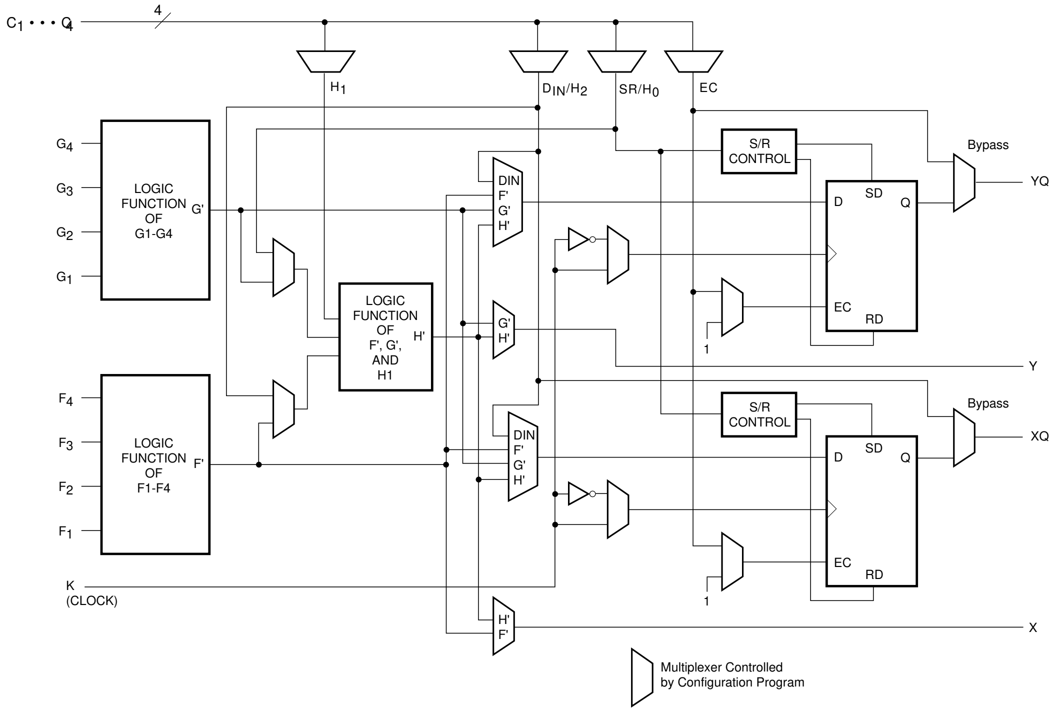
XC3000 Interconnect



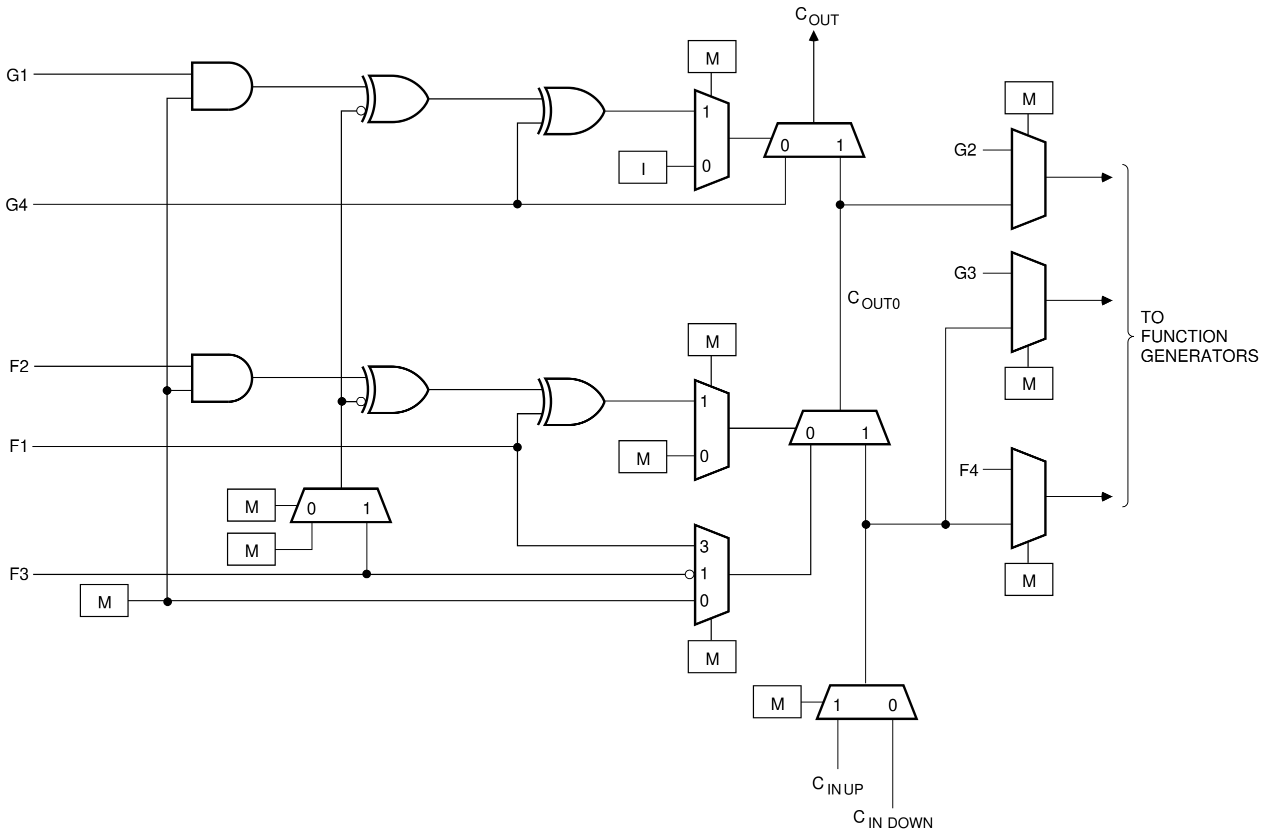


XC4000

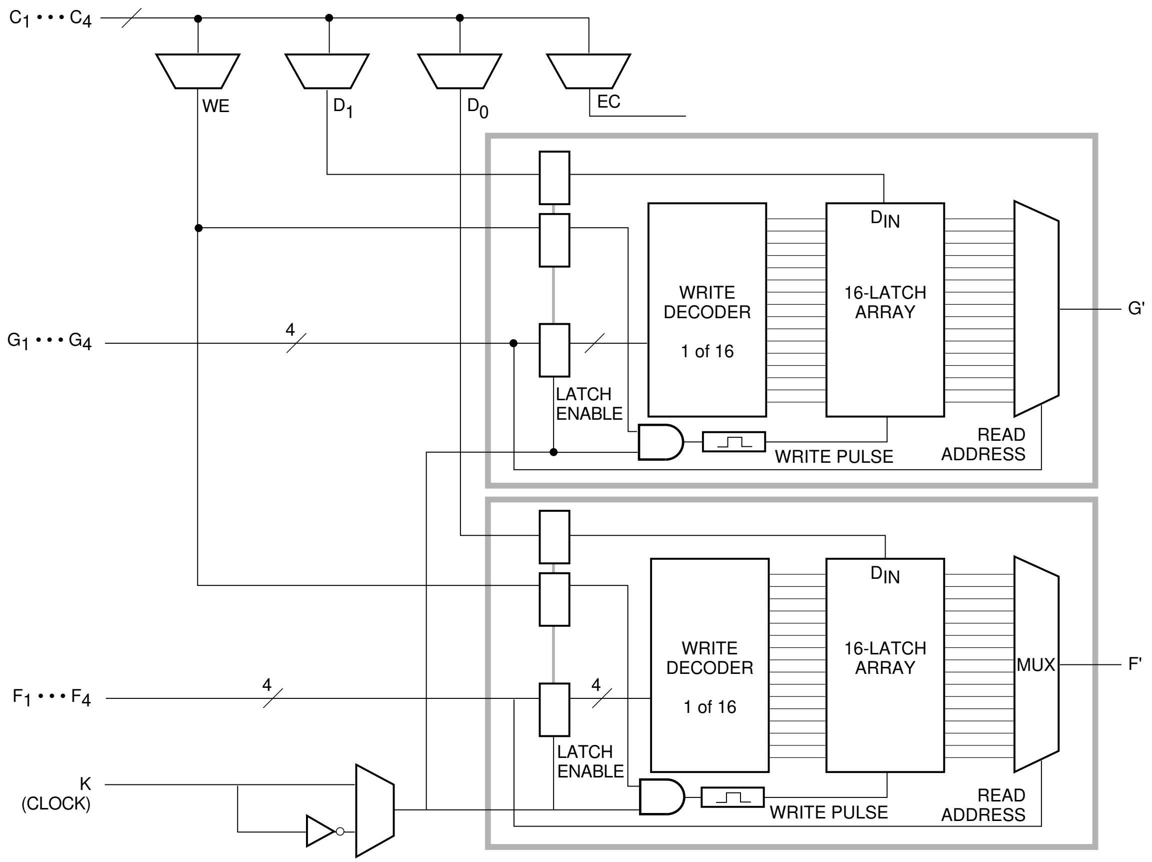
- Cascaded LUTs (2 4-LUT → 1 3-LUT)
- Fast Carry Logic
- LUTs as memory
- Serial programming (1b/50ns) (400 bits/CLB)



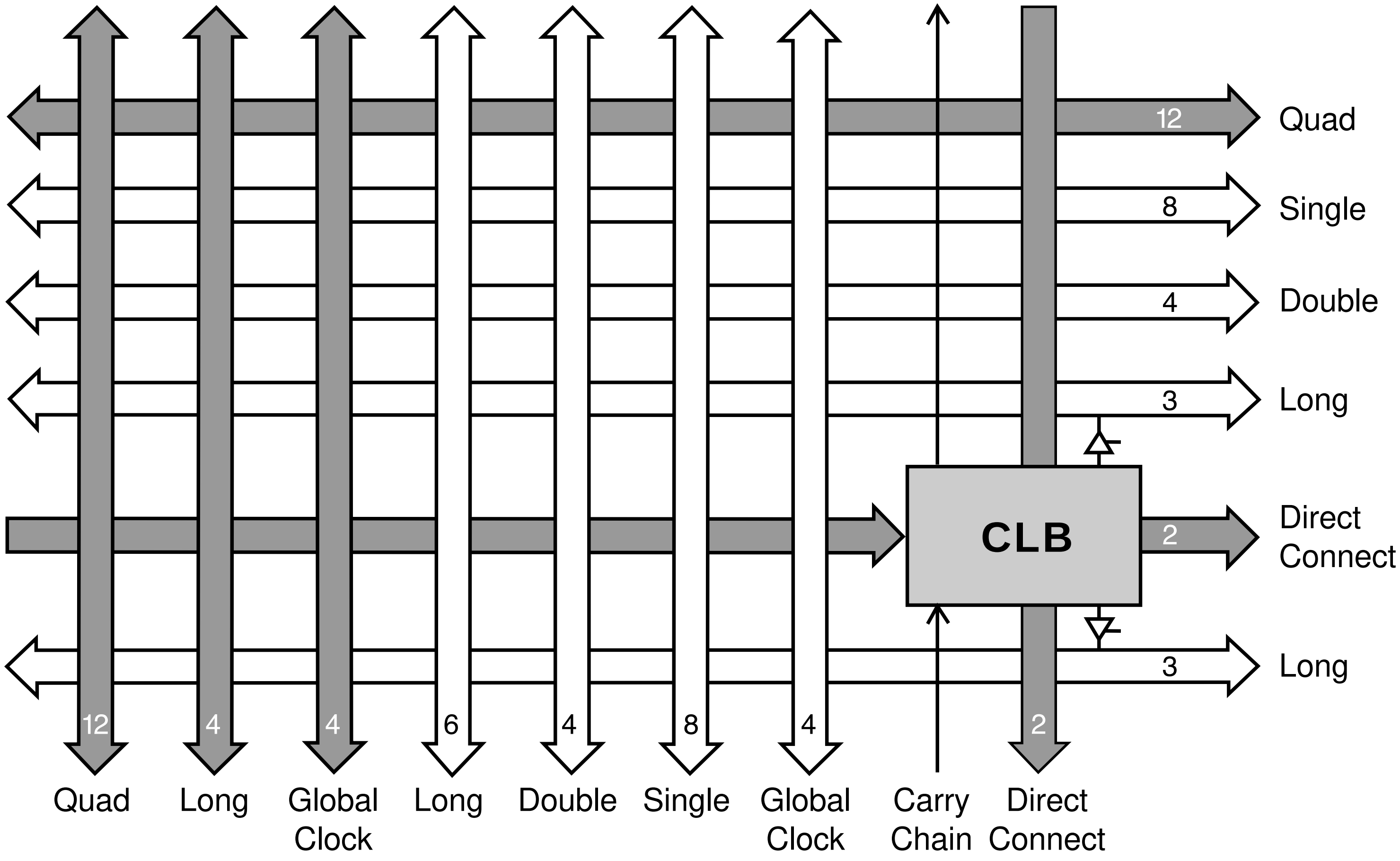
XC4000 – Carry Logic



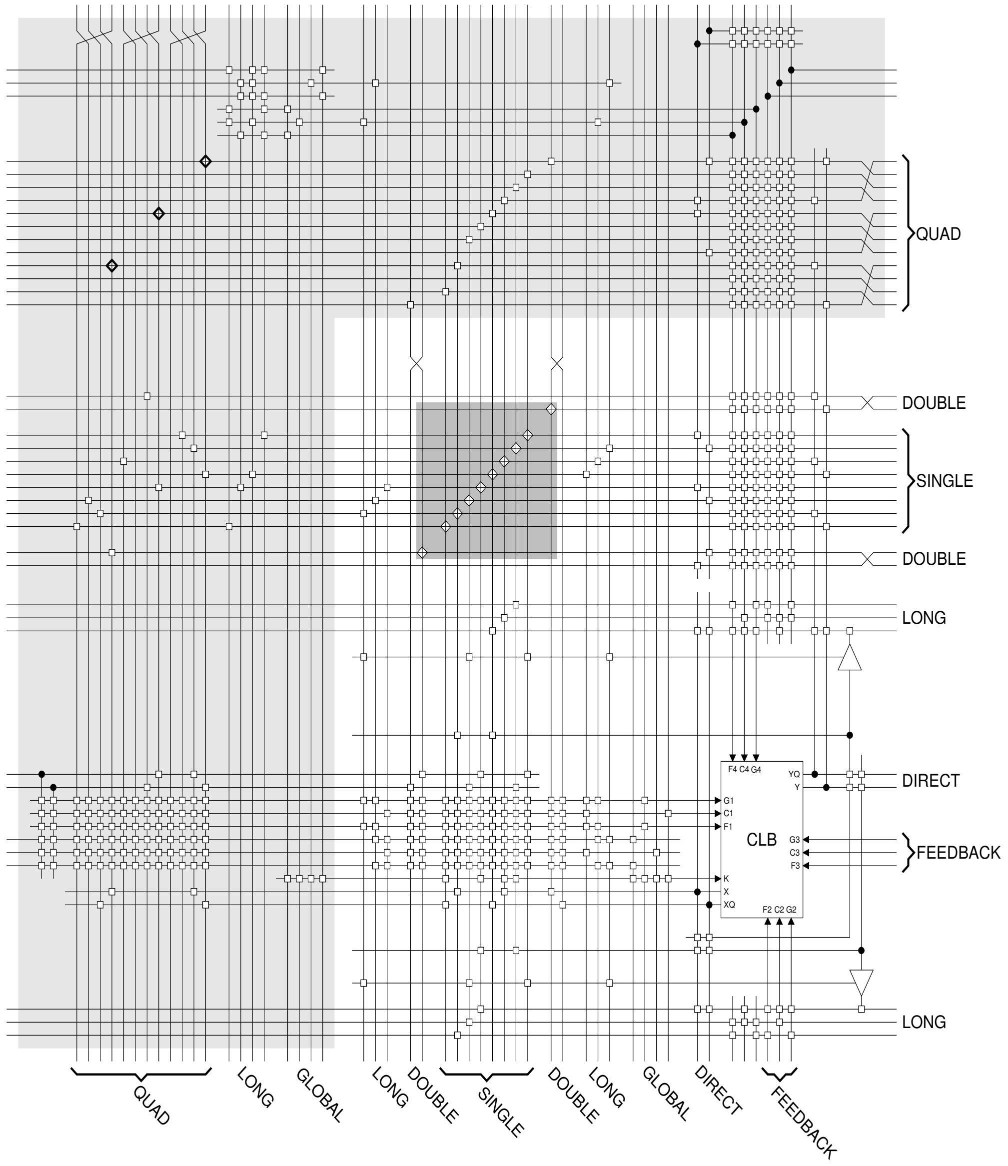
XC4000 – LUT Retiming



XC4000 – Interconnect



XC4000 – Interconnect Details



Common to XC4000E and XC4000EX

XC4000EX only

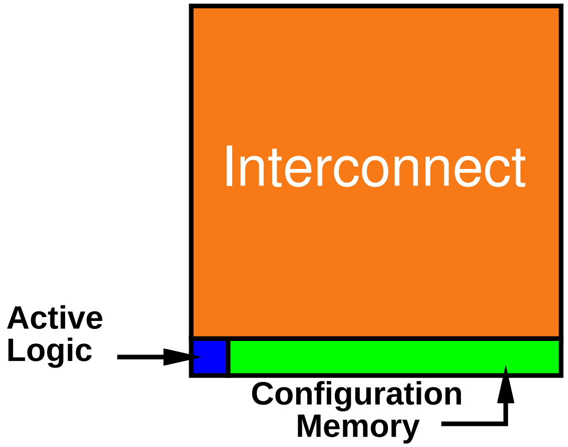
Programmable Switch Matrix

Areas and Times

Year	Design	Organization	Max	λ	λ^2 area	cycle
1986	Xilinx 2K	CLB (4-LUT)	100	1μ	500K	20 ns
1988	Xilinx 3K	CLB ($2\times$4-LUT)	320	0.6μ	1.3M	13 ns
1992	Xilinx 4K	CLB ($2\times$4-LUT +)	1024	0.6μ	1.25M	7 ns
1995	Xilinx 5K	CLB ($4\times$4-LUTS)	484	0.3μ	2.25M	6 ns
1995	Altera 8K	LE (4-LUT)	1296	0.3μ	920K	7.5 ns
1995	ORCA 2C	PLC ($4\times$4-LUT)	900	0.3μ	4.3M	7 ns
–	Model	4-LUT	512	–	650K	–
–	Model	4-LUT	2048	–	800K	–
–	Model	4-LUT	4096	–	880K	–
–	Model	4-LUT	16K	–	1M	–

Area Breakdown (from Model)

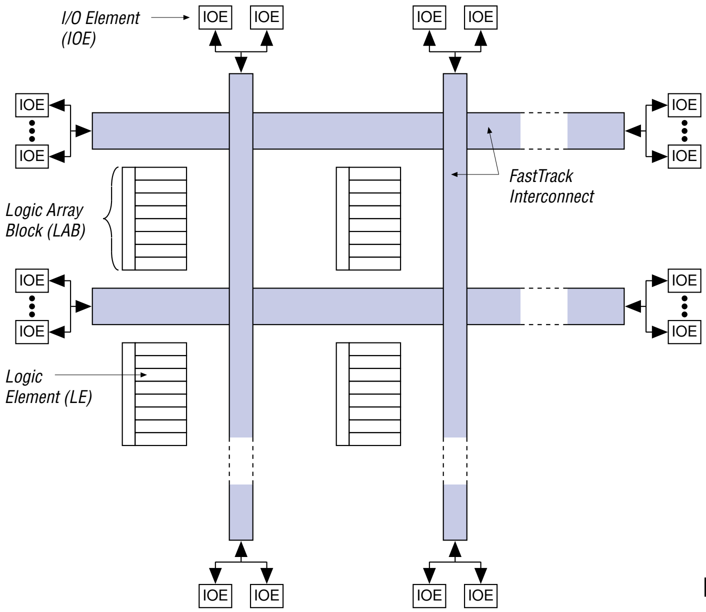
$$A_{bit\_elm} = A_{fixed} + \underbrace{N_{SW}(N_p, w, p) \cdot A_{SW}}_{\textbf{interconnect}}$$
$$+ \underbrace{\left(\frac{c}{w}\right) \cdot n_{ibits} \cdot A_{mem\_cell}}_{\textbf{instruction memory}}$$
$$+ \underbrace{d \cdot A_{mem\_cell}}_{\textbf{retiming memory}}$$



Function	Area (λ^2)
LUT MUX + ff	20K (generous, closer to 10K)
Programming Memory	80K (240K typical unencoded)
Interconnect	700K (for $N_p = 2048$)

Delay Breakdown

Design	Path	Total Delay	LUT Delay	Inter. %
Altera 8K	LUT-local-LUT	2.5 ns	2 ns	20%
	LUT-row-local-LUT	7.5 ns	2 ns	73%
	LUT-row-column-local-LUT	10.5 ns	2 ns	81%
DPGA	LUT-LUT (in subarray)	3.5 ns	1.5 ns	60%
	LUT-xbar-LUT	7 ns	1.5 ns	80%



FPGA Programming

$\Downarrow$

Technology Independent Mapping

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LUT Mapping

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CLB Collation

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Placement

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Routing

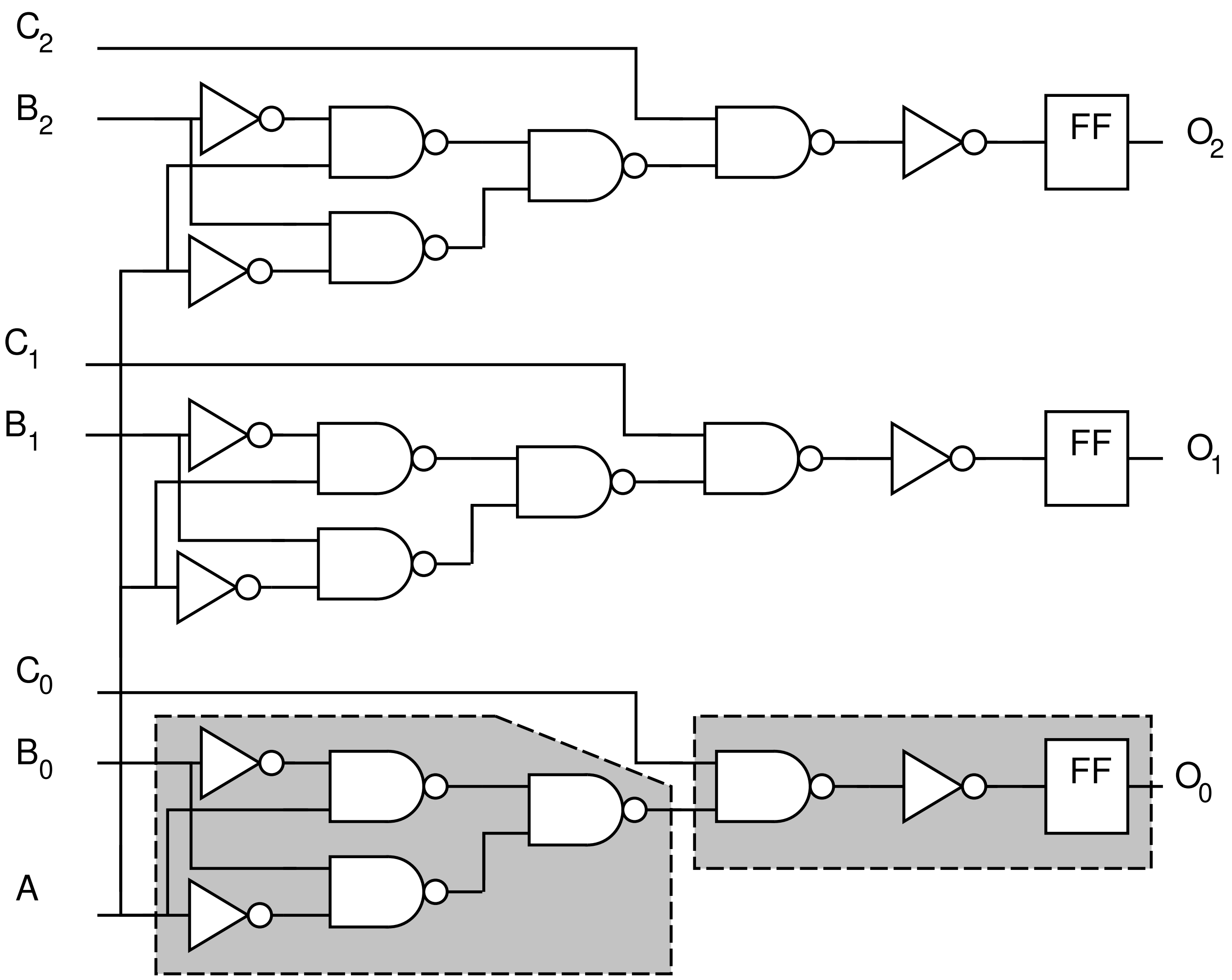
$\Downarrow$

(Bitstream Generation)

Technology Independent

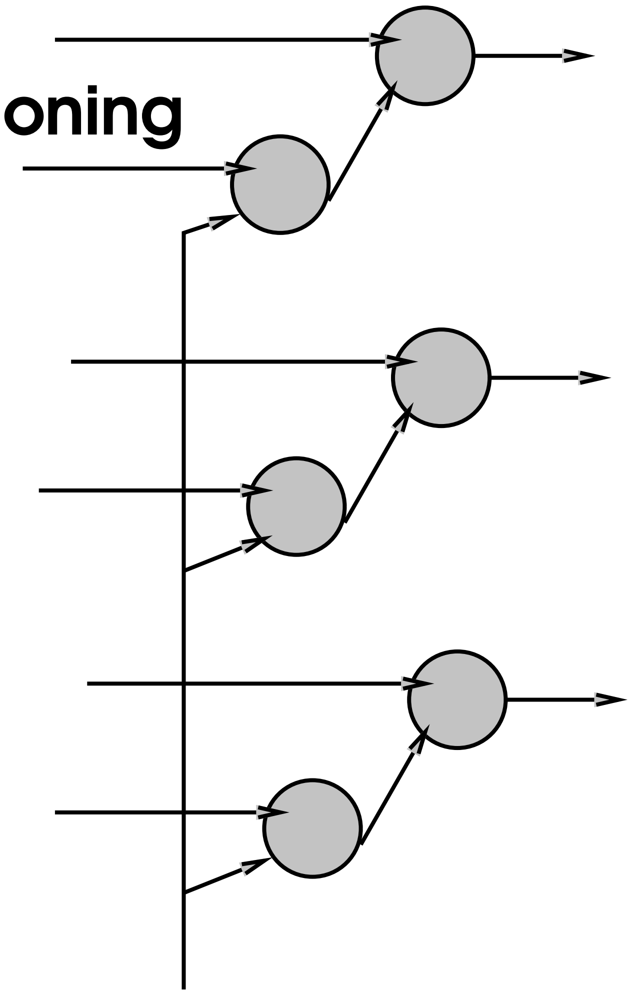
- Use standard tools (SIS, Synopsys)
- FPGA-specific cost model
- May map to macro/library elements
- Style differences
  - already paid for FFs
  - pipelining less (relative) expense than gate-array/custom
  - one-hot encoded FSMs generally preferable

LUT Mapping



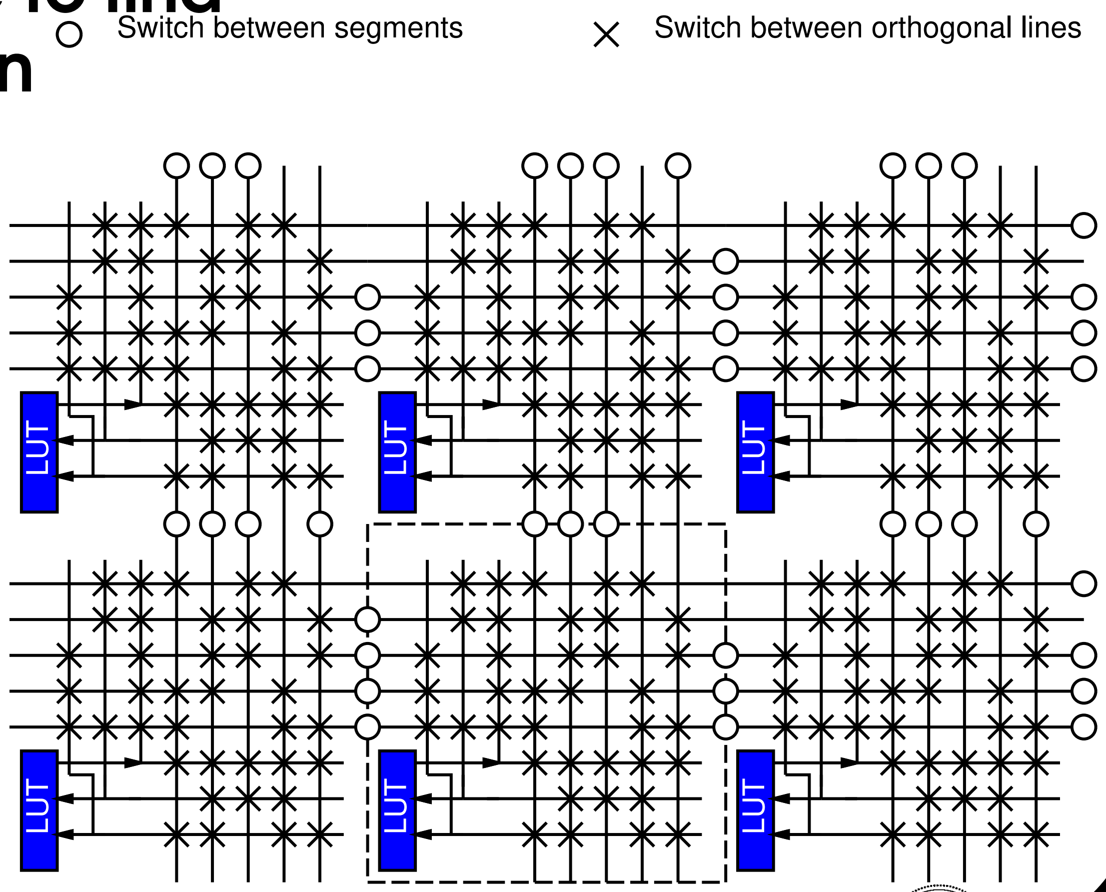
Placement

- Typically start with min-cut partitioning (minimize wiring bandwidth)
- Constraint satisfaction problem
  - maximize locality
  - match wiring resources
  - (avoid congestion)
  - minimize delay
- Usually attack with simulated annealing



Routing

- Global route to assign channels
- Detail route to make connection
- Can take long time to find acceptable solution
  - density of CSP solutions
  - longer as more constrained
  - easier if sparsely used or well placed
  - running times: 10s of minutes to hours



Summary

- Reviewed LUT-based FPGA Architectures
- Looked at traditional FPGA mapping
- Interconnect
  - Area
  - Delay
  - Mapping difficulty
- **Next Two Lectures:**
  Machines which use these devices to compute