CMOS Transistors

Introduction to Computer Systems, Fall 2022

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When poll is active, respond at **pollev.com/tqm**

Text **TQM** to **37607** once to join

How familiar are you with E&M concepts like voltage, current & charge?

- I am very familiar with these topics
- I am somewhat familiar with these topics
- I am neither particularly familiar or unfamiliar with these topics
- I am somewhat unfamiliar with these topics
- I am very unfamiliar with these topics
- I have never taken a class or studied these topics
- I prefer not to say

Logistics

- HW00 Binary Quiz: **This Friday** 9/16 @ 11:59 pm
  - Quiz On Canvas
  - Should have everything you need

- Chek-in01: Due this Monday @ 4:59 pm
  - To be released Thursday

- HW01 bits.c: to be released sometime this week
  - Will require VM setup (also to be released soon)
  - Has you "program" in C
  - Should have everything needed form lectures
    - VM Stuff will have information in the HW1 specification & recitation

Lecture Outline

- **Physics Background**
- CMOS Transistor
- CMOS Logical Circuits
- CMOS Circuit Design

Disclaimer:

- This course is NOT assuming you know E&M Physics
  - It may help to have some background
  - I am going to give a VERY simplified view of E&M Physics

- If you want to know more of the details with transistors & how they work, courses like ESE 2150 (Electrical Circuits and Systems) may appeal to you

Charge, Current, Voltage

This is a big simplification

- Charge can be either positive or negative
  - Electrons are common units of negative charge and can move through conductive material
  - Like charges repel, opposite charges attract

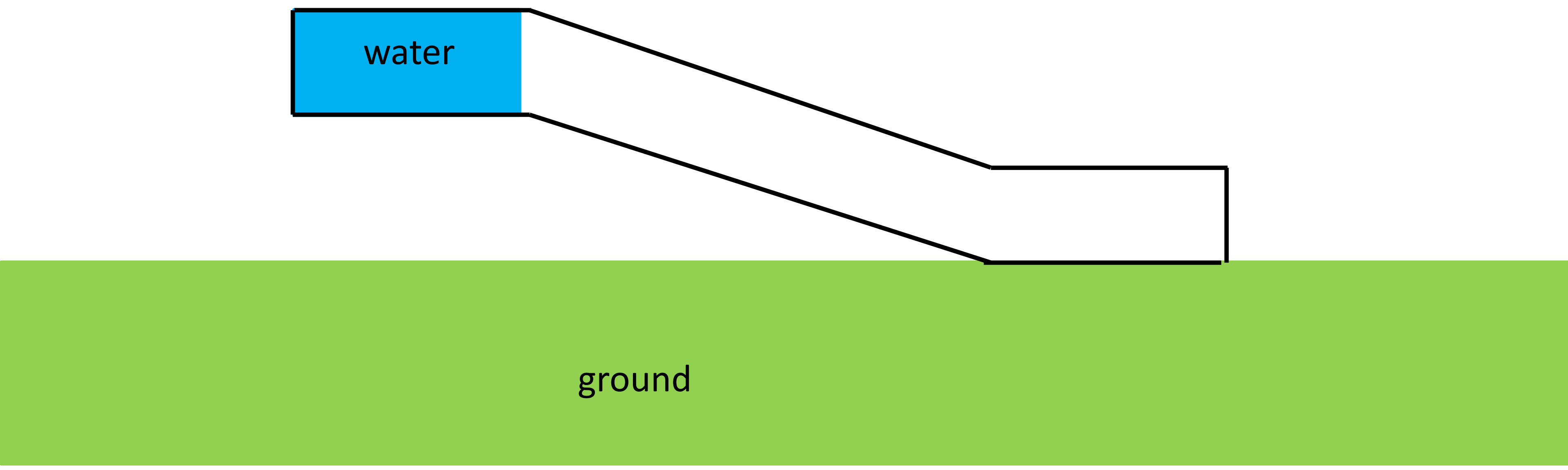
- Current: the rate of flow of positive charge

- Voltage: Positive charge want to move from places with high voltage to lower voltage
  - (vice versa for negative charge)
  - sometimes called “electric pressure”
  - Measured relative to a reference point (usually called “ground”)

Voltage & Current Analogy

This is a big simplification

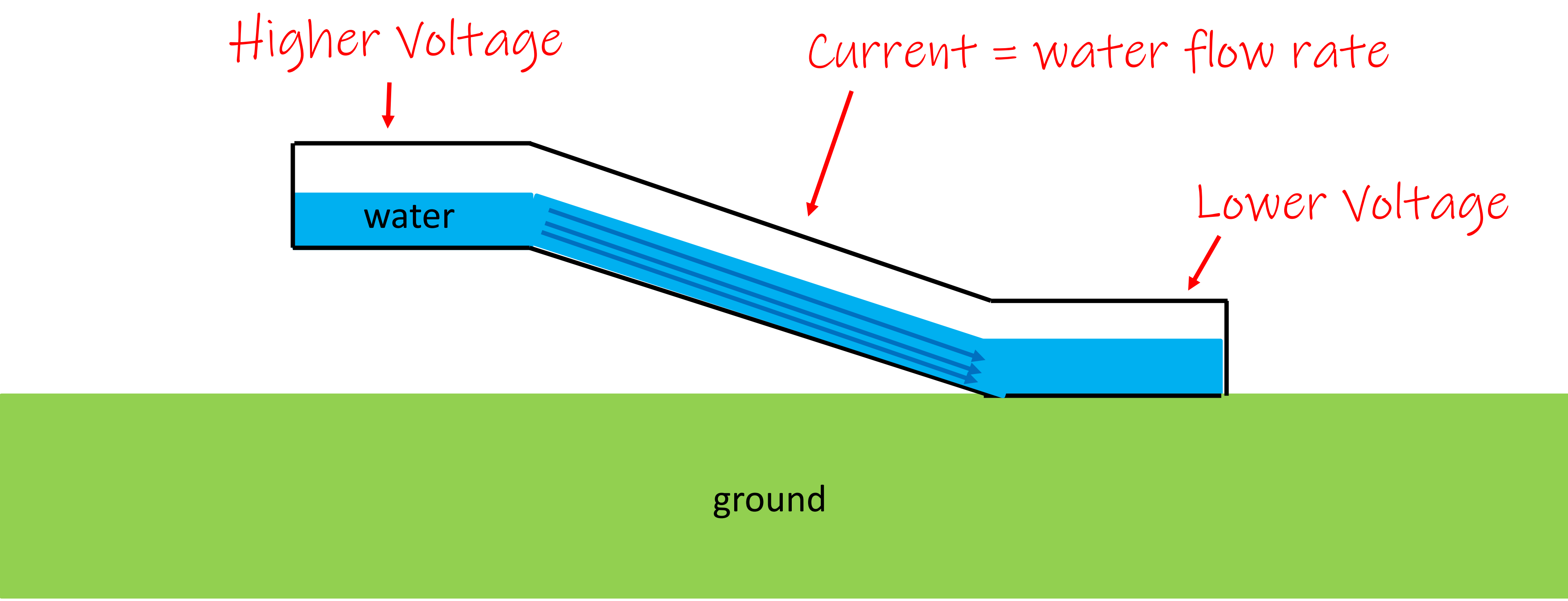
- Imagine we have a slanted pipe
  - One end on the ground, the other end is in the air
  - Water is placed in the high end of the pipe
  - What happens next?



Voltage & Current Analogy

This is a big simplification

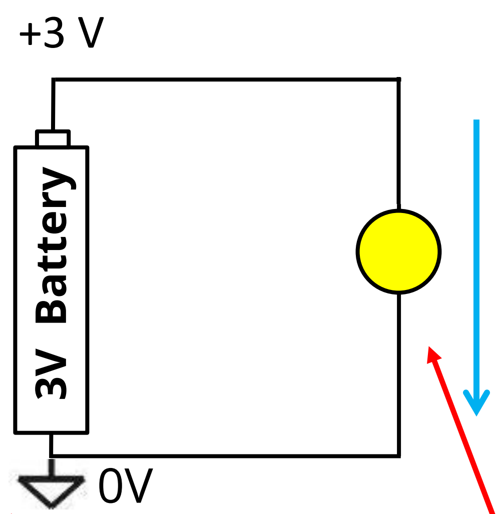
- Water flows to the bottom!
  - The water can be thought of positive charge
  - Positive charge moves form higher voltage to lower voltage



Circuit example

- Consider the following example circuit

Battery creates a voltage difference



Current flows from higher voltage to lower voltage.

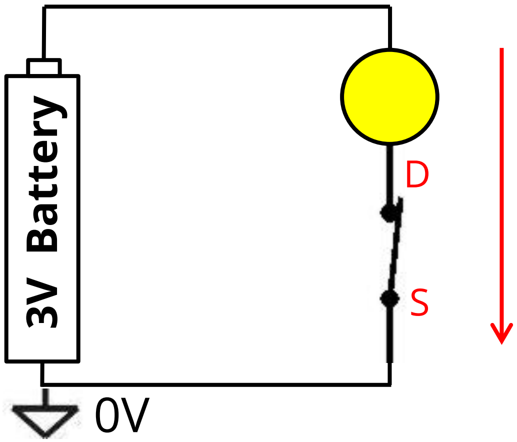
This indicates our refence for 0 volts called "ground"

Current passes through a lightbulb, turning it on

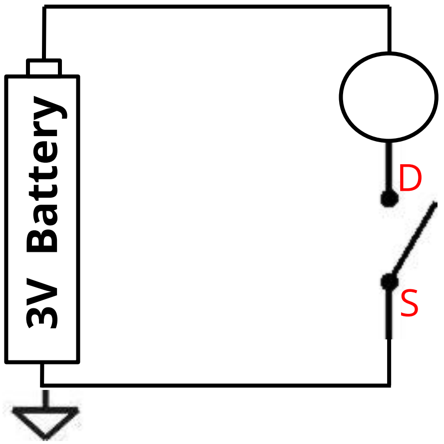
Circuit example w/ Switch

- Circuits can also have a switch
  - The switch can be open or close

If the switch is closed, charge can flow through like it is a wire

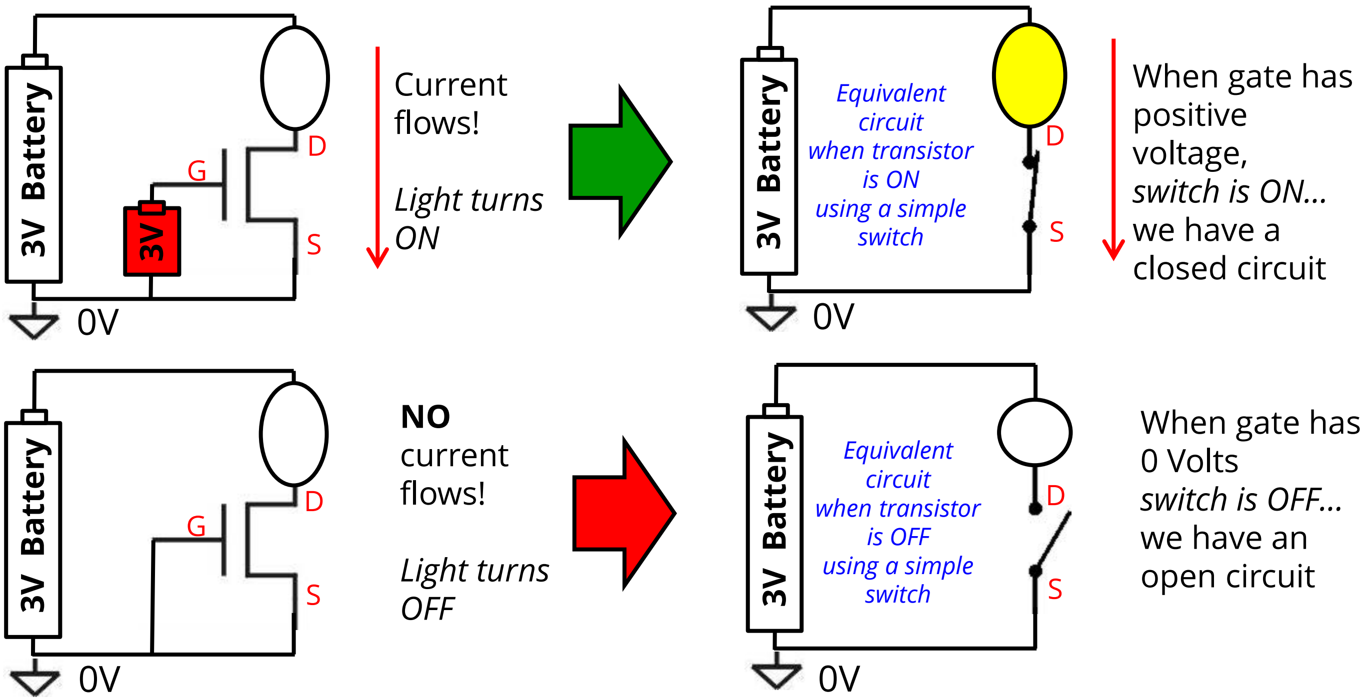


If the switch is open, charge cannot flow through



What Is a Transistor (MOSFET Type)?

- An electrical device that acts as an **electrical switch**; it's typically made from Silicon
  - 3 electrical contacts/terminals: Gate, Drain, Source
  - *Gate* controls flow of current between *Drain* and *Source* terminals; this style transistor is called a MOSFET

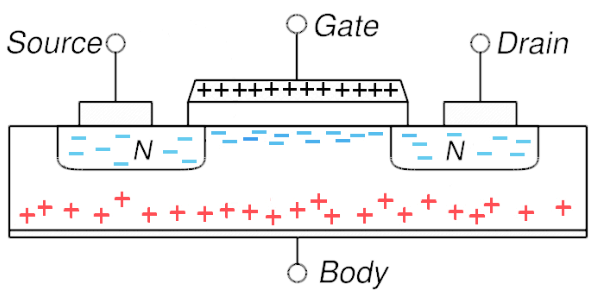


Lecture Outline

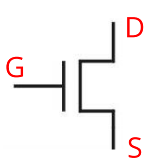
- Physics Background
- **CMOS Transistor**
- CMOS Logical Circuits
- CMOS Circuit Design

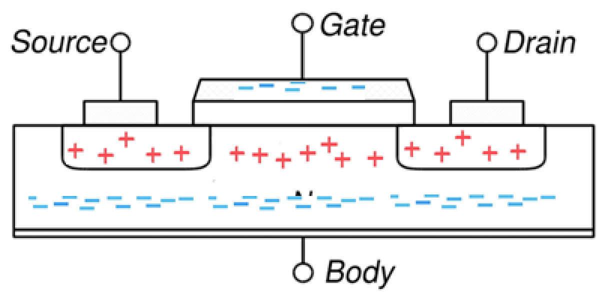
Two Types of MOSFET

- nMOS
  - **GATE Voltage MUST BE > Body, Source, Drain to be ON**
  - **(voltage must be high)**
- pMOS
  - **GATE Voltage MUST BE < Body,Source, Drain to be ON**
  - **(Voltage must be low)**

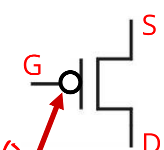


nMOSFET





pMOSFET

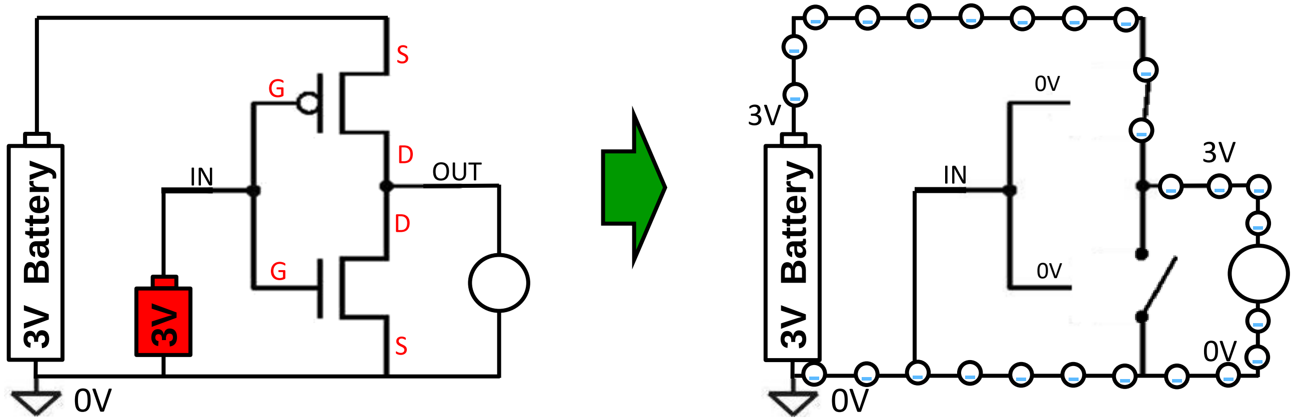


Do not forget to draw the circle.

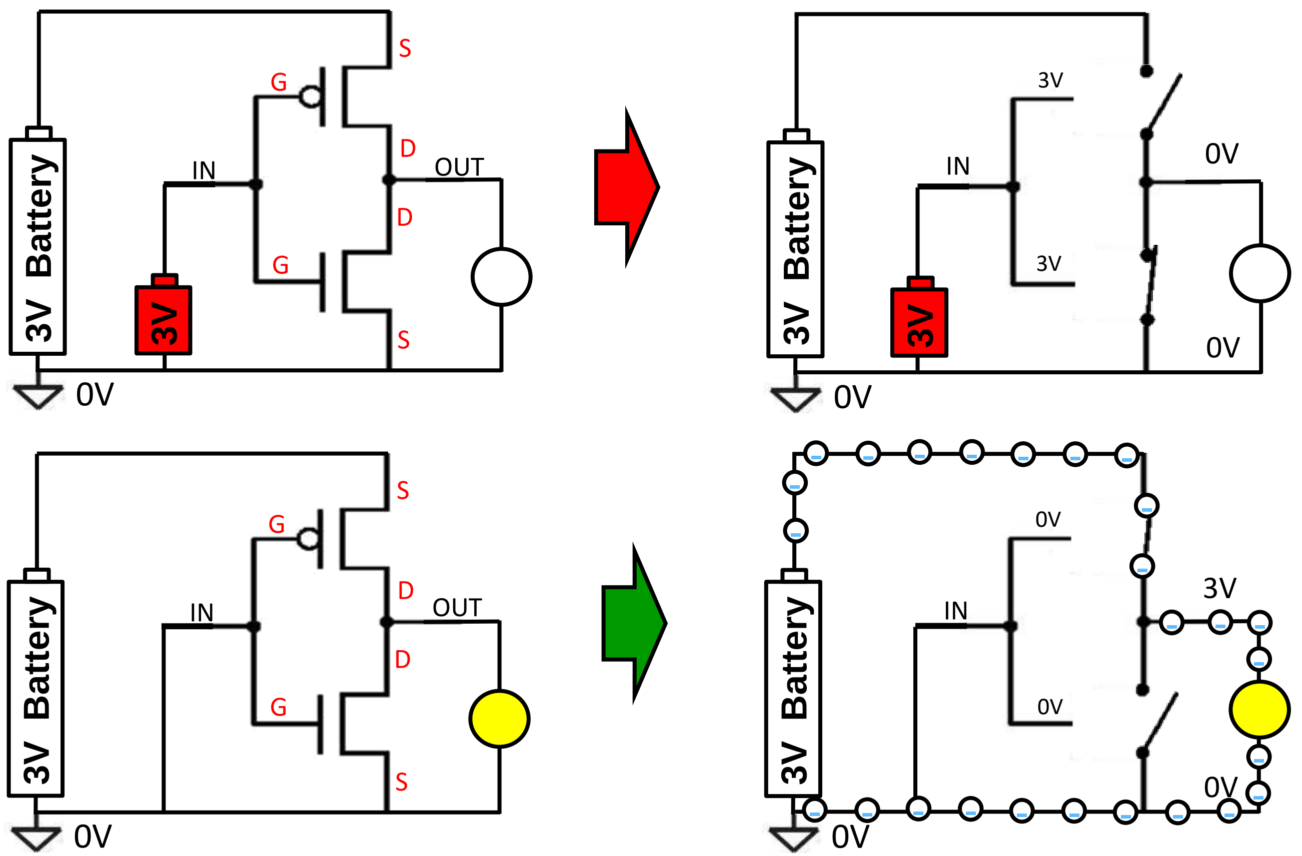
CMOS: pMOSFET & nMOSFET in Complement

3V on the input (the gates) turns the light OFF!

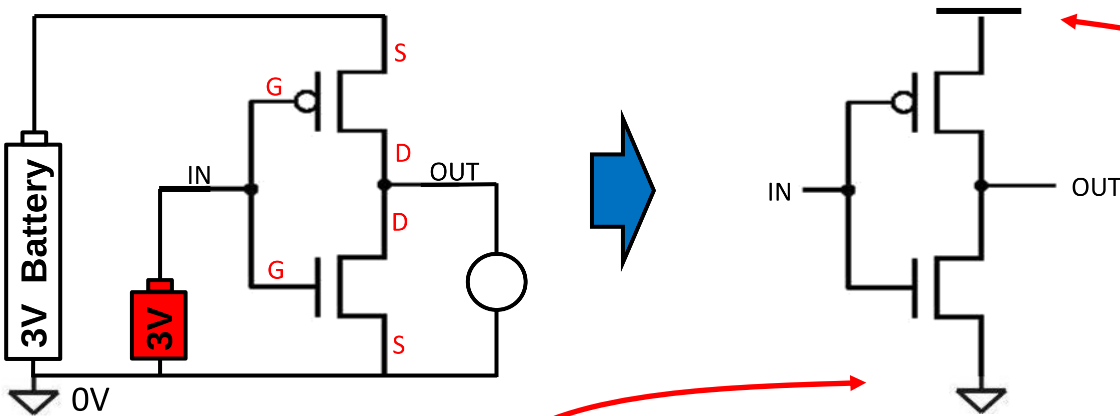
- What if the input is set to 0V?
  - 0V turns NMOS **OFF**
  - 0V turns PMOS **ON**
  - **Light has “3V” across it!**
  - Current flows in this circuit, so light turns **ON**!



CMOS: pMOSFET & nMOSFET in Complement

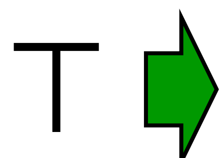


More Common Electrical Symbols

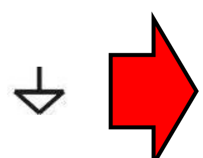


Circuit Drawings so far

Standard notation to use going forward



High Voltage
(3V, Vdd, etc)



Low Voltage (0V),
typically ground
(GND)

Lecture Outline

- Physics Background
- CMOS Transistor
- **CMOS Logical Circuits**
- CMOS Circuit Design

Voltages as Bits

- Transistors are the basis for all digital electronics
  - We've seen that they work by controlling the flow of charge

- We can map bits onto different voltages:
  - High voltage – we'll call this state "1"
  - Low voltage – we'll call this state "0"

**Only two relevant voltages

Computers use transistors as switches to manipulate bits
- Before transistors: tubes, electro-mechanical relays (pre 1950s)
- Mechanical adders (punch cards, gears) as far back as mid-1600s

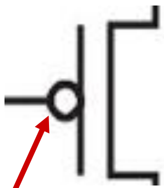
CMOS Transistors Simplified

nMos

Input	Output
1	Connected
0	Dis-connected

CMOS Transistors Simplified

pMos

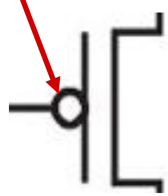


Circle = "negation"

Input	Output
1	Dis-connected
0	Connected

CMOS Transistors Simplified

Circle = "negation"



pMos

Input	Output
1	Dis-connected
0	Connected

nMos

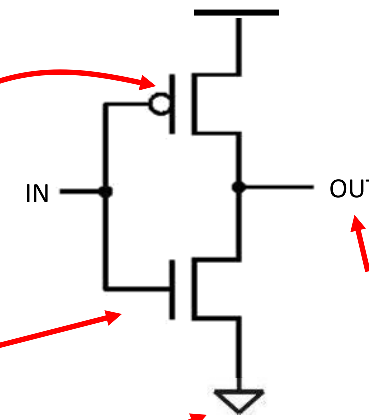
Input	Output
1	Connected
0	Dis-connected

CMOS Circuits as Logical Circuits

- Instead of thinking of voltages, we can analyze our circuit think of in terms of bits "1" or "0"

Vdd - 1 "source"

- Consider our previous circuit:
  - Output is the same as whatever "source" it is connected to
  - pMOS: on when input is low
  - nMOS: on when input is high



Output can only be connected to one "source" at a time

GND - 0 "source"

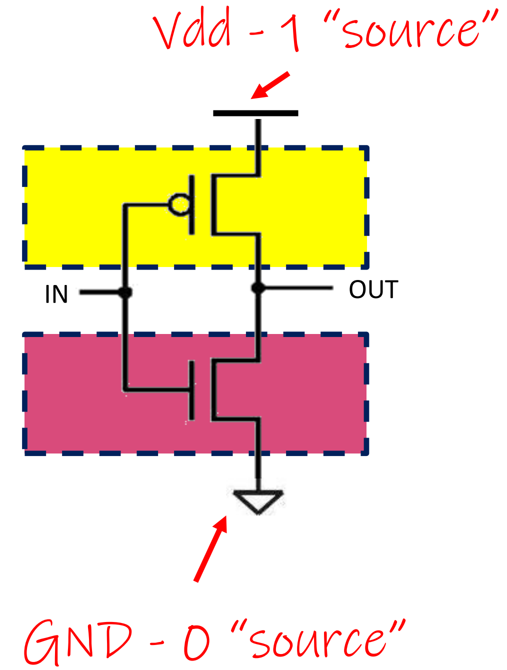
- Truth Table

Input	pMOS State	nMOS state	Output
1	Disconnected	Connected	0
0	Connected	Disconnected	1

This is the same as a "NOT" operation

PUN & PDN

- We can split our "NOT" circuit into two halves:
- Pull Up Network (PUN)
  - "Pulls" the output "Up" to "1"
  - **<u>Can only contain pMOS Transistors</u>**
- Pull Down Network (PDN)
  - "Pulls" the output "down" to "0"
  - **<u>Can only contain nMOS Transistors</u>**



- Output can only be connected to "1" or "0" at any time
  - **<u>Exactly one</u>** of PUN or PDN can be "ON" at a time
- We will see more complex examples in a moment

nMOS & pMOS in PUNs & PDNs

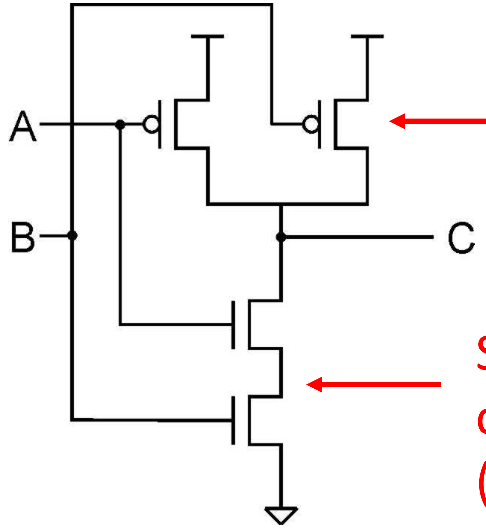
- **In a digital circuit there are only two relevant voltage levels, the low voltage level, GND (0), and the high voltage level, Vdd (1).**
  - An nMOS transistor is only ON when the gate voltage is **higher** than the source and drain voltages
  - A pMOS transistor is only ON when the gate voltage is **lower** than the source and drain voltages
- Therefore, an nMOS transistor can only be used to pass a low voltage and a pMOS transistor can only be used to pass a high voltage

- nMOS can only be used for the PDN
- pMOS can only be used for the PUN

The NAND (NOT-AND) Circuit

- NAND == NOT AND == ~(A & B)

Note: parallel structure on top, series on bottom



NAND Transistor Level

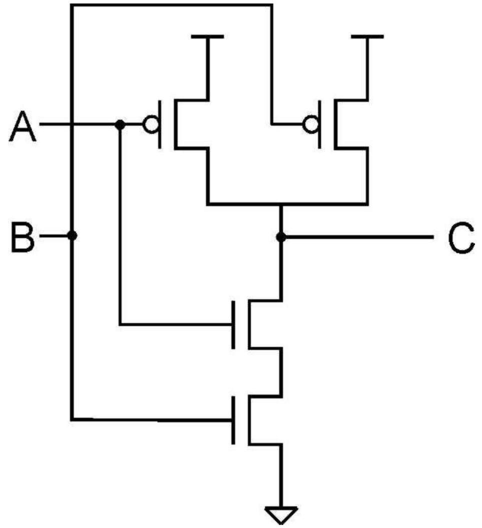
Parallel Transistors: only one needs to be on for a connection to be made across them
(Similar to using an OR)

Series Transistors: BOTH need to be on for a connection to be made across them
(Similar to using an AND)

The NAND (NOT-AND) Circuit

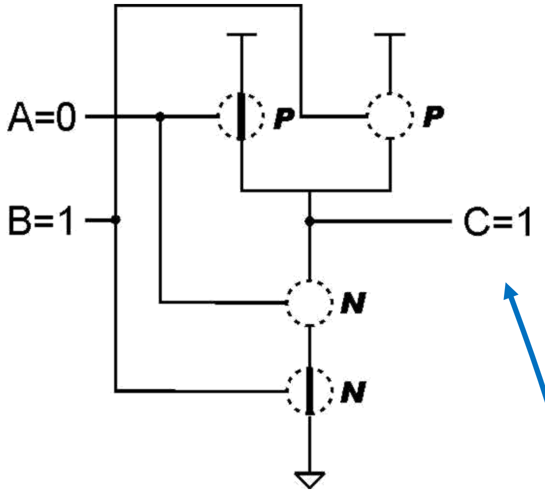
- NAND == NOT AND == ~(A & B)

Note: parallel structure on top, series on bottom



NAND Transistor Level

Sample Input: A=0, B=1



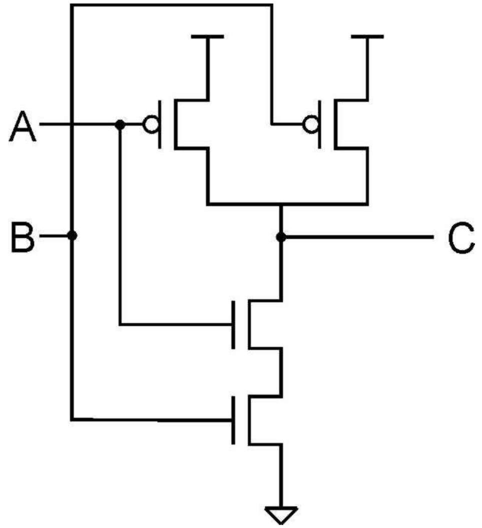
NAND Truth Table

A	B	C
0	0	1
0	1	1
1	0	1
1	1	?

The NAND (NOT-AND) Circuit

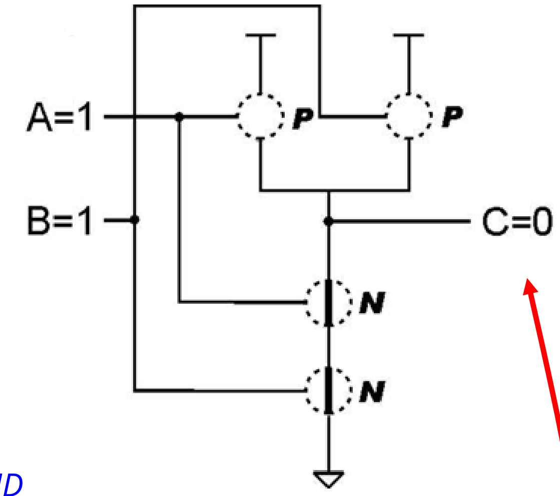
- NAND == NOT AND == ~(A & B)

Note: parallel structure on top, series on bottom



NAND Transistor Level

Sample Input: A=1, B=1

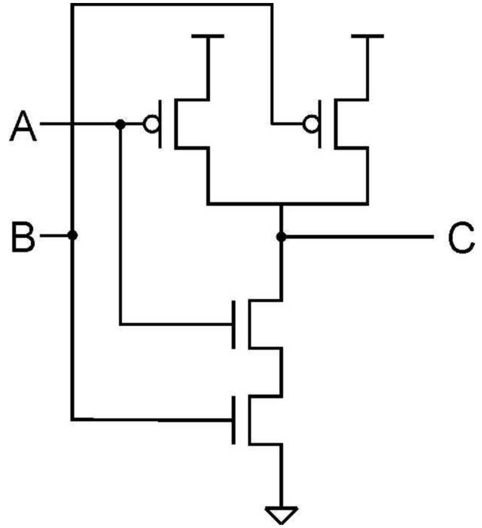


NAND Truth Table

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

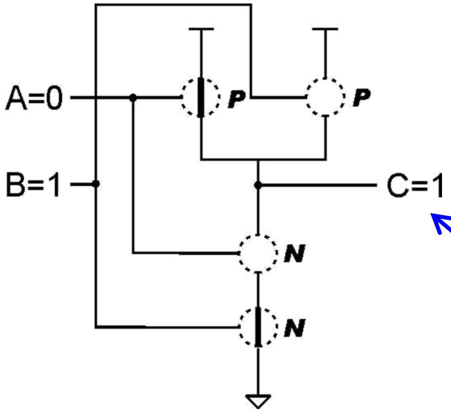
The NAND (NOT-AND) Circuit

Note: parallel structure on top, series on bottom



NAND Transistor Level

Sample Input: A=0, B=1



A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

NAND Gate Truth Table

Poll Everywhere

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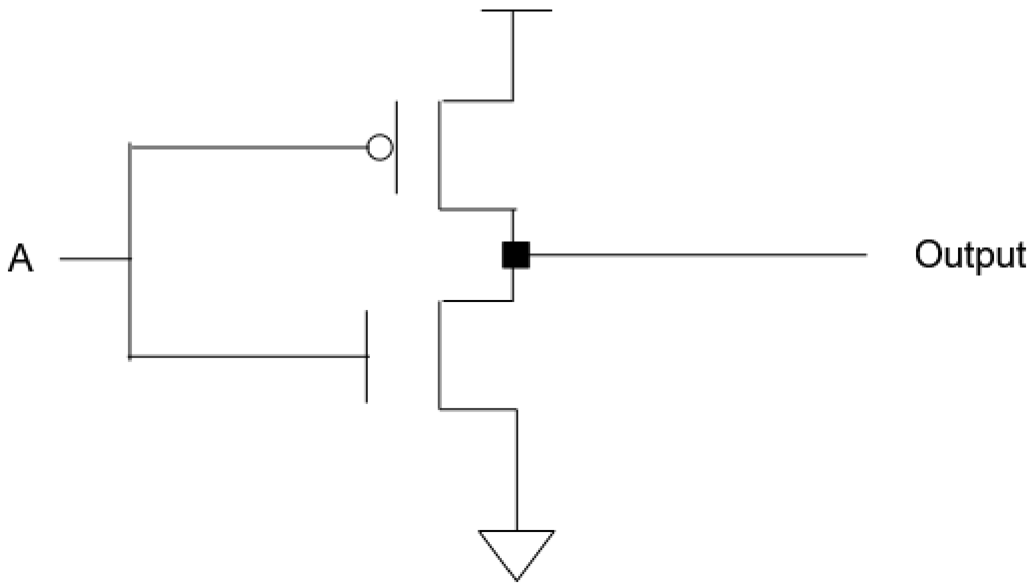
- Is this legal, if so, what's the truth table? If not, why?



Poll Everywhere

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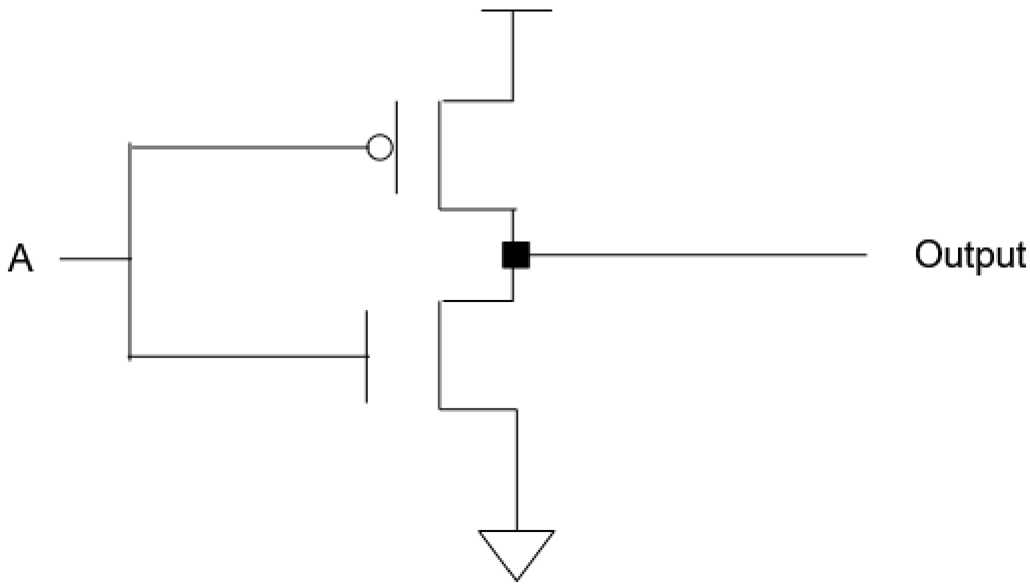

Legal!

A	Output
0	1
1	0

~A = output

This is the "not" circuit

Poll Everywhere

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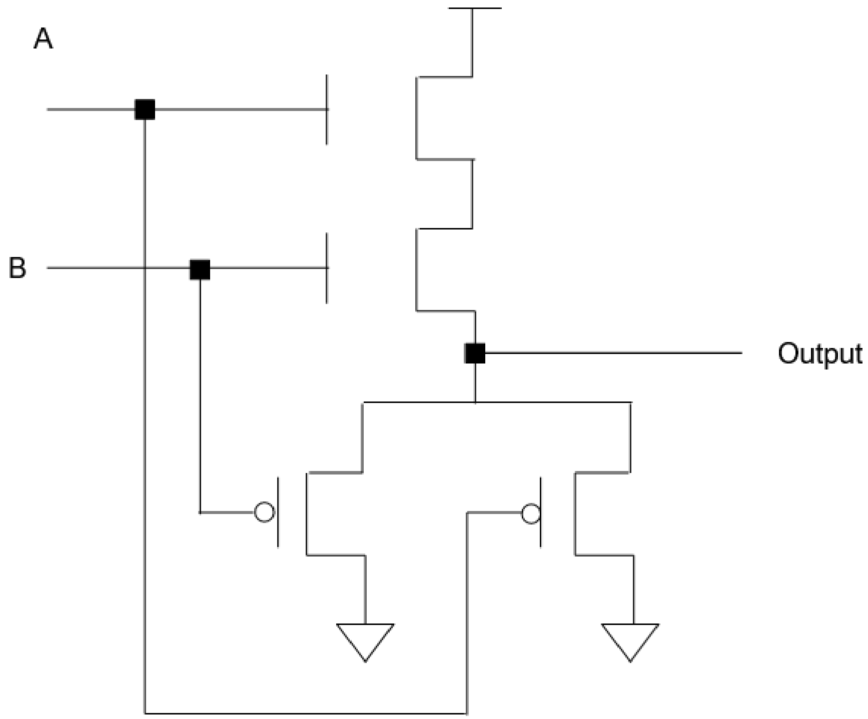
- Is this legal, if so, what's the truth table? If not, why?



Poll Everywhere

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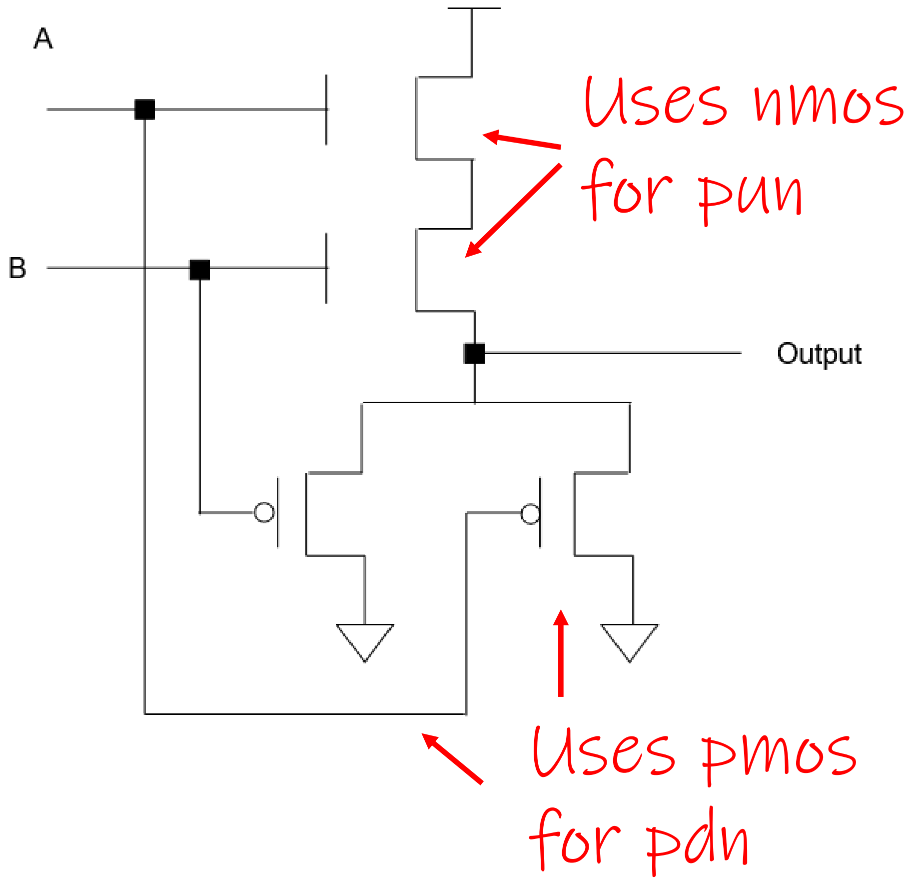

Illegal

Why?

Poll Everywhere

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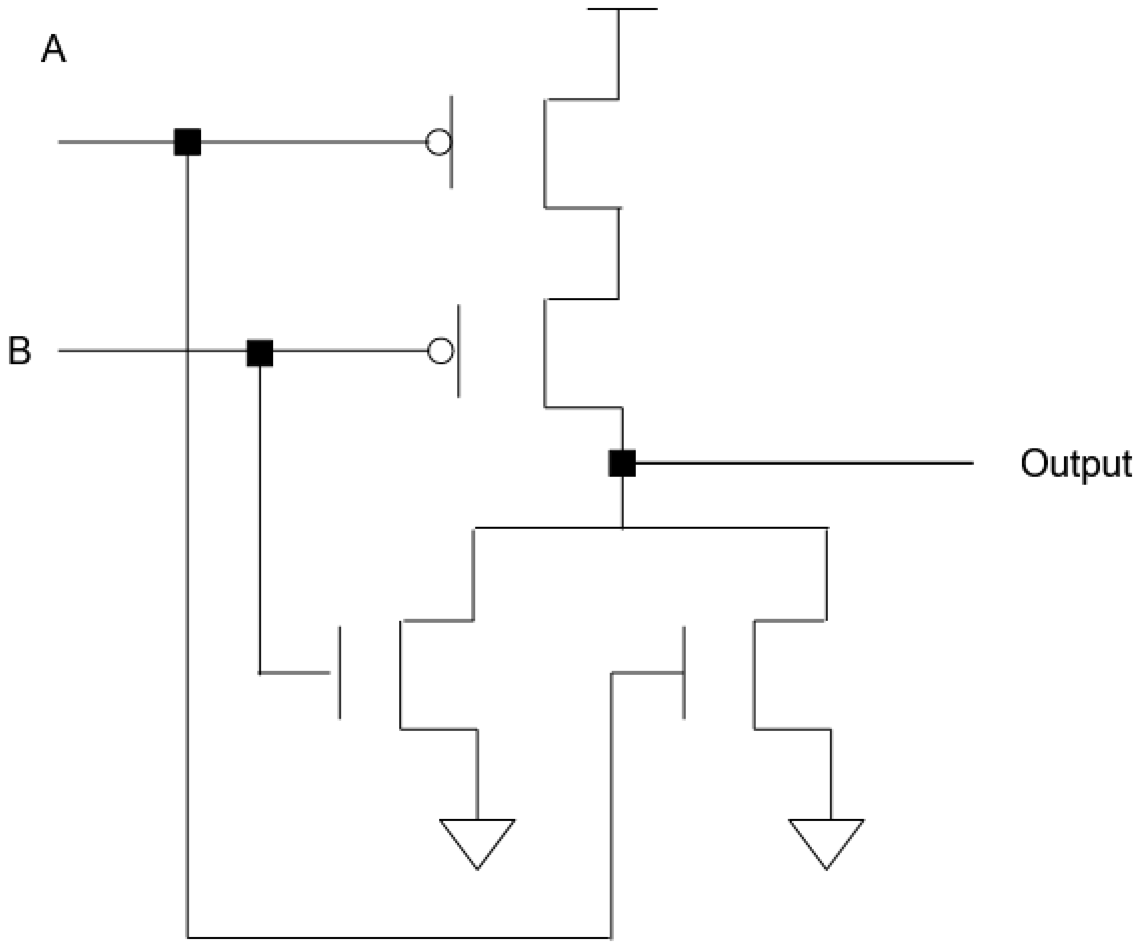
- Is this legal, if so, what's the truth table? If not, why?



Poll Everywhere

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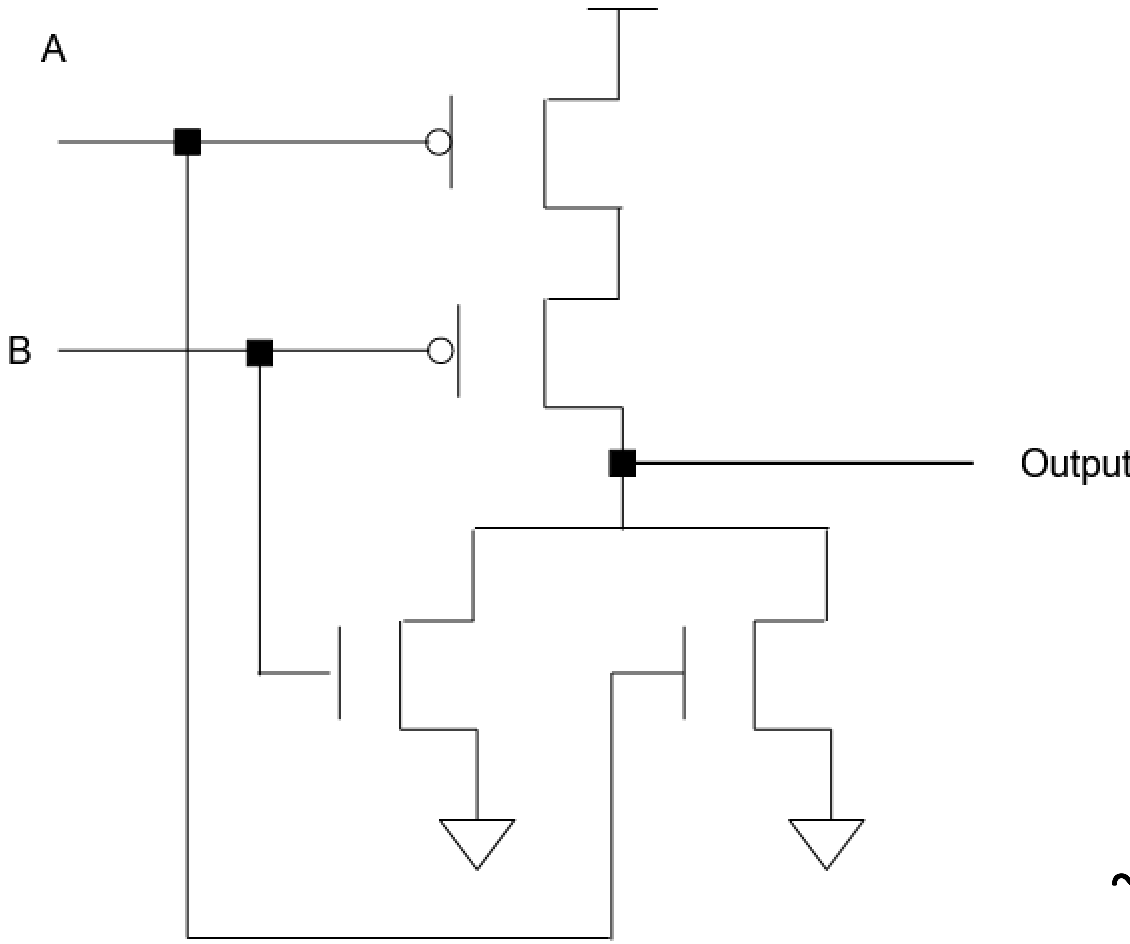

Legal!

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

~(A|B) = output

This is "nor"

Poll Everywhere

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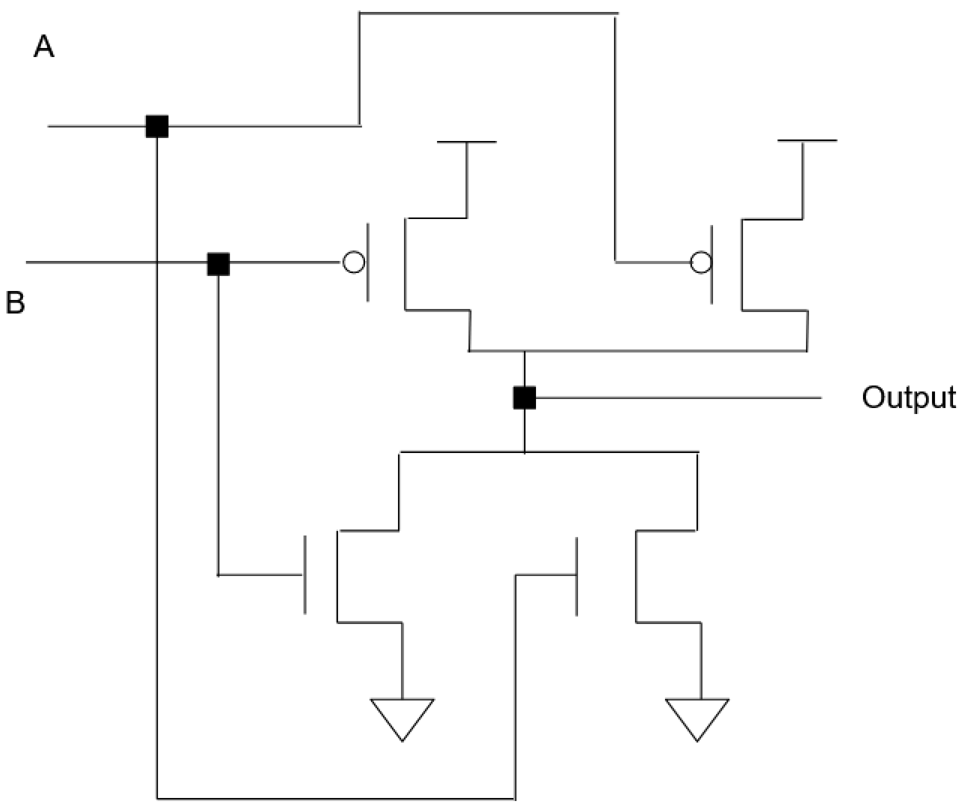
- Is this legal, if so, what's the truth table? If not, why?



Poll Everywhere

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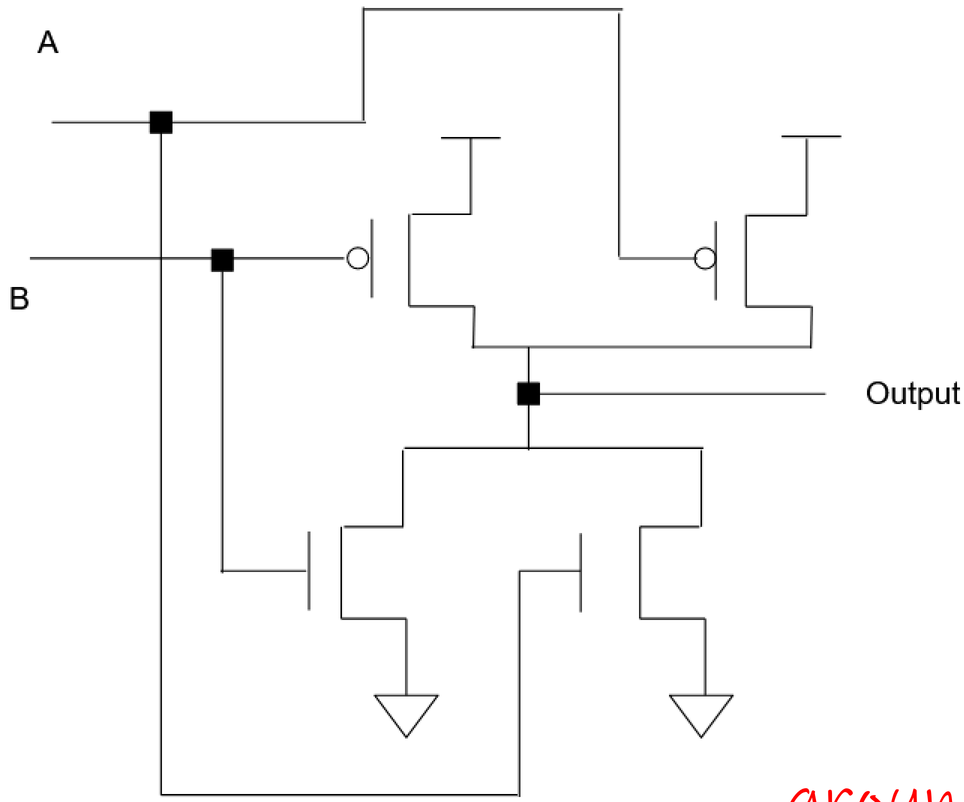


Illegal

Why?

Consider inputs

$a = 0$

$b = 1$

ground and power both connected to output!!!!!!

Lecture Outline

- Physics Background
- CMOS Transistor
- CMOS Logical Circuits
- **CMOS Circuit Design**

Rules & Suggestions For Design

- Rules:
  - You cannot have pMOS transistors in the PDN
  - You cannot have nMOS in the PUN
  - Exactly one of PDN/PUN must be "on" at a time
    - Cannot have neither connected to output
    - Cannot have both connected to output
  - Every transistor in the PDN must have a complimentary transistor in the PUN
    - When any transistor is PDN is ON, its compliment transistor is OFF

- Suggestions
  - Start with the PDN and then do the PUN (most find it easier)
  - Simplify logic before you design any part of the circuit

NOR Circuit Design Walkthrough

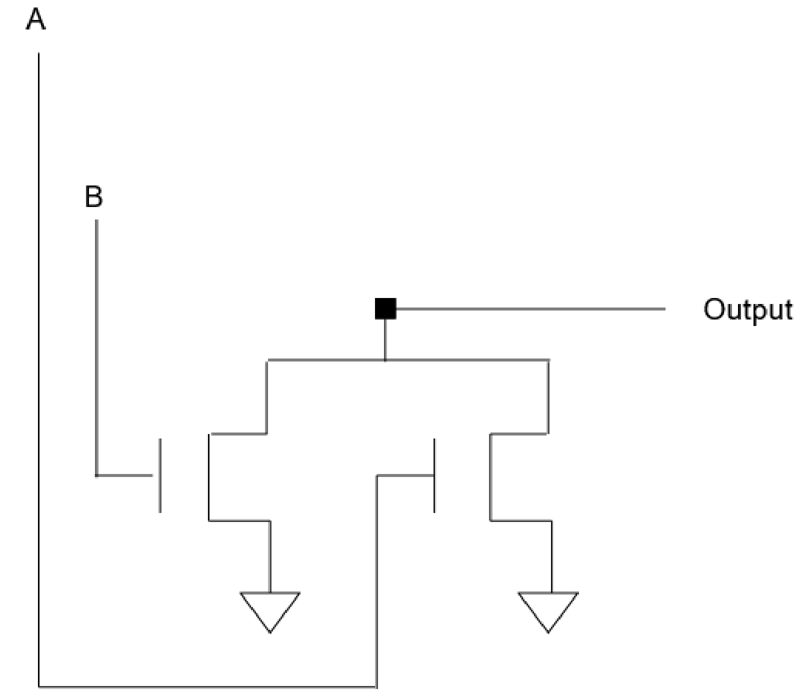
- First, start with the Boolean Expression
  - NOR is NOT-OR, which is
    ~(A | B) <- statement for when output is 1 (True)

- Since I like to start with PDN, find the cases when output is FALSE, then simplify
  - This can be done by negating the original expression
  - ~~(A | B) <- statement for when output is 0 (False)
  - (A | B) <- simplified by identity property

NOR Circuit Design Walkthrough

- With the expression for the PDN (when output is 0), translate it to a circuit diagram for the PDN
  - OR’s become transistors in parallel
  - AND’s become transistors in series

(A | B) becomes



NOR Circuit PUN (Strategy 1)

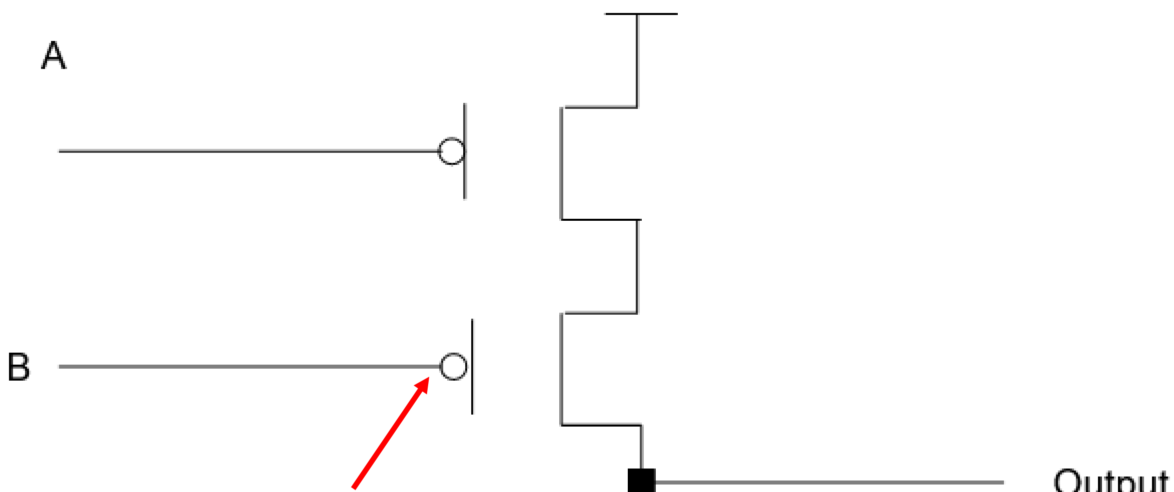
- With the simplified expression for PDN, negate it to get the expression for PUN
  - (A | B) becomes ~(A | B)
  - Simplify
    - ~(A | B)
    - (~A & ~B) // by De Morgan's Law

In this example, initial PUN expression is the same as the original expression. This is not always the case

- From here, we can convert (~A & ~B) into a PUN

NOR Circuit PUN (Strategy 1)

- From here, we can convert (~A & ~B) into a PUN
  - OR's become transistors in parallel
  - AND's become transistors in series
  - pMOS transistors have an implicit "NOT"
    - pMOS only turns on when input is low (0)

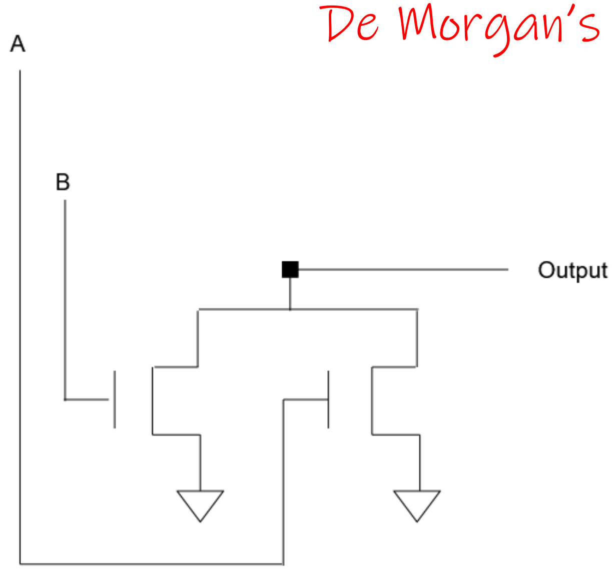


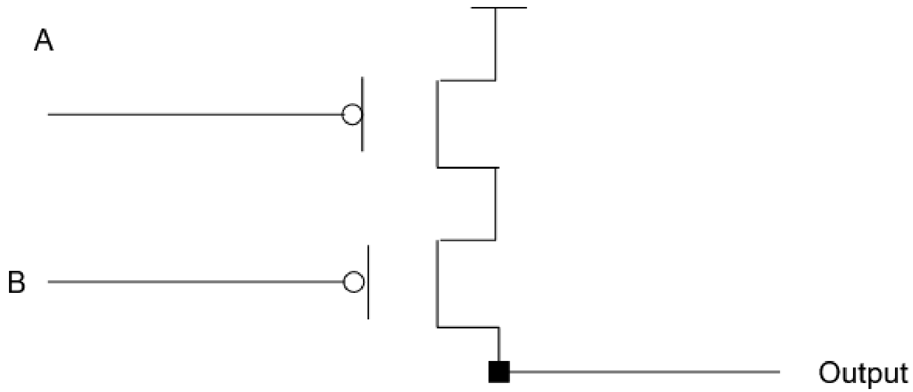
The reason for the circle in pMOS:
Circle represents a "Not" or negation

NOR Circuit PUN (Strategy 2)

- Alternative way to get the PUN from the PDN
  - Series relations in PDN become Parallel relations in PUN
  - Parallel relations in PUN become Series relations in PUN
  - nMOS transistors become pMOS transistors

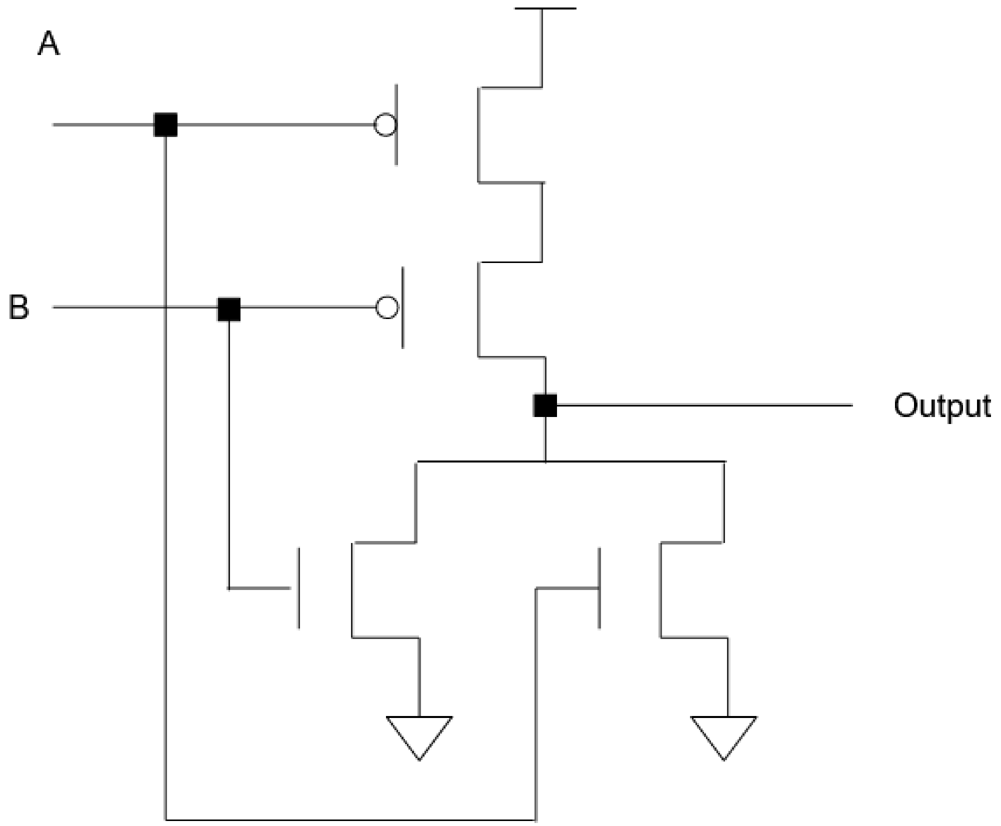
This is just a "short-cut" for applying
De Morgan's to the PDN





Completed NOR Circuit

- Finally, all you have to do is combine the PDN and PUN
  - To be safe, check your work and create a truth table



A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0