Sequential Logic

Latches, Flip Flop, Gate Delays, Clock, Timing

CIS 2400 Recitation 3

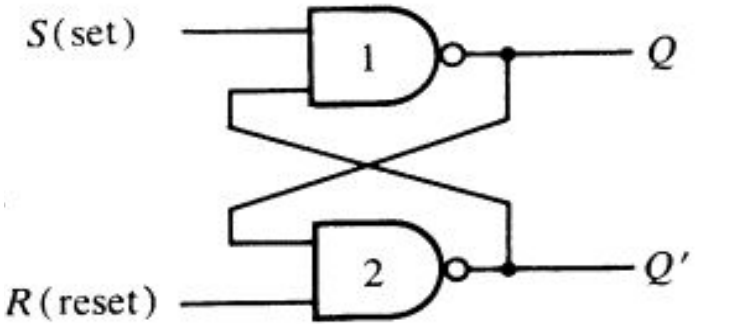
Recitation Outline

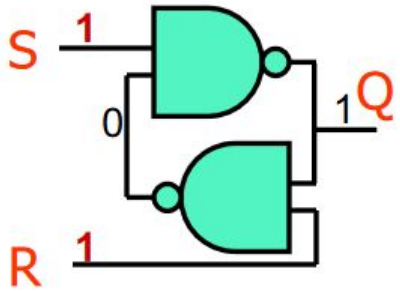
- Latches
- Clock
- Flip Flops

Latches

SR Latch

- Provides us a way to store a bit value (*Q*), used as memory
- Can store & change value with two inputs: S and R

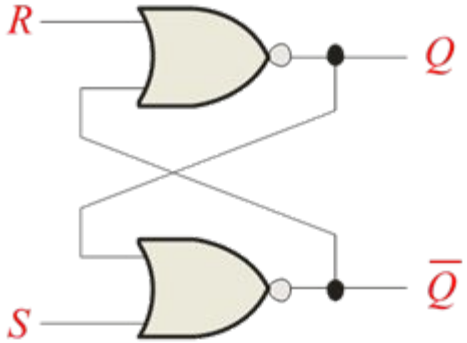




S	R	Effect
0	0	**BAD???**
0	1	Q = 1
1	0	Q = 0
1	1	Stable

Exercise: RS Latch?

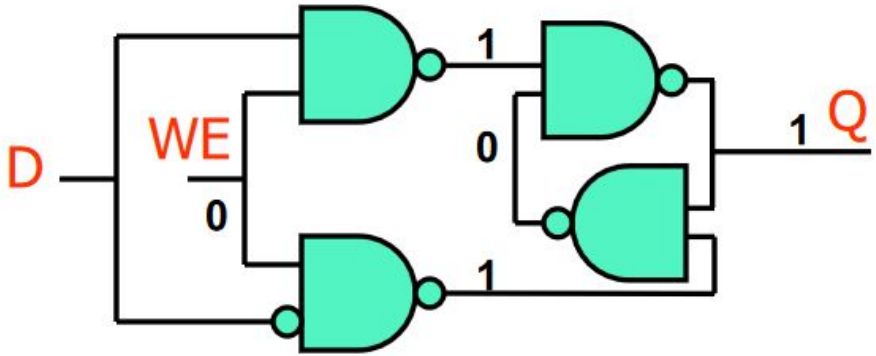
- How does the behavior change if we cross-couple NOR gates instead?



S	R	Effect
0	0	Stable
0	1	Q = 0
1	0	Q = 1
1	1	**Invalid**

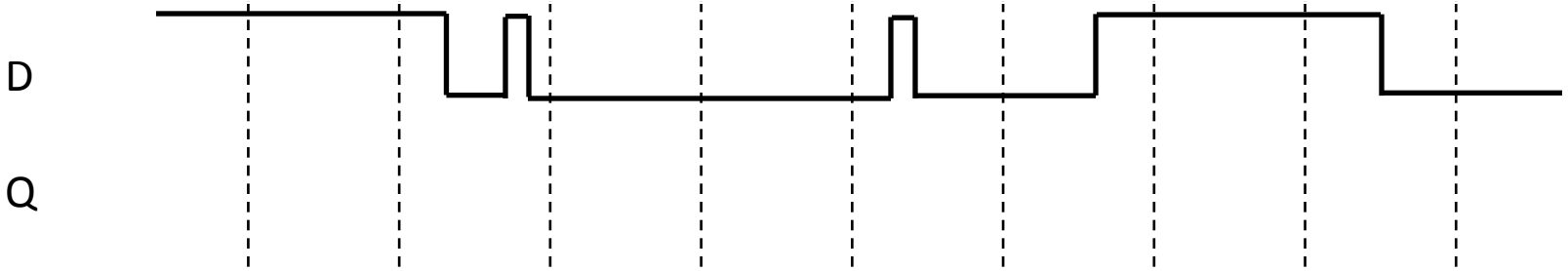
D Latch

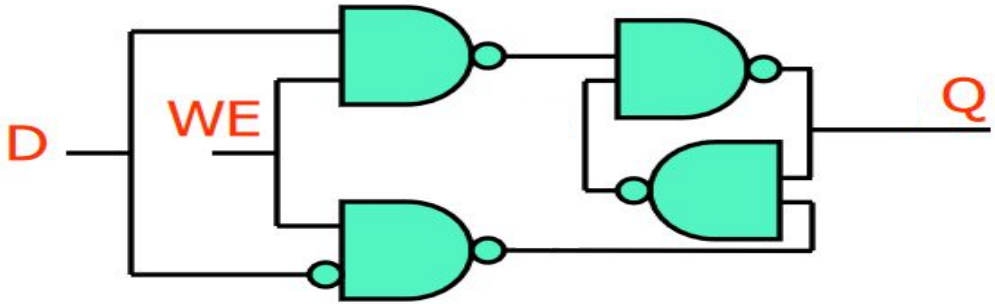
- Goal: Make the RS latch understandable
  - Replace R and S with D, add WE for utility
- D the data we want to store (either 1 or 0)
- WE, whether writing (storing that bit) is enabled.
  - If not enabled, Q (the stored data) maintains current value



D Latch

- Consider the following signal. What is the signal output (Q) of our D Latch? (Assume that WE is 1)

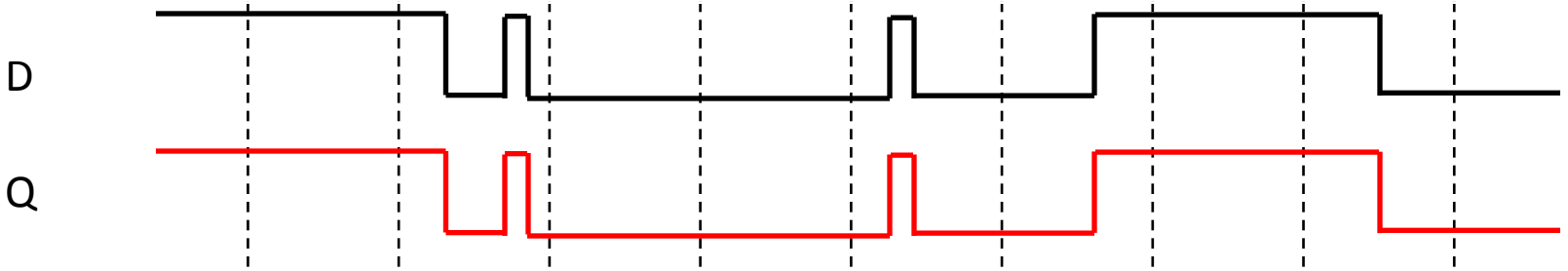


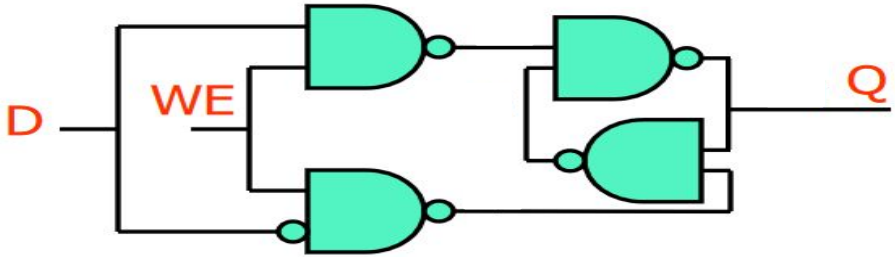


D Latch

- Consider the following signal. What is the signal output (Q) of our D Latch? (assume that WE is 1)

We get all the signal all the time

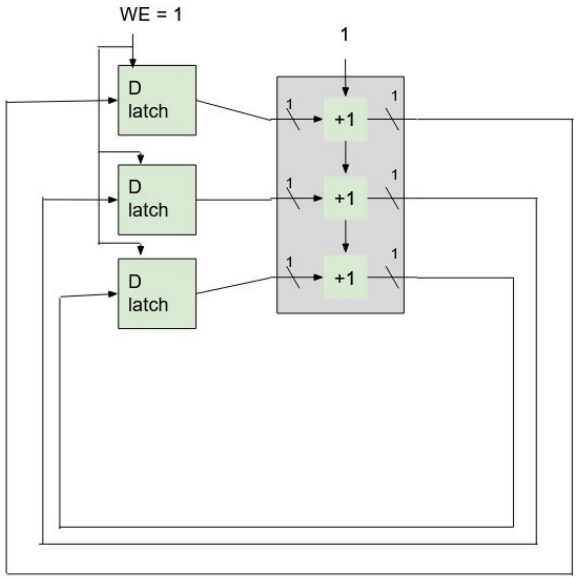




This is called "Transparent"

Transparency Issues

- Consider that we had a 3-bit incrementer and we wanted to make a machine with 3 1-bit D-latches that went 0 -> 7 repeatedly.



Transparency Issues

Next int feeds directly back into input

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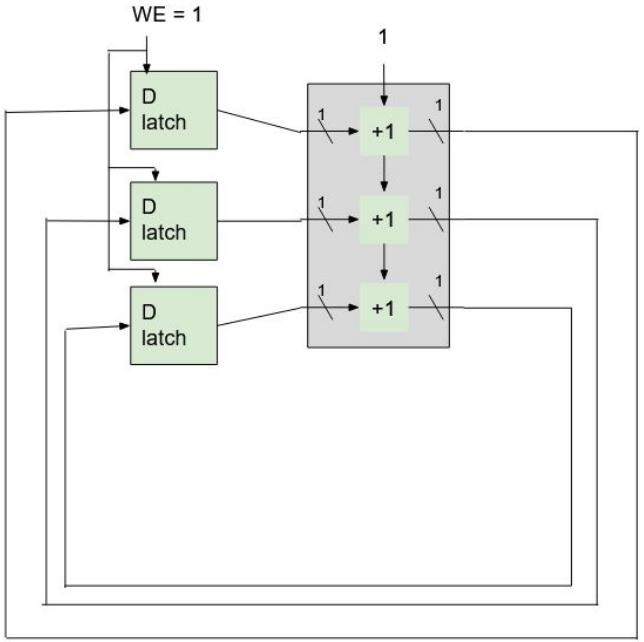
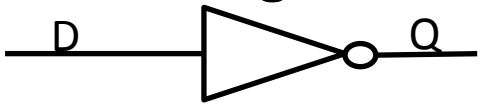


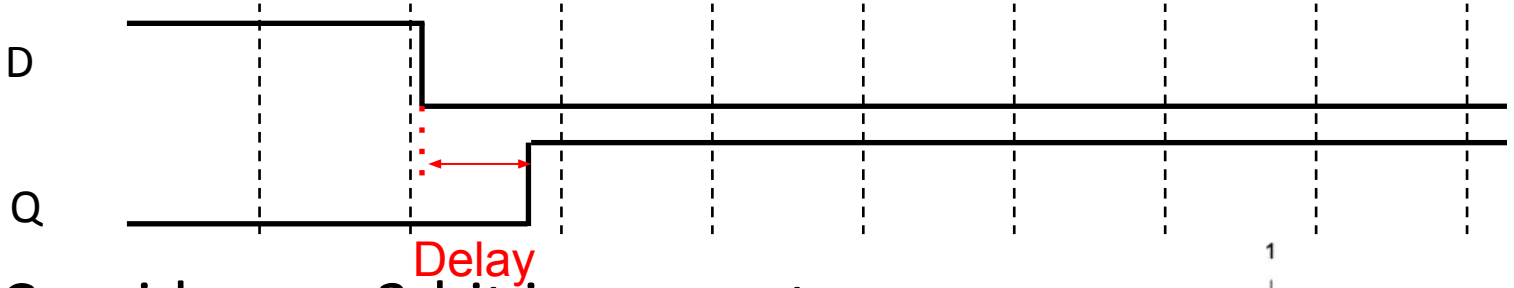
What if all three bits aren't ready at the same time?

How would we know when a value was "stable/readable"?

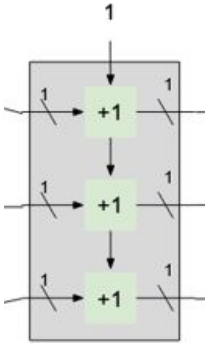
Delays

- It takes time for a gate/unit to process an input.





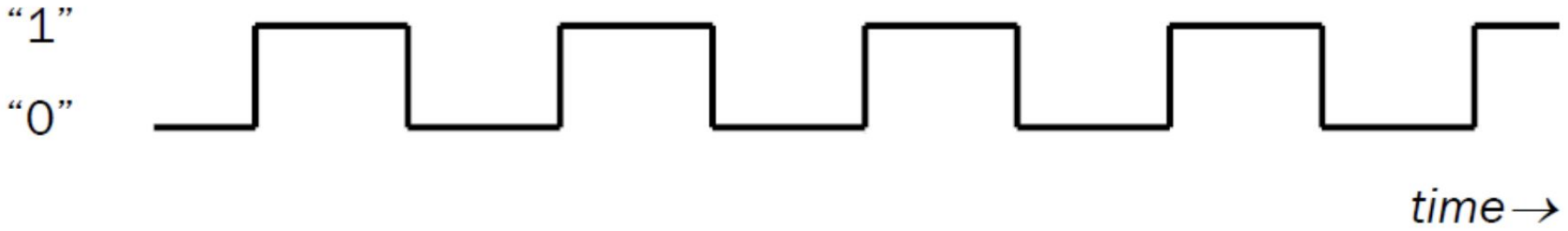
- Consider our 3-bit incrementer
  - Each 'bit' incrementer depends on the carry from the previous bit incrementors
    - The LSB may be updated before the MSB



Clock

Clock Review

- Regular up/down signal for synchronization
- Clock period?
- Clock frequency?

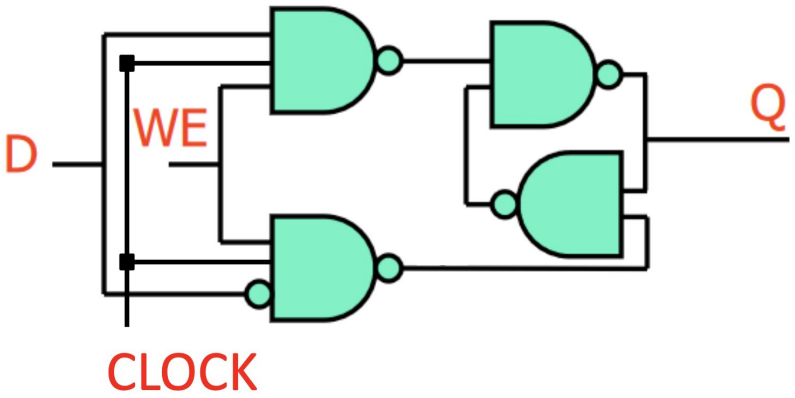


D-Latch with Clock

- CLK signal ANDed in

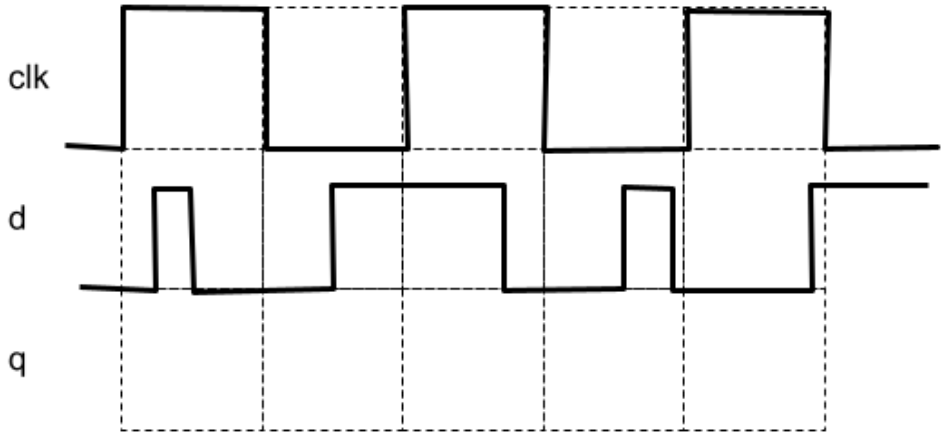
Assuming WE = 1:

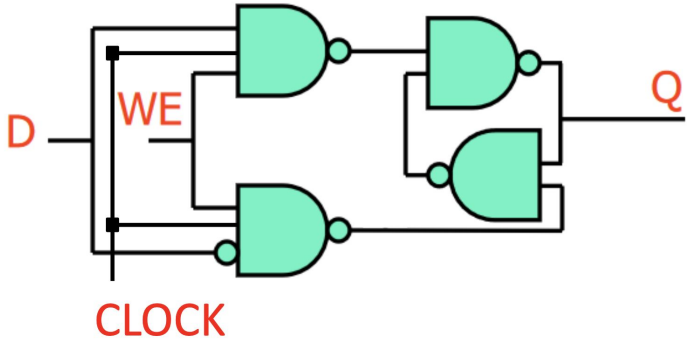
- What happens when CLK=0?
- What happens when CLK=1?



D-Latch with Clock

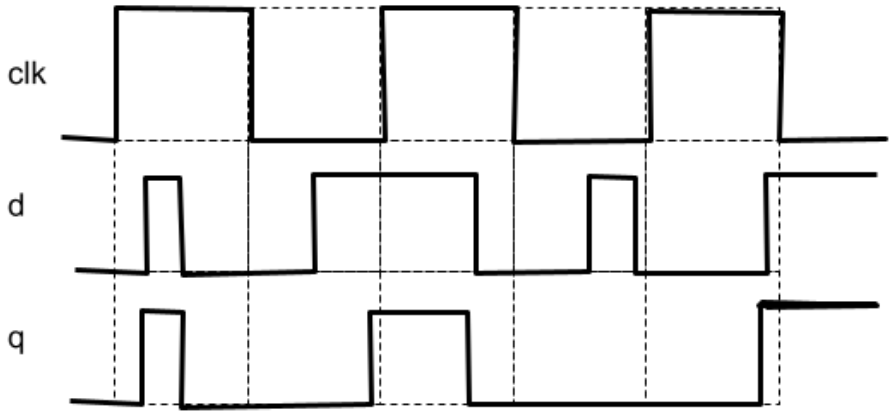
What's the timing diagram?

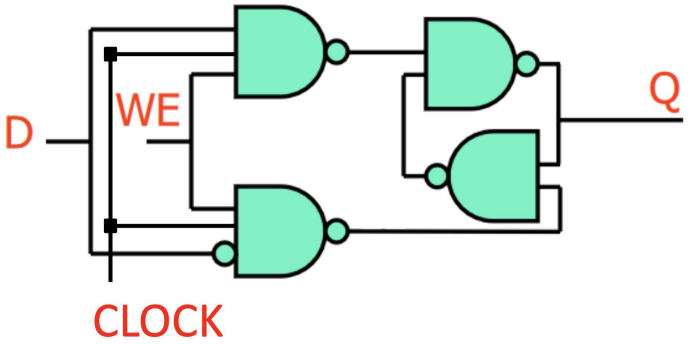




D-Latch with Clock

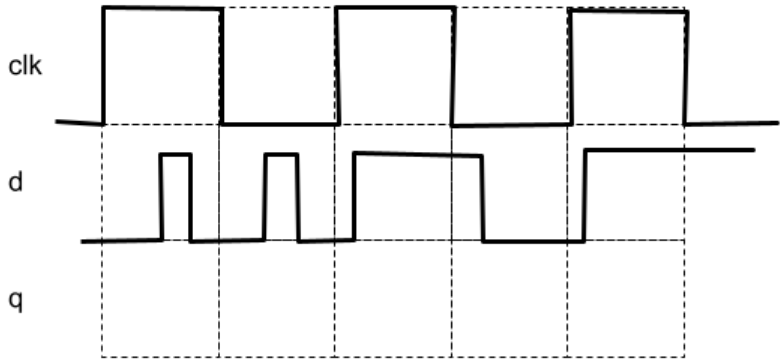
This is *semi-transparent*!

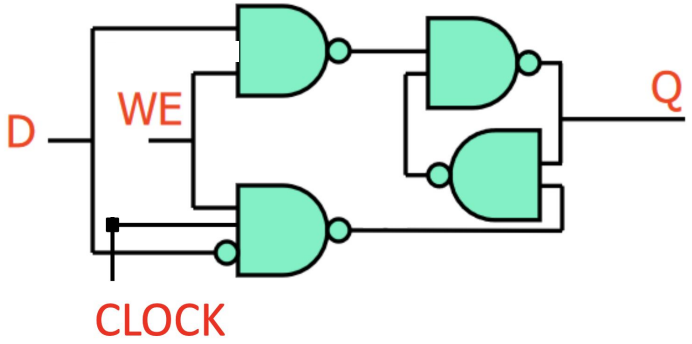




Thought Exercise

What if one of the CLK input wires breaks? What's the timing diagram then? (WE = 1)





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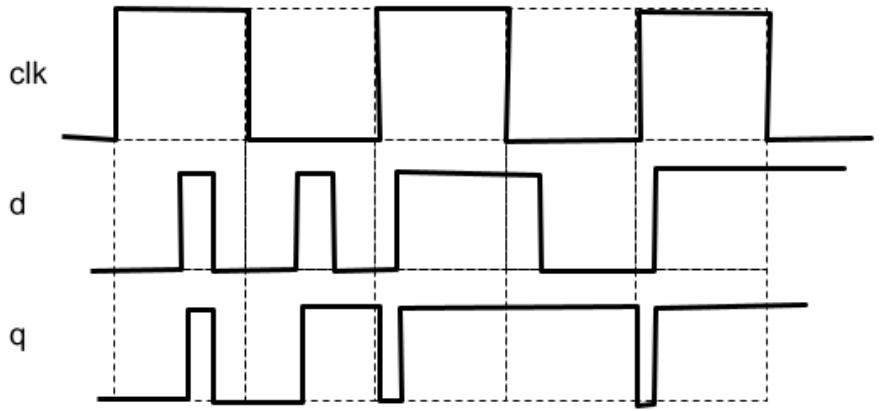
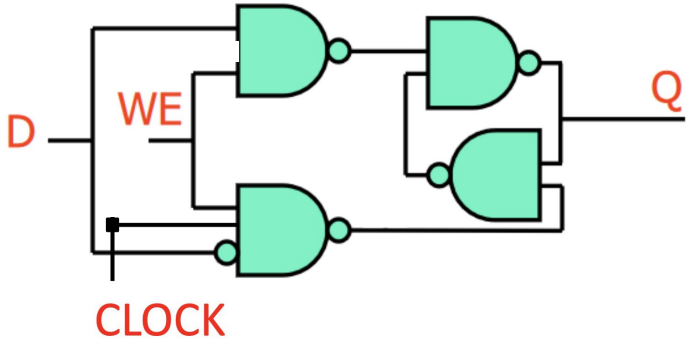


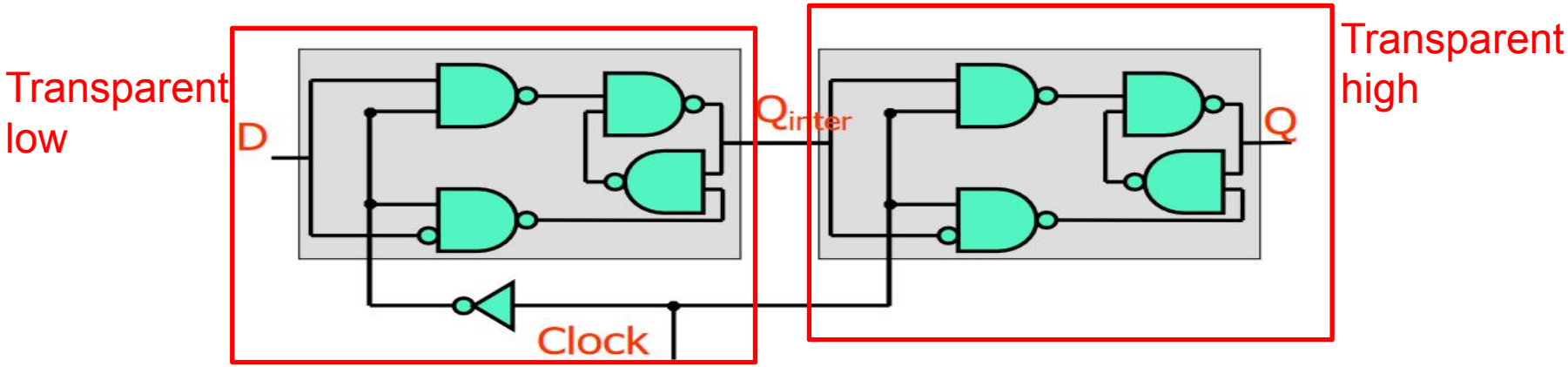


Flip Flops

D Flip Flop

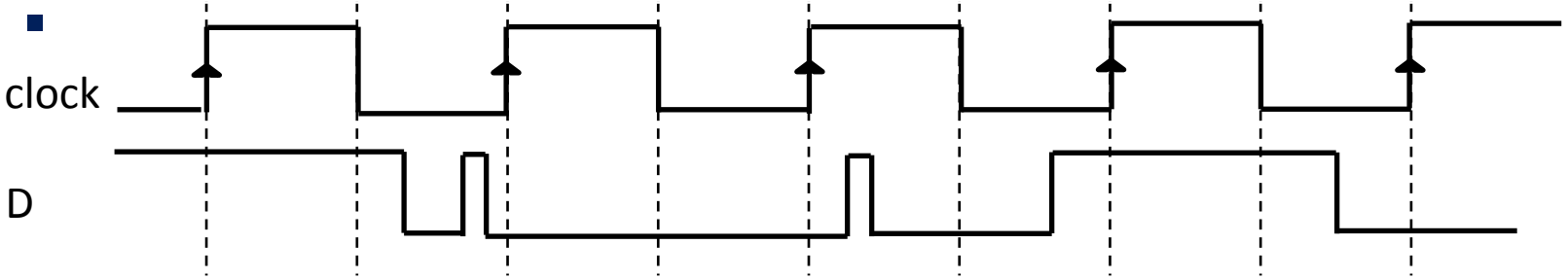
- Made by:
  - Appending a transparent-high onto a transparent-low latch
- Rules:
  - Q_{inter} is the result of passing D through a transparent-low latch
  - Q is the result of passing Q_{inter} through a transparent-high latch
    - Effectively,this makes Q only “sensitive” to the signal value at the rising edge of the clock

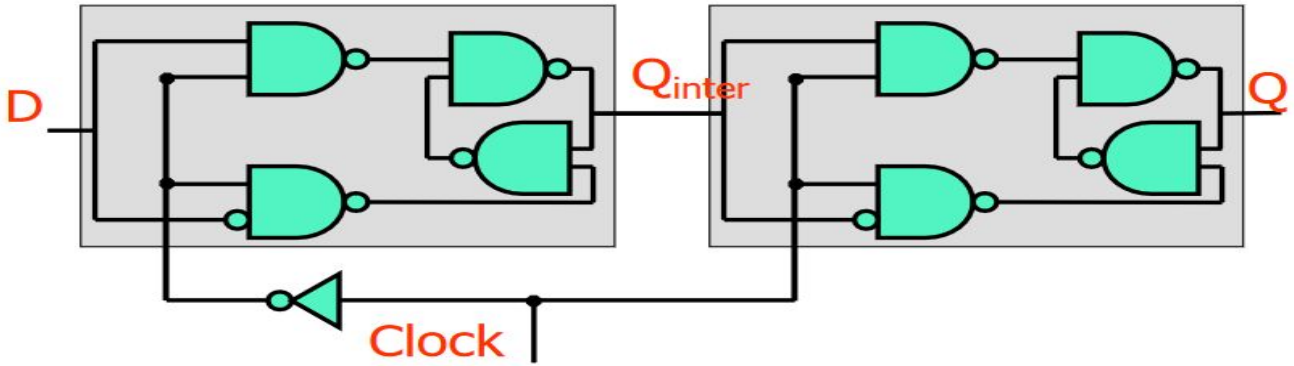
D Flip Flop



D Flip Flop Practice

- What is Q and Qinter for a D flip flop with the given clock and D signal





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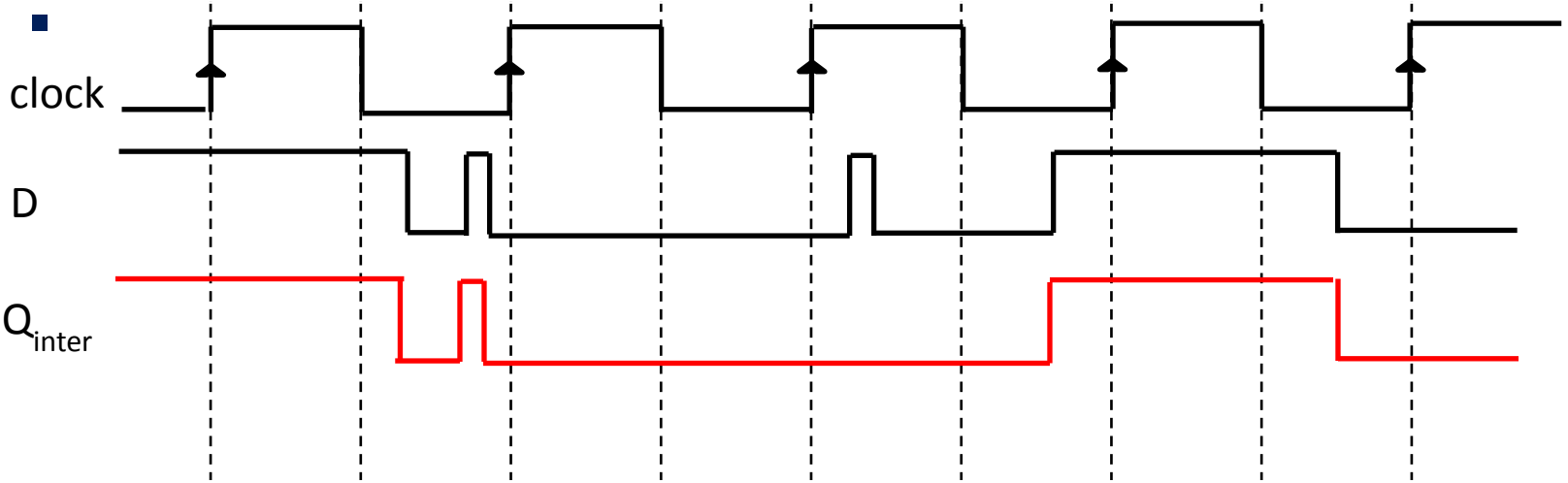

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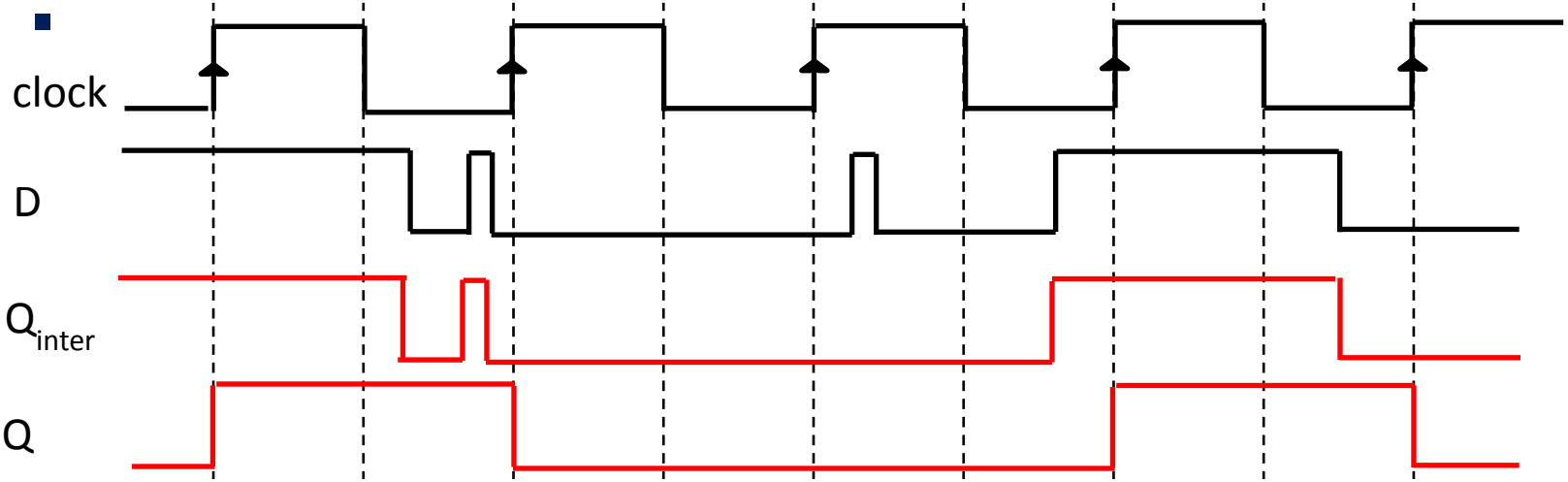

Q updates exactly once per clock cycle! (on a rising edge)
Value is more “stable”

That's all we have for today!

Reminders:

- TA-lead recitations will take place on
  - Tuesdays 6:30-8:00pm in Moore 100A
  - Wednesday 12:00-1:30pm in Moore 100C
- Homework 3 is due this Friday 10/7
- **Note:** Check the course website for OH times! They may have time changes, location changes, or cancellations due to fall break.

Enjoy your fall break!! 🍁🍂🌾