CIT 595

Finite State Machine Problem

1. Draw a FSM state diagram (Mealy/Moore) to describe a serial comparator with n-bit unsigned numbers x and y as inputs. The FSM takes two bits $x_i$ and $y_i$ at a time (every clock cycle). Assume the two bits are being fed in from MSB to LSB. E.g. $x_{n-1}$ and $y_{n-1}$ arrive at time unit 1 and $x_{n-2}$ and $y_{n-2}$ at time unit 2.

   The output of the FSM should be
   • 00 if the two values are equal
   • 10 if x has a larger value
   • 01 if y has a larger value

   You can assume that FSM has start state and can be reset to this state when new n-bit inputs (x & y) need to be evaluated.

   ![FSM Diagram](image)

   Note: In both FSM, A would be start state as at beginning we don’t know anything about the numbers and hence it is safe to assume that they are equal to start out with.
2. Consider a sequence detector that receives a bit-serial input $X$ and asserts an output $Z$ (i.e. $Z = 1$) when it detects a binary string 0110 in sequence of 0s and 1s. Use symbolic states with letters such as A, B, etc. You can also assume that ‘A’ is start state, in which the machine can start out or reset.

   a. Draw a Moore Machine state diagram for this sequence detector.

   ![Moore Machine Diagram]

   b. Draw a Mealy Machine state diagram for this sequence detector.

   ![Mealy Machine Diagram]