University of Pennsylvania
Department of Electrical and System Engineering
Digital Audio Basics

ESE150, Spring 2018 ~~Midterm~~ Final Wednesday, May 2

- Exam ends at 8:00PM; begin as instructed (target 6:00PM)
- Problems weighted as shown at bottom of page.
- Calculators allowed.
- Closed book = No text or notes allowed.
- Provided reference materials on next to last page.
- Show work for partial credit consideration.
- Unless otherwise noted, answers to two significant figures are sufficient.
- Sign Code of Academic Integrity statement (see last page for code).

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I certify that I have complied with the University of Pennsylvania's Code of Academic Integrity in completing this exam.

Name:

1	2					3						4			
	a	b.i	b.ii	c.i	c.ii	a	b	c	d	e	f	a	b	c.i	c.ii
10	4	2	1	2	1	3	3	3	3	3	3	3	3	3	4

5			6				7				8			**Total**
a	b	c	a	b	c	d	a.i	a.ii	a.iii	b	a	b	c	
2	3	7	3	3	3	3	2	2	2	2	5	5	7	100

1. Implement the following truth table using inverters and 2-input AND and OR gates.

a	b	c	d	out
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

2. We want to move a running computation from one processor to another.

   (a) What information do we need to transfer in order to allow the computation to continue and produce the correct answer?

   (b) Consider compressing the data before transfer (and decompressing after) using Huffman Encoding.

      i. Will this work (allow the computation to resume on the new processor, run to completion, and produce the same result as if it had not been moved or compressed/uncompressed)?

      ii. How effective is this compression likely to be (Impact on data transfered by component)? Give specific examples where it will be effective or ineffective.

   (c) Consider compressing the data before transfer (and decompressing after) using MP3 encoder (decoder).

      i. Will this work (allow the computation to resume on the new processor, run to completion, and produce the same result as if it had not been moved or compressed/uncompressed)?

      ii. How effective is this compression likely to be (Impact on data transfered by component)? Give specific examples where it will be effective or ineffective.

3. Consider sending audio data over a UDP (Unreliable Datagram Protocol) link. Assume the receiver is aware of which packets are lost and will make the best of the information it does receive. As in lab, the frequency packets are based on Fourier Transforms of time windows. Rank in order of subjective quality for humans based on your knowledge of audio processing and human psychoacoustics from this course (1-best, 6-worst). Justify your answers by explaining the impact of losing a packet in each case.

   (a) ☐ Packets contain PCM (raw, quantized time-sample data)

   (b) ☐ Packets come in pairs for a time window with the highest frequency critical bands in one packet, and the rest in the second.

   (c) ☐ Packets come in pairs for a time window with the even timeslot PCM samples in one packet of the pair, and odd timeslot PCM samples in the other.

   (d) ☐ Packets come in pairs for a time window, were the first packet contains the top 8b of the amplitude for all frequency and the second the low 8b.

(e) ☐ Packets come in pairs for a time window where both the first and second packet in a pair contains the top one-third frequencies (by amplitude) in each critical band. The first packet also contains the middle one-third of the highest frequency critical bands, while the second packet contains the middle one-third of the remaining critical bands.

(f) ☐ Packets come in pairs for a time window, where the highest amplitude frequencies from each critical band are in one packet and the lowest in the other.

4. Consider a FLASH memory with the following characteristic:
   - 64KB native flash pages
   - Opening a flash page takes 25μs
   - Once open, access within a flash page is 25 ns per Byte.
   - inodes and bnodes are 1KB blocks
   - must read all bytes in each 1KB block

   (a) How long to read a 38KB file organized as one 1KB inode and 38 1KB bnodes, all of which are placed in the same 64KB flash page?

   (b) How long to read a 38KB file organized as one 1KB inode and 38 1KB bnodes, each of which is placed in a different 64KB flash page?

(c) Consider storing 4 files: A of size 512B, B of size 41KB, C of size 33KB, and D of size 49KB.
(assume all are 1 inode and $\lceil size/1\text{KB} \rceil$ bnodes):

i. How should we place these files into pages in order to minimize the access time for every file? (minimize pages used as a secondary goal.)

ii. How should we place these files into pages to minimize the number of 64KB pages used? (minimize access time as a secondary goal.) Quantify overall space saving percentage and per file read performance impact percentage.

5. Consider the following Arduino Assembly code:

```
000010a2 <__udivmodsi4>:
    10a2: a1 e2        ldi r26, 0x21 ; 33
    10a4: 1a 2e        mov r1, r26
    10a6: aa 1b        sub r26, r26
    10a8: bb 1b        sub r27, r27
    10aa: fd 01        movw r30, r26
    10ac: 0d c0        rjmp .+26       ; 0x10c8 <__udivmodsi4_ep>

000010ae <__udivmodsi4_loop>:
    10ae: aa 1f        adc r26, r26
    10b0: bb 1f        adc r27, r27
    10b2: ee 1f        adc r30, r30
    10b4: ff 1f        adc r31, r31
    10b6: a2 17        cp r26, r18
    10b8: b3 07        cpc r27, r19
    10ba: e4 07        cpc r30, r20
    10bc: f5 07        cpc r31, r21
    10be: 20 f0        brcs .+8        ; 0x10c8 <__udivmodsi4_ep>
    10c0: a2 1b        sub r26, r18
    10c2: b3 0b        sbc r27, r19
    10c4: e4 0b        sbc r30, r20
    10c6: f5 0b        sbc r31, r21

000010c8 <__udivmodsi4_ep>:
    10c8: 66 1f        adc r22, r22
    10ca: 77 1f        adc r23, r23
    10cc: 88 1f        adc r24, r24
    10ce: 99 1f        adc r25, r25
    10d0: 1a 94        dec r1
    10d2: 69 f7        brne .-38       ; 0x10ae <__udivmodsi4_loop>
    10d4: 60 95        com r22
    10d6: 70 95        com r23
    10d8: 80 95        com r24
    10da: 90 95        com r25
    10dc: 9b 01        movw r18, r22
    10de: ac 01        movw r20, r24
    10e0: bd 01        movw r22, r26
    10e2: cf 01        movw r24, r30
    10e4: 08 95        ret
```

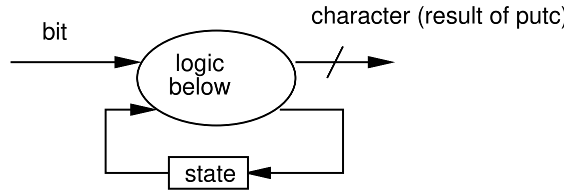
(a) Identify the top and bottom of the loop.

(b) How many times does the loop execute?
(Hint: What is the loop exit condition? What register holds the value tested for the exit condition? What happens to this register on each loop iteration? How is the register initialized?)

(c) What is the worst-case number of cycles from entering at 0x10a2 to performing the return at 0x10e4?

(instruction table on next to last page)

6. Consider the following FSM for decoding serial, Huffman encoded data into characters.




```
int state=START;
while(true) {
  int bit=nextInputBit();
  switch(state) {
  case START:  if (bit==0) state=S0; else state=S1; break;
  case S0:  if (bit==0) state=S00; else state=S01; break;
  case S1:  if (bit==0) state=S10; else state=S11; break;
  case S00:  if (bit==0) state=S000; else{ state=START; putc('E'); } break;
  case S01:  if (bit==0) state=S010; else  state=S011; break;
  case S10:  if (bit==0) state=S100; else {state=START; putc(' ');} break;
  case S11:  if (bit==0) state=S110; else state=S111; break;
  case S000: if (bit==0) state=S0000; else {state=START; putc('H');} break;
  case S010: if (bit==0) {state=START; putc('R');} else {state=START; putc('S');} break;
  case S011: if (bit==0) {state=START; putc('N');} else state=S0111; break;
  case S100: if (bit==0) {state=START; putc('I');} else {state=START; putc('O');} break;
  case S110: if (bit==0) {state=START; putc('A');} else state=S1101; break;
  case S111: if (bit==0) {state=START; putc('T');} else state=S1111; break;
  case S0000: if (bit==0) {state=START; putc('C');} else {state=START; putc('U');} break;
  case S0111: if (bit==0) state=S01110; else {state=START; putc('L');} break;
  case S1101: if (bit==0) state=S11010; else {state=START; putc('D');}  break;
  case S1111:  if (bit==0) state=S11110; else  state=S11111; break;
  case S01110: if (bit==0) {state=START; putc('B');} else {state=START; putc('P');}
               break;
  case S11010: if (bit==0) {state=START; putc('G');} else {state=START; putc('W');}
               break;
  case S11110: if (bit==0) {state=START; putc('Y');} else state=S111101; break;
  case S11111: if (bit==0) {state=START; putc('F');} else {state=START; putc('M');}
               break;
  case S111101: if (bit==0) {state=START; putc('V');} else state=S1111011; break;
  case S111011: if (bit==0) state=S1110110; else {state=START; putc('K');}  break;
  case S1110110:if (bit==0) {state=START; putc('X');} else state=S11101101; break;
  case S11101101:if (bit==0) {state=START; putc('Q');} else state=S111011011; break;
  case S111011011:if (bit==0) {state=START; putc('Z');} else {state=START; putc('J');}
                  break;
               }
  }
```

(a) What is the minimum number of state bits needed to encode `state` for a hardware implementation? Why?
(Hint: different from the 16b or 32b that might be used to encode an `int` in C.)

(b) What is the encoding for the following letters:

letter	encoding
A	
B	
E	
Y	

(c) What letters can be encoded with each of the following number of bits:

bits to encode	encoding
1	
2	
3	
4	
5	
6	
7	
8	

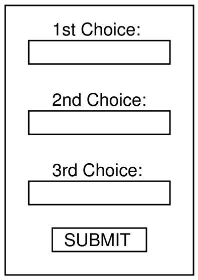
(d) Using the encoding, how many bits does it require to encode:

W	E		A	L	L		L	I	V	E		I	N		A	
Y	E	L	L	O	W		S	U	B	M	A	R	I	N	E	

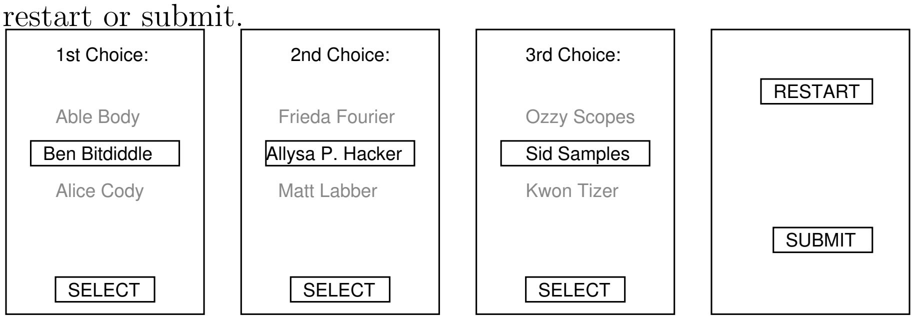
7. Consider a smartphone Application User Interface for requesting a partner assignment for lab, where the user gets to submit a prioritized list of 3 choices. Valid selections must be a student in the course which you have not worked with on previous labs.

   (a) Considering the UI design issues discussed in class, identify strengths and weaknesses of each of the following (at least one of each):

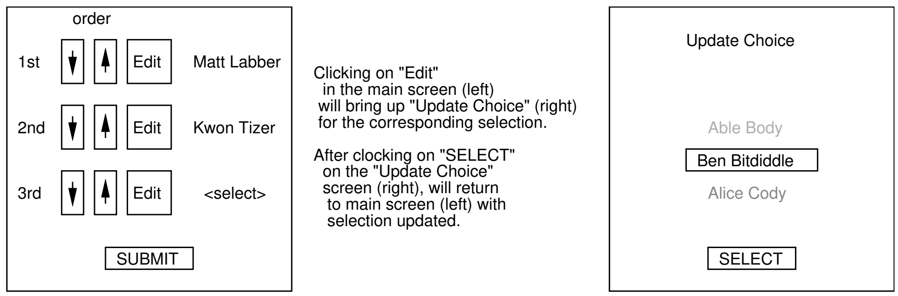
      i. Text fields to type in 3 names and submit button.



      ii. Sequence of three menus/scrolling pickers to select from all students who have not previously partnered (40-n), where n is week of lab. End with option to restart or submit.

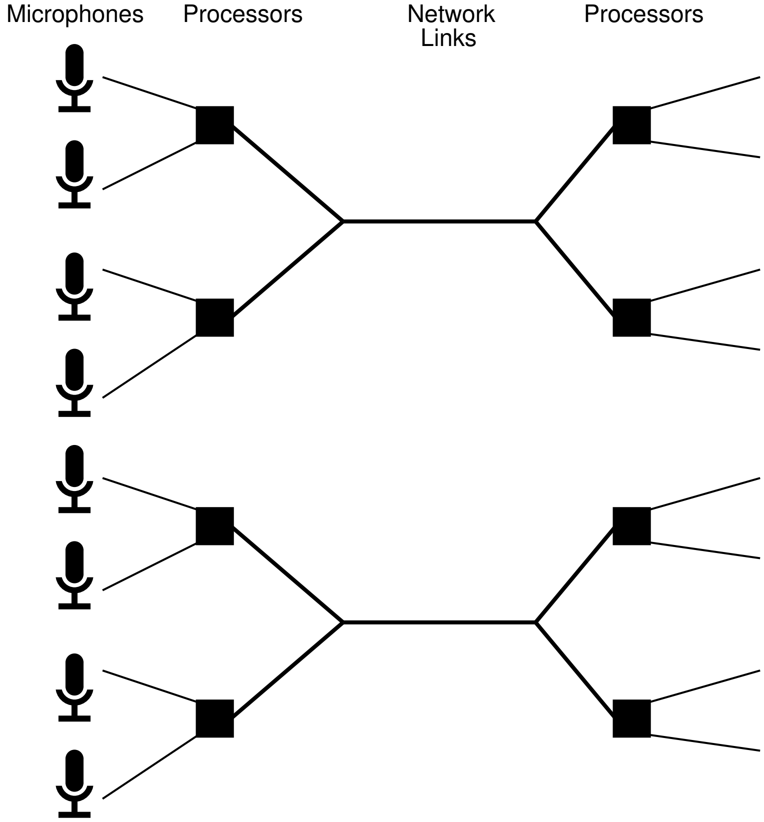


iii. Default 1st and 2nd selections to highest unassigned student from previous preferences. List current selections in order. Click on selection for scrolling picker to select (update choice). Up/down buttons to order. Submit button.



(b) Suggest an interface that is better than the options above; it may be an improvement to one of the above, a mix-and-match of features, or a completely new design.

8. Consider a scenario where audio data is collected at a number of points and sent over network links to a central location.



- PCM samples: 44KHz sample rate for each input channel at 16b/sample
- For compression (and decompression), each input channel is processed in 2048 point FFT windows
- context switch processor between channels every 2048 samples (matches window size for compression case)
- Processor runs at 1 GHz; can handle many audio channels depending on computation required.
- 20 cycles to handle each uncompressed sample
- 200 cycles of computation per sample for (de)compression
- 20,480 cycles to switch context (channels)
- Frequency transformed and MP3 compressed data is 128Kb/s per channel.
- Network link is 100 Mb/s
- Processor is $25; network link is $250.

(a) With one processor on each end and a single network link, how many uncompressed PCM sample channels can the system support? What resource sets the limit?

(b) With one processor on each end and a single network link, how many MP3 compressed channels can the system support? What resource sets the limit?

(c) What combination of processors, network links, and compression should you use to support 1000 channels at minimum cost? Include the final cost for the solution in your answer.

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Feel free to use for work space.

Human auditory critical bands:

Band Number	Low	High
1	20	100
2	100	200
3	200	300
4	300	400
5	400	510
6	510	630
7	630	720
8	720	920
9	920	1080
10	1080	1370
11	1270	1480
12	1480	1720
13	1720	2000
14	2000	2320
15	2320	2700
16	2700	3150
17	3150	3700
18	3700	4400
19	4400	5300
20	5300	6400
21	6400	7700
22	7700	9500
23	9500	12000
24	12000	15500

Arduino (AVR) Instructions:

Instruction	Operands	Description	Operation	# Clocks
add	Rd, Rr	add registers no carry	Rd ← Rd+Rr	1
adc	Rd, Rr	add registers with carry	Rd ← Rd+Rr+C	1
brcs	k	~~branch if not equal~~ branch if carry set	if (C=1) then PC ← PC+k+1	2
brne	k	~~branch if carry set~~ branch if not equal	if (Z=0) then PC ← PC+k+1	2
com	Rd	one's complement	Rd ← 0XFF-Rd	1
cp	Rd, Rr	compare	Rd-Rr	1
cpc	Rd, Rr	copmare with carry	Rd-Rr-C	1
dec	Rd	decrement	Rd ← Rd-1	1
ldi	Rd, k	load immediate	RD ← k	1
mov	Rd, Rr	move between registers	Rd ← Rr	1
movw	Rd, Rr	copy register word	Rd+1:Rd ← Rr+1:Rr	1
ret		subroutine return	PC ← STACK	4
rjmp	k	relative jump	PC ← PC+k+1	2
sub	Rd, Rr	subtract registers no carry	Rd ← Rd-Rr	1
subc	Rd, Rr	subtract registers with carry	Rd ← Rd-Rr-C	1

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