## University of Pennsylvania Department of Electrical and System Engineering Digital Audio Basics

ESE150, Spring 2018	Final	Wednesday, May 2

- Exam ends at 8:00PM; begin as instructed (target 6:00PM)
- Problems weighted as shown at bottom of page.
- Calculators allowed.

Name: Solution

- Closed book = No text or notes allowed.
- Provided reference materials on next to last page.
- Show work for partial credit consideration.
- Unless otherwise noted, answers to two significant figures are sufficient.
- Sign Code of Academic Integrity statement (see last page for code).

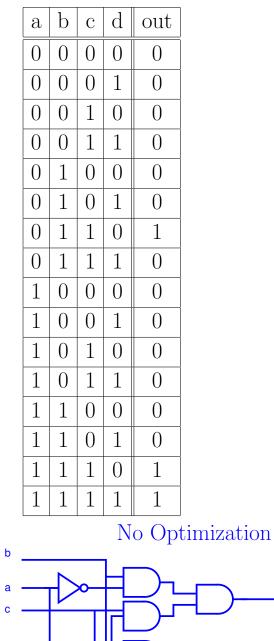
I certify that I have complied with the University of Pennsylvania's Code of Academic Integrity in completing this exam.

2 3 1 4 b.ii c.i f c.i b.i b d b c.ii c.ii а а С е а 223 1 1 3 3 3 3 3 3 3 10 3 4 4 7Total 6 58 a.ii b a.iii b b d a.i b С С a С а a 2 3 73 3 3 3 2 22 27 55 100

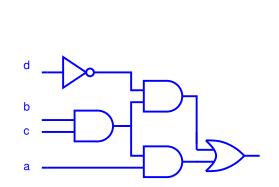
## ESE150

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1. Implement the following truth table using inverters and 2-input AND and OR gates.







- 2. We want to move a running computation from one processor to another.
  - (a) What information do we need to transfer in order to allow the computation to continue and produce the correct answer?
    - i. Program Counter
    - ii. Instructions (contents of instruction memory)
    - iii. Data (contents of data memory)
  - (b) Consider compressing the data before transfer (and decompressing after) using Huffman Encoding.
    - i. Will this work (allow the computation to resume on the new processor, run to completion, and produce the same result as if it had not been moved or compressed/uncompressed)?

Yes. Huffman encoding is lossless, so all state can be restored exactly to the original values.

- ii. How effective is this compression likely to be (Impact on data transfered by component)? Give specific examples where it will be effective or ineffective. We will likely to get some compression on instructions due to recurring instruction sequences. Effectiveness on data memory will depend on what's in it. If portions of the memory are 0 (perhaps because they are unused), that will compress well. Any other case where a common value is in memory will also compress well. The program counter is a small part of the state and not necessarily compressible.
- (c) Consider compressing the data before transfer (and decompressing after) using MP3 encoder (decoder).
  - i. Will this work (allow the computation to resume on the new processor, run to completion, and produce the same result as if it had not been moved or compressed/uncompressed)?

No. The MP3 encoding is lossy. If any of the bits in the instruction memory or program counter are changed, the program will not execute as intended. Changes in data state will also lead to incorrect values being computed.

ii. How effective is this compression likely to be (Impact on data transfered by component)? Give specific examples where it will be effective or ineffective. Using fixed-rate budgets for encoding, it can reduce the state; it just won't be restored to useful values when decoded.

3. Consider sending audio data over a UDP (Unreliable Datagram Protocol) link. Assume the receiver is aware of which packets are lost and will make the best of the information it does receive. As in lab, the frequency packets are based on Fourier Transforms of time windows. Rank in order of subjective quality for humans based on your knowledge of audio processing and human psychoacoustics from this course (1-best, 6-worst). Justify your answers by explaining the impact of losing a packet in each case.

Packets are at most a few thousand bytes – think 2048 sample windows, so cover 10s of ms of sound; a single song is 3 minutes, so will be composed of thousands of packets. Packets are lost independently, even in the case of packet pairs.

- (a) 6 Packets contain PCM (raw, quantized time-sample data)
   Every lost data packet will result in silence for the length of time covered by the packet.
- (b) 3 Packets come in pairs for a time window with the highest frequency critical bands in one packet, and the rest in the second. In the atypical case in which there are only high or low frequencies, this will be perfect half the time (when the empty frequency set is lost). Typically, there will be both. If the high frequencies are lost, the sound is likely understandable but lower quality; telephone audio only represents data up 4K Hz. If only the high frequency packet is received, this time period will sound odd and any spoken words may be hard or impossible to understand.
- (c) 2 Packets come in pairs for a time window with the even timeslot PCM samples in one packet of the pair, and odd timeslot PCM samples in the other. Losing one packet of a pair will be equivalent to sampling at half the frequency for that time interval. As long as the sound has no frequency content higher than the one-quarter the original sampling rate, the sound will be perfectly reproduced (half for the half lost, half since the Nyquist sampling rate is twice the highest frequency component). If there are higher frequencies present, we will get aliasing effects for the frequencies between one-quarter and half the original sampling rate (assuming the original data was filtered to remove frequencies above half the sampling rate).
- (d) 5 Packets come in pairs for a time window, were the first packet contains the top 8b of the amplitude for all frequency and the second the low 8b.

It will depend on which packet is lost. If the packet with the low 8b of amplitude is lost, there may be little noise; 8b audio is understandable, and, in many cases, introduces little noise. If the high 8b of amplitude is lost, the time window may sound like noise.

(e) 1 Packets come in pairs for a time window where both the first and second packet in a pair contains the top one-third frequencies (by amplitude) in each critical band. The first packet also contains the middle one-third of the highest frequency critical bands, while the second packet contains the middle one-third of the remaining critical bands.

Loss is likely unnoticeable. The highest amplitude frequencies in a critical band will mask the lower frequencies. Since the highest (one-third) frequencies exist in both packets in a pair, reconstruction will be able to produce these frequencies even if one of the packets in the pair is lost.

(f) 4 Packets come in pairs for a time window, where the highest amplitude frequencies from each critical band are in one packet and the lowest in the other. It will depend on which packet is lost. If the packet with the low amplitude is lost, the result will be unnoticeable, as the high amplitude frequencies will mask the low amplitude frequencies. If the packet with the high amplitude frequencies is lost, the sound will not be reproduced properly. The important components are lost. The remaining components are likely not noise, but they are sounds that would typically not have been heard, so the result is only slightly better than silence.

1 and 6 should not be contraversial. There might be some wiggle room for 2. 3, 4, 5 are more debatable. Pointing out key features of each to support ranking is important thing to get for these.

- 4. Consider a FLASH memory with the following characteristic:
  - 64KB native flash pages
  - Opening a flash page takes  $25\mu s$
  - Once open, access within a flash page is 25 ns per Byte.
  - inodes and bnodes are 1KB blocks
  - must read all bytes in each 1KB block
  - (a) How long to read a 38KB file organized as one 1KB inode and 38 1KB bnodes, all of which are placed in the same 64KB flash page?  $25\mu s+(25 ns \times 1024) \times (38+1)=1,023,400 ns\approx 1.0 ms$

(b) How long to read a 38KB file organized as one 1KB inode and 38 1KB bnodes, each of which is placed in a different 64KB flash page? Each of the 39 nodes is in a separate page.  $(25\mu s+25 ns \times 1024) \times (38+1)=1,973,400 ns \approx 2.0 ms$  (c) Consider storing 4 files: A of size 512B, B of size 41KB, C of size 33KB, and D of size 49KB.

(assume all are 1 inode and  $\lceil size/1\text{KB} \rceil$  bnodes):

- i. How should we place these files into pages in order to minimize the access time for every file? (minimize pages used as a secondary goal.) Put A and C together in one page, and B and D each in their own pages.
- ii. How should we place these files into pages to minimize the number of 64KB pages used? (minimize access time as a secondary goal.) Quantify overall space saving percentage and per file read performance impact percentage.

One page contains all of A and B and 20 1KB bnode blocks from C (a total of 2+42+20=64 blocks); the second page contains all of D and the rest of B (inode block + 13 bnode blocks; so this becomes 50+1+13=64 blocks). This saves 1 of 3 pages or 33% compared to the accesstime-optimized version above.

- Access to files A, B, and D is not impacted.
- Access to file C is slowed by 3% ( $\frac{920400-895400}{895400}\approx 0.028)$ 
  - Performance packing:  $25\mu s + 25 ns \times 1024 \times 34 = 895,400 ns \approx 0.90 ms$
  - Space packing:  $25\mu s \times 2 + 25 ns \times 1024 \times 34 = 920,400 ns \approx 0.92 ms$

5. Consider the following Arduino Assembly code:

```
000010a2 <__udivmodsi4>:
    10a2: a1 e2
                        ldi r26, 0x21 ; 33
    10a4: 1a 2e
                        mov r1, r26
                        sub r26, r26
    10a6: aa 1b
    10a8: bb 1b
                        sub r27, r27
    10aa: fd 01
                        movw r30, r26
    10ac: 0d c0
                        rjmp .+26
                                        ; 0x10c8 <__udivmodsi4_ep>
000010ae <__udivmodsi4_loop>:
    10ae: aa 1f
                        adc r26, r26
    10b0: bb 1f
                        adc r27, r27
                        adc r30, r30
    10b2: ee 1f
    10b4: ff 1f
                        adc r31, r31
    10b6: a2 17
                        cp r26, r18
    10b8: b3 07
                        cpc r27, r19
    10ba: e4 07
                        cpc r30, r20
    10bc: f5 07
                        cpc r31, r21
    10be: 20 f0
                        brcs .+8
                                        ; 0x10c8 <__udivmodsi4_ep>
    10c0: a2 1b
                        sub r26, r18
    10c2: b3 0b
                        sbc r27, r19
    10c4: e4 Ob
                        sbc r30, r20
                        sbc r31, r21
    10c6: f5 0b
000010c8 <__udivmodsi4_ep>:
    10c8: 66 1f
                        adc r22, r22
    10ca: 77 1f
                        adc r23, r23
    10cc: 88 1f
                        adc r24, r24
    10ce: 99 1f
                        adc r25, r25
    10d0: 1a 94
                        dec r1
    10d2: 69 f7
                                        ; 0x10ae <__udivmodsi4_loop>
                        brne .-38
    10d4: 60 95
                        com r22
    10d6: 70 95
                        com r23
    10d8: 80 95
                        com r24
    10da: 90 95
                        com r25
    10dc: 9b 01
                        movw r18, r22
    10de: ac 01
                       movw r20, r24
                       movw r22, r26
    10e0: bd 01
    10e2: cf 01
                       movw r24, r30
    10e4: 08 95
                        ret
```

(a) Identify the top and bottom of the loop.

Loop ends at 0x10d2 where it branches back to the top at 0x10ae. The **brne** is the end of the loop where it conditionally branches back to the top.

(b) How many times does the loop execute?(Hint: What is the loop exit condition? What register holds the value tested for the exit condition? What happens to this register on each loop iteration? How is the register initialized?)The full loop executes 32 times, with one part of the loop

(0x10c8–0x10d2) executing 33 times. The loop exits when r1 becomes 0. r1 is holding the value.

r1 is decremented (dec r1) on every loop iteration. r1 is initialized to 33 in 0x10a2 and 0x10a4, where the ldi loads 33 into r26 and moves it to r1.

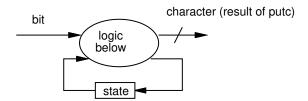
(c) What is the worst-case number of cycles from entering at 0x10a2 to performing the return at 0x10e4?

698

(instruction table on next to last page)

10a2: Idi r26, $0x21$ 1111 $10a4:$ mov r1, r261111 $10a4:$ mov r1, r261111 $10a6:$ sub r26, r261111 $10a8:$ sub r27, r271111 $10ae:$ movw r30, r261111 $10ae:$ adc r26, r2613232 $10b0:$ adc r27, r2713232 $10b1:$ adc r31, r3113232 $10b2:$ adc r30, r3013232 $10b4:$ adc r31, r3113232 $10b6:$ cp r26, r1813232 $10b6:$ cp r26, r1813232 $10b6:$ cp r30, r2013232 $10b6:$ cp cr31, r2113232 $10be:$ brcs .+823264 $10c0:$ sub r26, r1813232 $10c2:$ sbc r27, r1913232 $10c4:$ sbc r30, r2013232 $10c4:$ sbc r30, r2013232 $10c6:$ sbc r31, r2113232 $10c6:$ sbc r31, r2113333 $10ca:$ adc r23, r2313333 $10ca:$ adc r23, r2313333 $10ca:$ adc r25, r2513333 $10d2:$ brne3823366 $10d4:$ com r24111 $10d6:$ com r25111 $10d6:$ movw r18, r2211 </th <th>code</th> <th>cycles</th> <th>executed</th> <th>total</th>	code	cycles	executed	total
10a6: sub r26, r26111 $10a8: sub r27, r27$ 111 $10aa: movw r30, r26$ 111 $10aa: movw r30, r26$ 111 $10ac: rjmp .+26$ 212 $10ae: adc r26, r26$ 13232 $10b0: adc r27, r27$ 13232 $10b2: adc r30, r30$ 13232 $10b4: adc r31, r31$ 13232 $10b6: cp r26, r18$ 13232 $10b6: cp r26, r18$ 13232 $10ba: cpc r30, r20$ 13232 $10be: brcs .+8$ 23264 $10c0: sub r26, r18$ 13232 $10c4: sbc r30, r20$ 13232 $10c6: sbc r31, r21$ 13232 $10c6: sbc r31, r21$ 13333 $10c2: adc r22, r22$ 13333 $10c2: adc r25, r25$ 13333 $10d2: brne38$ 23366 $10d4: com r25$ 111 $10d6: con r23$ 111 $10de: movw r18, r22$ 111 $10de: movw r20, r24$ 111 $10e2: movw r24, r30$ 111	10a2: ldi r26, 0x21	1	1	1
10a8: sub r27, r27111 $10aa: movw r30, r26$ 111 $10ac: rjmp .+26$ 212 $10ae: adc r26, r26$ 13232 $10b0: adc r27, r27$ 13232 $10b2: adc r30, r30$ 13232 $10b4: adc r31, r31$ 13232 $10b6: cp r26, r18$ 13232 $10b6: cp r26, r18$ 13232 $10b6: cp r30, r20$ 13232 $10be: brcs .+8$ 232 $10be: brcs .+8$ 232 $10c0: sub r26, r18$ 13232 $10c2: sbc r31, r21$ 13232 $10c4: sbc r30, r20$ 13232 $10c4: sbc r30, r20$ 13232 $10c4: sbc r30, r20$ 13232 $10c4: sbc r31, r21$ 13232 $10c4: sbc r31, r21$ 13232 $10c4: sbc r31, r21$ 13333 $10c4: adc r22, r22$ 13333 $10c4: adc r23, r23$ 13333 $10d2: brne38$ 23366 $10d4: com r24$ 111 $10d6: com r23$ 111 $10de: movw r18, r22$ 111 $10de: movw r20, r24$ 111 $10de: movw r22, r26$ 111 $10e2: movw r24, r30$ 111	10a4: mov r1, r26	1	1	1
10aa: movw r30, r26111 $10ac: rjmp .+26$ 212 $10ae: adc r26, r26$ 13232 $10b0: adc r27, r27$ 13232 $10b2: adc r30, r30$ 13232 $10b4: adc r31, r31$ 13232 $10b6: cp r26, r18$ 13232 $10b6: cp r26, r18$ 13232 $10b6: cp cr30, r20$ 13232 $10ba: cpc r30, r20$ 13232 $10bc: cpc r31, r21$ 13232 $10bc: brcs .+8$ 23264 $10c0: sub r26, r18$ 13232 $10c4: sbc r30, r20$ 13232 $10c4: sbc r30, r20$ 13232 $10c4: sbc r31, r21$ 13232 $10c6: sbc r31, r21$ 13232 $10c6: sbc r31, r21$ 13232 $10c6: sbc r31, r21$ 13333 $10ca: adc r22, r22$ 13333 $10ca: adc r23, r23$ 13333 $10dc: com r23, r23$ 111 $10d6: com r23$ 111 $10d6: com r24$ 111 $10de: movw r18, r22$ 111 $10de: movw r20, r24$ 111 $10e2: movw r24, r30$ 111	10a6: sub r26, r26	1	1	1
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10b2: adc r30, r301 $32$ $32$ $10b4: adc r31, r31$ 1 $32$ $32$ $10b6: cp r26, r18$ 1 $32$ $32$ $10b8: cpc r27, r19$ 1 $32$ $32$ $10ba: cpc r30, r20$ 1 $32$ $32$ $10bc: cpc r31, r21$ 1 $32$ $32$ $10bc: sub r26, r18$ 1 $32$ $32$ $10c0: sub r26, r18$ 1 $32$ $32$ $10c2: sbc r27, r19$ 1 $32$ $32$ $10c4: sbc r30, r20$ 1 $32$ $32$ $10c6: sbc r31, r21$ 1 $32$ $32$ $10c6: sbc r31, r21$ 1 $32$ $32$ $10c8: adc r22, r22$ 1 $33$ $33$ $10ca: adc r23, r23$ 1 $33$ $33$ $10cc: adc r24, r24$ 1 $33$ $33$ $10d0: dec r1$ 11 $33$ $33$ $10d2: brne38$ 2 $33$ $66$ $10d4: com r22$ 111 $10d6: com r23$ 111 $10da: com r25$ 111 $10dc: movw r18, r22$ 111 $10de: movw r20, r24$ 111 $10e2: movw r24, r30$ 111	10ae: adc r26, r26	1	32	32
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10ba: cpc r30, r201 $32$ $32$ $10bc: cpc r31, r21$ 1 $32$ $32$ $10be: brcs .+8$ 2 $32$ $64$ $10c0: sub r26, r18$ 1 $32$ $32$ $10c2: sbc r27, r19$ 1 $32$ $32$ $10c4: sbc r30, r20$ 1 $32$ $32$ $10c6: sbc r31, r21$ 1 $32$ $32$ $10c6: sbc r31, r21$ 1 $32$ $32$ $10c8: adc r22, r22$ 1 $33$ $33$ $10ca: adc r23, r23$ 1 $33$ $33$ $10ce: adc r25, r25$ 1 $33$ $33$ $10dc: dec r1$ 1 $33$ $33$ $10d2: brne38$ 2 $33$ $66$ $10d4: com r22$ 111 $10d6: com r23$ 111 $10da: com r25$ 111 $10de: movw r18, r22$ 111 $10e0: movw r20, r24$ 111 $10e2: movw r24, r30$ 111	10b6: cp r26, r18	1	32	32
10bc: cpc r31, r2113232 $10be: brcs .+8$ 23264 $10c0: sub r26, r18$ 13232 $10c2: sbc r27, r19$ 13232 $10c4: sbc r30, r20$ 13232 $10c6: sbc r31, r21$ 13232 $10c6: sbc r31, r21$ 13232 $10c6: sbc r31, r21$ 13333 $10c6: adc r22, r22$ 13333 $10ca: adc r23, r23$ 13333 $10cc: adc r24, r24$ 13333 $10ce: adc r25, r25$ 13333 $10d2: brne38$ 23366 $10d4: com r22$ 111 $10d6: com r23$ 111 $10d6: com r25$ 111 $10dc: movw r18, r22$ 111 $10de: movw r20, r24$ 111 $10e0: movw r24, r30$ 111	10b8: cpc r27, r19	1	32	32
10be: brcs .+823264 $10c0: sub r26, r18$ 13232 $10c2: sbc r27, r19$ 13232 $10c4: sbc r30, r20$ 13232 $10c6: sbc r31, r21$ 13232 $10c8: adc r22, r22$ 13333 $10ca: adc r23, r23$ 13333 $10ce: adc r24, r24$ 13333 $10ce: adc r25, r25$ 13333 $10d2: brne38$ 23366 $10d4: com r22$ 111 $10d6: com r23$ 111 $10d6: com r25$ 111 $10de: movw r18, r22$ 111 $10e: movw r20, r24$ 111 $10e: movw r24, r30$ 111	10ba: cpc r30, r20	1	32	32
10c0: sub r26, r181 $32$ $32$ $10c2: sbc r27, r19$ 1 $32$ $32$ $10c4: sbc r30, r20$ 1 $32$ $32$ $10c6: sbc r31, r21$ 1 $32$ $32$ $10c8: adc r22, r22$ 1 $33$ $33$ $10ca: adc r23, r23$ 1 $33$ $33$ $10cc: adc r24, r24$ 1 $33$ $33$ $10ce: adc r25, r25$ 1 $33$ $33$ $10d0: dec r1$ 1 $33$ $33$ $10d2: brne38$ 2 $33$ $66$ $10d4: com r22$ 111 $10d6: com r23$ 111 $10da: com r25$ 111 $10dc: movw r18, r22$ 111 $10e: movw r20, r24$ 111 $10e: movw r24, r30$ 111	10bc: cpc r31, r21	1	32	32
10c2: sbc r27, r191 $32$ $32$ $10c4: sbc r30, r20$ 1 $32$ $32$ $10c6: sbc r31, r21$ 1 $32$ $32$ $10c8: adc r22, r22$ 1 $33$ $33$ $10ca: adc r23, r23$ 1 $33$ $33$ $10cc: adc r24, r24$ 1 $33$ $33$ $10ce: adc r25, r25$ 1 $33$ $33$ $10d0: dec r1$ 1 $33$ $33$ $10d2: brne38$ 2 $33$ $66$ $10d4: com r22$ 111 $10d6: com r23$ 111 $10da: com r25$ 111 $10dc: movw r18, r22$ 111 $10e: movw r20, r24$ 111 $10e2: movw r24, r30$ 111	10be: brcs $.+8$	2	32	64
10c4: sbc r30, r201 $32$ $32$ $10c6: sbc r31, r21$ 1 $32$ $32$ $10c8: adc r22, r22$ 1 $33$ $33$ $10ca: adc r23, r23$ 1 $33$ $33$ $10cc: adc r24, r24$ 1 $33$ $33$ $10ce: adc r25, r25$ 1 $33$ $33$ $10d0: dec r1$ 1 $33$ $33$ $10d2: brne38$ 2 $33$ $66$ $10d4: com r22$ 111 $10d6: com r23$ 111 $10d8: com r24$ 111 $10dc: movw r18, r22$ 111 $10e: movw r20, r24$ 111 $10e: movw r24, r30$ 111	10c0: sub r26, r18	1	32	32
10c6: sbc r31, r2113232 $10c8: adc r22, r22$ 13333 $10ca: adc r23, r23$ 13333 $10cc: adc r24, r24$ 13333 $10ce: adc r25, r25$ 13333 $10d0: dec r1$ 13333 $10d2: brne38$ 23366 $10d4: com r22$ 111 $10d6: com r23$ 111 $10d8: com r24$ 111 $10da: com r25$ 111 $10de: movw r18, r22$ 111 $10e0: movw r20, r24$ 111 $10e2: movw r24, r30$ 111	10c2: sbc r27, r19	1	32	32
10c8: adc r22, r2213333 $10ca: adc r23, r23$ 13333 $10cc: adc r24, r24$ 13333 $10ce: adc r25, r25$ 13333 $10d0: dec r1$ 13333 $10d2: brne38$ 23366 $10d4: com r22$ 111 $10d6: com r23$ 111 $10d8: com r24$ 111 $10de: movw r18, r22$ 111 $10de: movw r20, r24$ 111 $10e0: movw r24, r30$ 111	10c4: sbc r30, r20	1	32	32
10ca: adc r23, r2313333 $10cc: adc r24, r24$ 13333 $10ce: adc r25, r25$ 13333 $10d0: dec r1$ 13333 $10d2: brne38$ 23366 $10d4: com r22$ 111 $10d6: com r23$ 111 $10d8: com r24$ 111 $10da: com r25$ 111 $10dc: movw r18, r22$ 111 $10e: movw r20, r24$ 111 $10e: movw r24, r30$ 111	10c6: sbc r31, r21	1	32	32
10cc: adc r24, r2413333 $10ce: adc r25, r25$ 13333 $10d0: dec r1$ 13333 $10d2: brne38$ 23366 $10d4: com r22$ 111 $10d6: com r23$ 111 $10d8: com r24$ 111 $10da: com r25$ 111 $10dc: movw r18, r22$ 111 $10de: movw r20, r24$ 111 $10e0: movw r24, r30$ 111	10c8: adc r22, r22	1	33	33
10ce: adc r25, r2513333 $10d0: dec r1$ 13333 $10d2: brne38$ 23366 $10d4: com r22$ 111 $10d6: com r23$ 111 $10d8: com r24$ 111 $10da: com r25$ 111 $10dc: movw r18, r22$ 111 $10de: movw r20, r24$ 111 $10e2: movw r24, r30$ 111	10ca: adc r23, r23	1	33	33
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	10cc: adc r24, r24	1	33	33
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	10ce: adc r25, r25	1	33	33
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	10d0: dec r1	1	33	33
10d6: com r2311110d8: com r2411110da: com r2511110dc: movw r18, r2211110de: movw r20, r2411110e0: movw r22, r2611110e2: movw r24, r30111	10d2: brne38	2	33	66
10d8: com r2411110da: com r2511110dc: movw r18, r2211110de: movw r20, r2411110e0: movw r22, r2611110e2: movw r24, r30111	10d4:  com  r22	1	1	1
10da: com r2511110dc: movw r18, r2211110de: movw r20, r2411110e0: movw r22, r2611110e2: movw r24, r30111	10d6:  com  r23	1	1	1
10dc: movw r18, r2211110de: movw r20, r2411110e0: movw r22, r2611110e2: movw r24, r30111	10d8:  com  r24	1	1	1
10de: movw r20, r2411110e0: movw r22, r2611110e2: movw r24, r30111	10da: com r $25$	1	1	1
10e0: movw r22, r26       1       1       1         10e2: movw r24, r30       1       1       1	10dc: movw r18, r22	1	1	1
10e2: movw r24, r30         1         1         1	10de: movw r20, r24	1	1	1
	10e0: movw r22, r26	1	1	1
1004: rot $1$	10e2: movw r24, r30	1	1	1
	10e4: ret	4	1	4
698				698

6. Consider the following FSM for decoding serial, Huffman encoded data into characters.



```
int state=START;
while(true) {
 int bit=nextInputBit();
 switch(state) {
 case START: if (bit==0) state=S0; else state=S1; break;
 case S0: if (bit==0) state=S00; else state=S01; break;
 case S1: if (bit==0) state=S10; else state=S11; break;
 case S00: if (bit==0) state=S000; else{ state=START; putc('E'); } break;
 case S01: if (bit==0) state=S010; else state=S011; break;
 case S10: if (bit==0) state=S100; else {state=START; putc(' ');} break;
 case S11: if (bit==0) state=S110; else state=S111; break;
 case S000: if (bit==0) state=S0000; else {state=START; putc('H');} break;
 case S010: if (bit==0) {state=START; putc('R');} else {state=START; putc('S');} break;
 case S011: if (bit==0) {state=START; putc('N');} else state=S0111; break;
 case S100: if (bit==0) {state=START; putc('I');} else {state=START; putc('O');} break;
 case S110: if (bit==0) {state=START; putc('A');} else state=S1101; break;
 case S111: if (bit==0) {state=START; putc('T');} else state=S1111; break;
 case S0000: if (bit==0) {state=START; putc('C');} else {state=START; putc('U');} break;
 case S0111: if (bit==0) state=S01110; else {state=START; putc('L');} break;
 case S1101: if (bit==0) state=S11010; else {state=START; putc('D');} break;
 case S1111: if (bit==0) state=S11110; else state=S11111; break;
 case S01110: if (bit==0) {state=START; putc('B');} else {state=START; putc('P');}
               break;
 case S11010: if (bit==0) {state=START; putc('G');} else {state=START; putc('W');}
               break;
 case S11110: if (bit==0) {state=START; putc('Y');} else state=S111101; break;
 case S11111: if (bit==0) {state=START; putc('F');} else {state=START; putc('M');}
               break;
 case S111101: if (bit==0) {state=START; putc('V');} else state=S1111011; break;
 case S111011: if (bit==0) state=S1110110; else {state=START; putc('K');} break;
 case S1110110:if (bit==0) {state=START; putc('X');} else state=S11101101; break;
 case S11101101:if (bit==0) {state=START; putc('Q');} else state=S111011011; break;
 case S111011011:if (bit==0) {state=START; putc('Z');} else {state=START; putc('J');}
                  break;
               }
 }
```

- (a) What is the minimum number of state bits needed to encode state for a hardware implementation? Why?
  (Hint: different from the 16b or 32b that might be used to encode an int in C.) 5b, because there are 26 states. [log<sub>2</sub>(26)] = 5
- (b) What is the encoding for the following letters:

letter	encoding
А	1100
В	011100
Е	001
Y	111100

(c) What letters can be encoded with each of the following number of bits:

bits to encode	encoding
1	
2	
3	E, space
4	HRSNIOAT
5	C U L D
6	BPGWYFM
7	VK
8	X

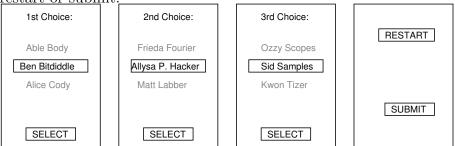
(d) Using the encoding, how many bits does it require to encode:

W	Е		А	L	L		L	Ι	V	Е		Ι	N		А	
Y	Е	L	L	Ο	W		S	U	В	М	А	R	Ι	Ν	Е	
	144															

- 7. Consider a smartphone Application User Interface for requesting a partner assignment for lab, where the user gets to submit a prioritized list of 3 choices. Valid selections must be a student in the course which you have not worked with on previous labs.
  - (a) Considering the UI design issues discussed in class, identify strengths and weaknesses of each of the following (at least one of each):
    - i. <u>Text fields to type in 3 names and submit button</u>.

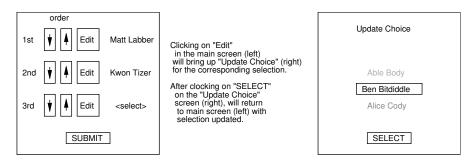
1st Choice:
2nd Choice:
3rd Choice:
SUBMIT

- strength: how to use interface is clear
- strength: can see selection all together before submit
- weakness: does not prevent invalid selections (e.g., students not in class, students who have already partnered with)
- ii. Sequence of three menus/scrolling pickers to select from all students who have not previously partnered (40-n), where n is week of lab. End with option to restart or submit.



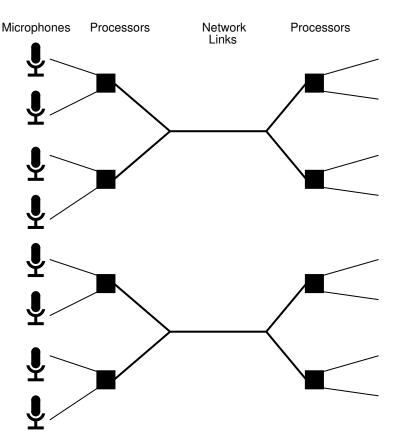
- strength: prevents invalid selections—only allows selection from valid list
- weakness: if make mistake or change your mind must start over
- weakness: does not show what selection will be in one place before submit

iii. Default 1st and 2nd selections to highest unassigned student from previous preferences. List current selections in order. Click on selection for scrolling picker to select (update choice). Up/down buttons to order. Submit button.



- strength: prevents invalid selections—only allows selection from valid list
- strength: reduces work by preselecting likely choices; in typical case only need to make one selection rather than 3
- strength: can see selection all together before submit
- weakness: more complicated interface; may be less clear how to use
- weakness: may be too easy to accidentally submit before ready
- (b) Suggest an interface that is better than the options above; it may be an improvement to one of the above, a mix-and-match of features, or a completely new design.
  - ii add summary of selections on final selection page; add option to go back and edit a selection
  - iii Default 3rd option to random students, so possibly no need for selection. Add review confirmation screen for submit (maybe it's too easy to accidentally submit?). Show current choices on selection screen. Maybe remove up/down arrows (both or only up or down) to simplify.

8. Consider a scenario where audio data is collected at a number of points and sent over network links to a central location.



- PCM samples: 44KHz sample rate for each input channel at 16b/sample
- For compression (and decompression), each input channel is processed in 2048 point FFT windows
- context switch processor between channels every 2048 samples (matches window size for compression case)
- Processor runs at 1 GHz; can handle many audio channels depending on computation required.
- 20 cycles to handle each uncompressed sample
- 200 cycles of computation per sample for (de)compression
- 20,480 cycles to switch context (channels)
- Frequency transformed and MP3 compressed data is 128Kb/s per channel.
- Network link is 100 Mb/s
- Processor is \$25; network link is \$250.

- (a) With one processor on each end and a single network link, how many uncompressed PCM sample channels = 150, limited by the bandwidth on the network link.
  Processor: (20 + 20480/2048) instructions /sample × 44,000 samples/sec/channel = 1.3M instructions/sec/channel.
  (10<sup>9</sup> instructions/sec)/1.3×10<sup>6</sup> instructions/sec/channel 757.57≈ 760 channels/processor.
  Network link: (100×2<sup>20</sup>b/s)/(44,000 × 16b/s/channel) = 148.945≈ 150 channels/network link.
- (b) With one processor on each end and a single network link, how many MP3 compressed channels can the system support? What resource sets the limit? MP3 compressed channels=110, limited by the bandwidth on the processor (de)compression capacity. Processor:  $(200 + \frac{20480}{2048})$  instructions /sample × 44,000 samples/sec/channel = 9.24M instructions/sec/channel.  $(10^9 \text{ instructions/sec})/9.24 \times 10^6 \text{ instructions/sec/channel} = 108.225 \approx 110 \text{ channels/processor}.$ Network link:  $(100 \times 2^{20} \text{ b/s})/(128 \times 1024 \text{ b/s/channel}) = 800 \text{ channels/network link}.$
- (c) What combination of processors, network links, and compression should you use to support 1000 channels at minimum cost? Include the final cost for the solution in your answer.

	Processors	Net		
	each End	Links	Cost	
Compressed	1000/110	1000/800	$2 \times 25 \times 10 + 2 \times 250$	
	10	2	\$1,000	Minimum
Uncompressed	1000/760	1000/150	$2 \times 25 \times 2 + 7 \times 250$	
	2	7	\$1,850	

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Band Number	Low	High
1	20	100
2	100	200
3	200	300
4	300	400
5	400	510
6	510	630
7	630	720
8	720	920
9	920	1080
10	1080	1370
11	1270	1480
12	1480	1720
13	1720	2000
14	2000	2320
15	2320	2700
16	2700	3150
17	3150	3700
18	3700	4400
19	4400	5300
20	5300	6400
21	6400	7700
22	7700	9500
23	9500	12000
24	12000	15500

Human auditory critical bands:

Arduino (AVR) Instructions:

Instruction	Operands	Description	Operation	# Clocks
add	Rd, Rr	add registers no carry	$Rd \leftarrow Rd + Rr$	1
adc	Rd, Rr	add registers with carry	$Rd \leftarrow Rd + Rr + C$	1
brcs	k	<del>branch if not equal</del> branch if	if (C=1) then $PC \leftarrow PC+k+1$	2
		carry set		
brne	k	<del>branch if carry set</del> branch if	if (Z=0) then $PC \leftarrow PC+k+1$	2
		not equal		
com	Rd	One's Complement	$Rd \leftarrow 0XFF-Rd$	1
ср	Rd, Rr	Compare	Rd-Rr	1
cpc	Rd, Rr	Copmare with carry	Rd-Rr-C	1
dec	Rd	Decrement	$\mathrm{Rd} \leftarrow \mathrm{Rd}\text{-}1$	1
ldi	Rd, k	Load Immediate	$RD \leftarrow k$	1
mov	Rd, Rr	Move Between Registers	$\mathrm{Rd} \leftarrow \mathrm{Rr}$	1
movw	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	1
ret		Subroutine Return	$PC \leftarrow STACK$	4
rjmp	k	Relative Jump	$PC \leftarrow PC+k+1$	2
sub	Rd, Rr	subtract registers no carry	$\mathrm{Rd} \leftarrow \mathrm{Rd}\text{-}\mathrm{Rr}$	1
subc	Rd, Rr	subtract registers with carry	$\mathrm{Rd} \leftarrow \mathrm{Rd}\text{-}\mathrm{Rr}\text{-}\mathrm{C}$	1

## Code of Academic Integrity

Since the University is an academic community, its fundamental purpose is the pursuit of knowledge. Essential to the success of this educational mission is a commitment to the principles of academic integrity. Every member of the University community is responsible for upholding the highest standards of honesty at all times. Students, as members of the community, are also responsible for adhering to the principles and spirit of the following Code of Academic Integrity.\*

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Activities that have the effect or intention of interfering with education, pursuit of knowledge, or fair evaluation of a students performance are prohibited. Examples of such activities include but are not limited to the following definitions:

**A. Cheating** Using or attempting to use unauthorized assistance, material, or study aids in examinations or other academic work or preventing, or attempting to prevent, another from using authorized assistance, material, or study aids. Example: using a cheat sheet in a quiz or exam, altering a graded exam and resubmitting it for a better grade, etc.

**B.** Plagiarism Using the ideas, data, or language of another without specific or proper acknowledgment. Example: copying another persons paper, article, or computer work and submitting it for an assignment, cloning someone elses ideas without attribution, failing to use quotation marks where appropriate, etc.

**C. Fabrication** Submitting contrived or altered information in any academic exercise. Example: making up data for an experiment, fudging data, citing nonexistent articles, contriving sources, etc.

**D.** Multiple Submissions Multiple submissions: submitting, without prior permission, any work submitted to fulfill another academic requirement.

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**G. Unfair Advantage** Attempting to gain unauthorized advantage over fellow students in an academic exercise. Example: gaining or providing unauthorized access to examination materials, obstructing or interfering with another students efforts in an academic exercise, lying about a need for an extension for an exam or paper, continuing to write even when time is up during an exam, destroying or keeping library materials for ones own use., etc.

\* If a student is unsure whether his action(s) constitute a violation of the Code of Academic Integrity, then it is that students responsibility to consult with the instructor to clarify any ambiguities.