



Penn Engineering **ESE**



Lecture #13 – Intellectual Property ESE150 Spring 2019

**ESE 150 –
DIGITAL AUDIO BASICS**



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PRECLASS

- × **Cost to develop and write a book?**
 - + 200 days @ \$500/day
- × **Cost per book (assume \$1 to print book)**
 - + Total volume 1
 - + Total volume 10,000
 - + Total volume 1 million
- × **Book sells \$10**
 - + Value added by writer?
 - + Copies sold to break even at \$2/copy to writer?

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ECONOMIC TERMS

- × **Production cost – expense to produce**
- × **Price – what consumer will pay for it**
 - + Value to consumer
- × **Profit = Price – cost**

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OBSERVE

- × **Creative / Intellectual work produces most of value**
- × **At least in volume, physical costs of reproduction is small part of product price**

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PRECLASS CONTINUED

- × **Cost to photocopy 200 page book at \$0.05/page?**
- × **Cost to scan book at 10page/minute?**
- × **Cost to retype book (50 words/minute type)?**
- × **Cost to perform a 10s copy onto flash drive?**
- × **Cost of portion of flash drive used**
 - + \$8 for 16GB drive, 0.5MB file

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OBSERVE

- × **With digital representation**
 - + Cost of “physical” reproduction trends to 0

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PAST

- × **Much of value in physical construction of objects**
 - + Bridge, house, car, screwdriver
- × **Expensive to reproduce / copy**
- × **Reproductions imperfect**
 - + 5th generation analog recording
 - + 4th generation photocopy of text
- × **Inherent barrier to making copies**
 - + Value to buying original

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DIGITAL REPRESENTATION

- × **Can represent perfectly in bits**
 - + Including sound, words
- × **Can make perfect copies**
- × **Bits are cheap...and getting cheaper**
 - + Copying "free"
- × **Intellectual value disconnected from physical reproduction**

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WHAT ELSE HAS THIS PROPERTY?

| Digital Intellectual Property | Physical IP Renderer |
|-------------------------------|------------------------------|
| Novel | eReader |
| Song (MP3) | MP3 Player |
| JPEG Photo | Video Player |
| Video Game | Arduino or Personal Computer |
| Verilog digital circuit | Web Server |
| STL (3D CAD drawing) | DNA Printer |
| DNA Sequence | |

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INTELLECTUAL PROPERTY

- × **Intangible creations of human intellect**
- × **Have value**
- × **Don't necessarily have physical embodiment on their own**

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INTELLECTUAL PROPERTY CREATORS

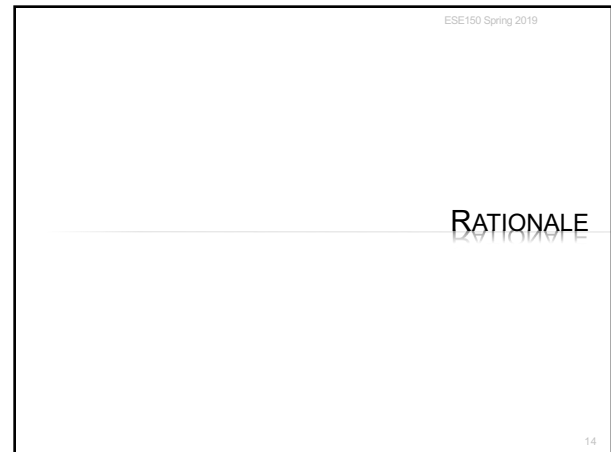
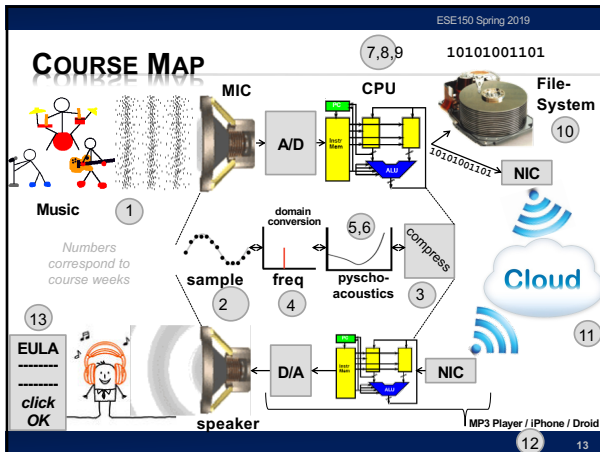
- × **As Engineers**
 - + Program, develop algorithms, design circuits
- × **Almost everything we create will have this property**
 - + Value added is intellectual
 - + Can be represented digitally in bits
 - + Can (increasingly) be copied/reproduced cheaply
- × **Easy to have impact**
 - + Our solutions can reach millions, billions
 - + Decreasing physical barriers to propagation of solutions
- × **Challenge to protect and reward IP creators**

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OUTLINE

- × **Setup Need / Opportunity – What is IP**
- × **Where are we**
- × **Rationale for IP Protection – Why Protect**
- × **How protect?**
 - + Patents
 - + Copyrights
 - + Open Source
 - + NDA
 - + Licensing

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PRICING CHALLENGE

- ✘ **When cost of copying $\rightarrow 0$**
 - + Inventor/author must recover development cost
 - ✘ Price must include develop cost + copy cost
 - + Copier does not have development cost
 - ✘ Price = copy cost + epsilon
 - ✘ Competition of copiers will drive epsilon down near 0
 - + Inventor/author not compensated for development
 - ✘ Remove incentive/reward for development
- ✘ **Demand: developers need way to exclude others from copying to incentivize creation**

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ARROW'S INFORMATION PARADOX

- ✘ **Customer not know how to value information until see information (see details of product)**
 - + Enough information to decide to buy
 - + Enough information to decide what will pay for it
- ✘ **Once show customer information, sufficient detail, they have enough information to reproduce**
 - + Could walk away and produce their own without paying for it
- ✘ **Disclosure of what effectively transfers technology**
- ✘ **Demand: protection for developer**
 - + Arrow, Kenneth J. Economic Welfare and the Allocation of Resources for Invention, in *The Rate and Direction of Inventive Activity*, 609 (Nat'l Bureau of Econ. Research ed. 1962).

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BALANCE INDIVIDUAL AND SOCIETAL GOOD

- ✘ **Individual should benefit from their own effort**
- ✘ **Society advances with the accumulation of knowledge**

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BEFORE COPYING WAS AN ISSUE

- ✘ **Concern that new developments/ideas would be lost when inventor die**
 - + Techniques could remain secret for decades!
- ✘ **Incentive to make inventions known**
 - + Advance the general welfare

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US CONSTITUTION

- × **Article 1, Section 8, Clause 8:**
 - + To promote the Progress of Science and useful Arts, by securing for limited Times to Authors and Inventors the exclusive Right to their respective Writings and Discoveries

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MECHANISMS (TO SUPPORT)

- × **Patents**
 - + Cover inventions
 - + E.g., Flying Machine (US 821,393) ENIAC (US 3,120,606),
- × **Copyrights**
 - + Creative expression
 - + E.g., novel, song, movie

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MECHANISMS FOR PROTECTION

- × **Messy and imperfect**
- × **Haven't kept up with technology**
- × **Likely need (and will need) innovation and refinement**

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INTERLUDE: NIL
NIKOLAI IVANOVICH LOBACHEVSKY

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PATENTS

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PATENT

- × **Inventions**
- × **Non-obvious to one "ordinary skill in art"**
- × **Reduced to practice**
- × **Cannot patent**
 - + Abstract ideas
 - + Laws of nature
- × **US: First to file**
 - + (prior to 2013 was first to invent)
- × **Exclusive rights 20 years from filing**

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WHAT MIGHT BE TRICKY / NON-SATISFYING?

- ✗ **First to file? (even invent?)**
- ✗ **20 year term?**

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PATENT

- ✗ **Identification of problem is part of invention**
- ✗ **Claims**
 - + Define the invention
 - + Technical coverage
- ✗ **Requires disclosure**
 - + If really believe no one else will figure it out...or can copy it, maybe better to keep as a *trade secret*
- ✗ **License to litigate**
 - + Recover damages is through litigation
 - + Establish violation
 - + Validity of many patents overturned in litigation

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PATENT PROCESS

- ✗ **US have one year from first-public disclosure to file**
 - + Many places – public disclosure prevent patent
 - + <https://www.uspto.gov/web/offices/pac/mpep/s2153.html>
- ✗ **File provisional patent to get filing date**
- ✗ **Reviewed by examiner**
- ✗ **Examiner reports on what may be allowable**
 - + As-is
 - + With tighter qualifications
 - + Not-at-all
 - + On a per-claim basis
- ✗ **Typically requires several iterations**
- ✗ **Often year(s) before patent issues**
- ✗ **Filing costs thousands of dollars**
 - + With lawyer/legal fees tens to hundreds of thousands

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US10261794B2

(12) **United States Patent** (10) **Patent No.:** US 10,261,794 B2
DeHon (45) **Date of Patent:** Apr. 16, 2019

(54) **TECHNIQUES FOR METADATA PROCESSING** (56) **References Cited**

(71) Applicant: **The Charles Stark Draper Laboratory, Inc., Cambridge, MA (US)** 5,201,056 A 4/1993 David et al.
 6,298,432 B1 10/2001 Goto
 (Continued)

(72) Inventor: **Andre' DeHon, Philadelphia, PA (US)**

(73) Assignee: **The Charles Stark Draper Laboratory, Inc., Cambridge, MA (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 15/695,541

(22) Filed: Sep. 5, 2017

(65) **Prior Publication Data**
 US 2018/0011708 A1 Jan. 11, 2018

Related U.S. Application Data

(60) Division of application No. 15/426,098, filed on Feb. 7, 2017, now Pat. No. 9,785,440, which is a (Continued)

(57) **ABSTRACT**
 Techniques are described for metadata processing that can be used to encode an arbitrary number of security policies for code running on a processor. Metadata may be added to

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What is claimed is:

1. A method of processing computer instructions on a computer processor comprising:

- receiving a current instruction for metadata processing performed in a metadata processing domain that is isolated from a code execution domain including the current instruction;
- determining, by the metadata processing domain in connection with metadata for the current instruction, whether to allow execution of the current instruction in accordance with a set of one or more policies, wherein the one or more policies include a set of rules that enforce execution of a complete sequence of instructions in a specified order from a first instruction of the complete sequence to a last instruction of the complete sequence, the set of rules including a first rule and a second rule;
- performing metadata processing of the first rule for the first instruction, wherein the metadata processing of the first rule includes setting a program counter tag of a program counter used for a next instruction following runtime execution of the first instruction to a special tag value indicating that the next instruction is part of the complete sequence of instructions;

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US005742180A

United States Patent [19] (11) **Patent Number:** 5,742,180
DeHon et al. (45) **Date of Patent:** Apr. 21, 1998

(54) **DYNAMICALLY PROGRAMMABLE GATE ARRAY WITH MULTIPLE CONTEXTS**

(75) Inventors: **Andre' DeHon, Cambridge; Thomas F. Knight, Jr., Belmont; Edward Tau, Boston; Michael Bolecki, Somerville; Ian Edick, Cambridge; Derrick Chen, Cambridge; Jeremy Brown, Cambridge, all of Mass.**

(73) Assignee: **Massachusetts Institute of Technology, Cambridge, Mass.**

(21) Appl. No.: 386,851

(22) Filed: Feb. 16, 1995

(51) Int. Cl.⁵ H03K 19/177

(52) U.S. Cl. 326/40; 326/38

(58) Field of Search 326/38-40, 46

(56) **References Cited**
 U.S. PATENT DOCUMENTS
 4,336,601 6/1982 Tanaka 364/900
 4,354,228 10/1982 Moore et al. 364/200
 4,493,026 1/1983 Tibshirani 364/200

Denneau, M.M., "The Yorktown Simulation Engine," *IEEE 19th Design Automation Conference*, pp. 55-59 (1982).

Razdan, R., et al., "A High Performance Microarchitecture with Hardware-Programmable Functional Units," *Micro-21 Proceedings of the 27th Annual International Symposium on Microarchitecture*, San Jose, California, pp. 172-180 (Nov. 30-Dec. 2, 1994).

(List continued on next page.)

ABSTRACT
 An integrated dynamically programmable gate array comprises a two dimensional array of programmable gates. These gates can be implemented as look up tables but hardware gates with programmable interconnections are also possible. Each one of the gates receives plural input logic signals from plural other gates. Consequently, a broad range of logic combinations are possible. The gates further include locally stored multiple contexts dictating different combinatorial logic operations performed by the gates. The contexts increase the logic operations performable by the gate and the fact that the contexts are locally stored enables

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CLAIMS

We claim:

1. An integrated dynamically programmable logic array, comprising:
 - at least a two dimensional array of programmable logic elements, each one of the logic elements receiving plural input logic signals from plural other logic elements and including locally stored multiple contexts dictating different combinatorial logic operations performed by the logic elements; and
 - a context signal source that provides a context signal, indicating an active one of the contexts, commonly to the programmable logic elements of the array; and
 - wherein the contexts for each one of the logic elements are individually accessible so that a new context can be loaded into the logic elements while another context is controlling logic operations of the logic elements.
2. A programmable logic array as described in claim 1, wherein the context signal source provides the context signal up to every cycle of the programmable logic array.
3. A programmable logic array as described in claim 1, wherein the context signal source generates plural context signals that dictate contexts for regions of the array of the logic elements.

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WHAT'S PATENTABLE

- × **Not law's of nature**
- × **Not abstract ideas**
- × **Cannot patent pi (π)**
- × **Software?**
 - + Originally not
 - + With reference to machine, can often manage
- × **Genetic sequences?...**
- × **...evolving...**

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ADMINISTRATIVE INTERLUDE: FINAL

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FINAL

- × **Final Office Hours:**
 - + Saturday 6pm
 - + Sunday 4pm and 5pm
- × **Final: Monday (5/6) 3-5pm in Moore 212**
 - + Same Rules as midterm
 - × Calculators allowed (work that out in advance)
 - × Closed book, notes
 - + 15% of grade
 - + Comprehensive
 - + Last year final and answers linked to Spring 2018 syllabus
 - × Probably mix ideas from first and second half

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FINAL TOPICS

| Pre Midterm | Post midterm |
|-------------------------------|-----------------------------|
| × Data representation in bits | × Combinational Logic |
| × Sounds waves | × Finite-State Machines |
| × Sampling | × Stored-Program Processors |
| × Quantization | × Processing Requirements |
| × Nyquist | × Process Virtualization |
| × Lossy/lossless compression | × Persistent Storage |
| × Common case | × File Systems |
| × Frequency domain | × Networking |
| × Psychoacoustics | × User Interface |
| × Perceptual coding | × Intellectual Property |

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COPYRIGHT

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COPYRIGHT

- × **Cover particular, original expression**
 - + Including software
- × **Technically don't need to register**
 - + But should...
 - + Must register before sue for infringement
 - + \$35
 - + No review, just registration
- × **Life of author + 70 years**
- × **Work for hire: 95 years from publication**

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TRADITIONALLY: TRANSFER COPYRIGHT ...

- × **Publish in ACM, IEEE journal**
 - + Transfer copyright to them, they license you back rights for derived work and post on person web site.

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DOI: <http://dx.doi.org/10.1145/3020078.3026124>

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LICENSING

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LICENSE

- × **Where have you seen licenses?**

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LICENSES

- × **How get right to use**
 - + Something patented, copyrighted by someone else
- × **Between companies**
 - + Get IP need to build a product
- × **To consumers**
 - + Technically, most software is licensed, not sold
 - + ...shrink-wrap licensing agreements...
- × **Define terms of use**
 - + What you are paying for (one copy, many, resale...)
 - + What uses (dis)allowed

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DIRECT LICENSING/SALES

PAST

- × **Selling a product require huge infrastructure and up-front capital costs**
 - + Manufacture (physical things)
 - + Marketing
 - + Distribution
 - + Sales
- × **Demand large business to support infrastructure**
- × **Not easy for individual**

TODAY (EMERGING)

- × **Eliminate infrastructure needs with ubiquitous networking, IP products, service businesses**
 - + Manufacture (physical things) → not issue for IP
 - × ...or licensed manufacturing
 - + Marketing → still need to get the word out
 - × ...can use web at low cost
 - + Distribution → not an issue for IP
 - × ...leverage common carriers
 - + Sales
 - × Handle online, eBusiness support
- × **Becomes possible for individuals/small businesses to sell IP directly to consumers**

DIRECT IP BUSINESSES TODAY

- × **Examples?**

DIRECT IP BUSINESSES TODAY

- × **Kindle Direct Publishing**
- × **App Store**
- × **AWS Marketplace**
- × **Café Press**
- × **Shapeways**

OPEN SOURCE / CREATIVE COMMONS

SHARING

- × **Sometimes we want to share**
 - + Isn't it great doesn't cost us anything to give away digital products?
 - + Isn't it great can build on work of others without necessary cost?
 - + Cooperation on standards create opportunities for everyone, for an industry

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CHALLENGE

- × **Patents cost money**
- × **Business (people making money) will spend money to patent things**
 - + ...and typically incentivized to patent everything they can
- × **Company (individual) could patent something and grant free license**
- × **How does individual, non-profit, etc.**
 - + Create something and protect right to share?
- × **Variety of Open-Source/Public Domain licenses**

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CREATIVE COMMONS

- × **Framework and set of licenses for clearly expressing intent**
- × **Issues**
 - + Attribution
 - + Share-Alike
 - + (Non-)commercial
 - + (No)Derivatives
- × **Apps to choose, logos to show, legal backing to define precisely**
- × **<https://creativecommons.org/share-your-work/licensing-types-examples/>**



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NON-DISCLOSURE AGREEMENT (NDA)

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NDA


- × **Tool for protecting IP**
- × **Legal agreement that you won't disclose someone information shared with you**
 - + Prevent loss of IP
- × **Typical for collaborating companies**
- × **Typical for employers**
- × **In part to make sure sharing with you doesn't count as "disclosure" to preclude patents**
- × **Define scope of disclosure**

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WHO OWNS IP?

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US010261794B2

(12) United States Patent
DeHon

(10) Patent No.: **US 10,261,794 B2**
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Related U.S. Application Data
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(51) Int. Cl. **G06F 02/00 (2018.01)**

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5,201,856 A 4/1993 Daniel et al.
6,298,432 B1 10/2001 Goto (Continued)

FOREIGN PATENT DOCUMENTS
GB 2519608 A 4/2015
WO 2010/028316 A1 3/2010 (Continued)

OTHER PUBLICATIONS
Uda Dharwan, et al., "PUMP: A Programmable Unit for Metadata Processing. In Proceedings of the 3rd International Workshop on Hardware and Architectural Support for Security and Privacy", Jun 2014.
(74) Attorney, Agent, or Firm — Hamilton, Brook, Smith & Reynolds, PC.
(57) **ABSTRACT**
Techniques are described for metadata processing that can be used to encode an arbitrary number of security policies for code running on a processor. Metadata may be added to

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US005742180A

United States Patent [19]
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(73) Assignee: **Massachusetts Institute of Technology, Cambridge, Mass.**

(21) Appl. No.: **386,851**
(22) Filed: **Feb. 10, 1995**
(51) Int. Cl.⁶ **H03K 19/177**
(52) U.S. Cl. **326/40; 326/38**
(58) Field of Search **326/38-40, 46**

(56) **References Cited**
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4,354,228 10/1982 Moore et al. 364/900
4,493,029 1/1985 Thibaut 364/200

Denneau, M.M., "The Yorktown Simulation Engine," *IEEE 19th Design Automation Conference*, pp. 55-59 (1982).
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(List continued on next page.)
Primary Examiner—Edward P. Westin
Assistant Examiner—Jon Santamauro
Attorney, Agent, or Firm—Hamilton, Brook, Smith & Reynolds, PC.

(57) **ABSTRACT**
An integrated dynamically programmable gate array comprises a two dimensional array of programmable gates. These gates can be implemented as look up tables but hardwired gates with programmable interconnections are also possible. Each one of the gates receives plural input logic signals from plural other gates. Consequently, a broad range of logic combinations are possible. The gates further include locally stored multiple contexts dictating different combinatorial logic operations performed by the gates. The contexts increase the logic operations performable by the gate and the fact that the contexts are locally stored enables

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WORK SCENARIOS

- ✘ **Hired/paid by company to invent**
 - + Belongs to company
- ✘ **Invent on side on free time**
 - + ...may depend on employment agreement
 - + ...whether or not subject matter overlaps with company
- ✘ **Consultant**
 - + By default yours, but consulting agreement may define

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UNIVERSITY

- ✘ **Based on grant funds and resources**
 - + Typically goes to university and funding source
 - + Right of first refusal...won't always pursue
- ✘ **Undergraduate**
 - + Invent in class, senior-design → yours
- ✘ **Graduate students paid RA from grant**
 - + Typically funded by grant and go to University
- ✘ **Undergraduate paid research (employee)**
 - + Typically funded by grant and go to University
- ✘ **Graduate students in class, using class resources**
 - + Goes to University

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LAB DUE

- ✘ **Note: Lab due Today (by midnight)**
 - + Last day of classes (not have due during reading period)
 - + **Final office hours now to 8pm**

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BIG IDEAS

- ✘ **We (engineers...particularly in computing space) are knowledge workers, producing IP**
- ✘ **IP carries great value**
 - + That is less and less tied to physical objects
- ✘ **Need to equitably reward and encourage IP creation**
- ✘ **Patents, Copyrights, Licenses ...**
 - + Attempts to provide framework for IP ownership, sharing, monetization
 - + ...probably not the final answer, particularly as technology landscape continues to evolve.

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LEARN MORE

- × **EAS 507 – IP and Business Law for Engineers**
- × **EAS 545 – Engineering Entrepreneurship**
 - + Has sections on IP

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| Topic | CIS | CMPE | EE | SSE |
|------------------|-----------------------|-------------------------------|-----------------------|-----------------------|
| Analog Circuits | | ESE215 | ESE215 | |
| Compress | CIS121 | CIS121 | | |
| Nyquist, Fourier | | | ESE224, ESE325 | ESE224, ESE325 |
| Optimization | CIS320 | (many) | | ESE204 |
| Digital Logic | CIS240 | CIS240, ESE370, ESE532 | | |
| Processor | CIS371 | CIS371 | | |
| OS | CIS380 | CIS380 | | |
| File System | CIS380, CIS121 | CIS380, CIS121 | | |
| IP | | EAS545 | ESE545 | ESE545 |
| Networking | | ESE407 or CIS553 | ESE407 | ESE407 |
| Embedded | | ESE350, CIS441 | ESE350 | ESE350 |
| UI | | | | ESE543 |

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(NOTES FOR PREVIOUS SLIDE)

- × **Bold – required**
- × Not bold – restricted elective
- × Simplified to fit on one slide
 - + (e.g. should show many more analog circuits courses as restricted-electives for EE)

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