Penn Engineering

ESE

Lecture #13 – Intellectual Property

ESE150 Spring 2020

ESE 150 – Digital Audio Basics

1

Preclass

- **Cost to develop and write a book?**
  - 200 days @ $500/day
- **Cost per book (assume $1 to print book)**
  - Total volume 1
  - Total volume 10,000
  - Total volume 1 million
- **Book sells $10**
  - Value added by writer?
  - Copies sold to break even at $2/copy to writer?

2

Economic Terms

- **Production cost – expense to produce**
- **Price – what consume will pay for it**
  - Value to consumer
- **Profit = Price – cost**

3

Observe

- **Creative / Intellectual work produces most of value**
- **At least in volume, physical costs of reproduction is small part of product price**

4

Preclass Continued

- **Cost to photocopy 200 page book at $0.05/page?**
- **Cost to scan book at 10page/minute?**
- **Cost to perform a 10s copy onto flash drive?**
- **Cost of portion of flash drive used**
  - $8 for 16GB drive, 0.5MB file

5

Observe

- **With digital representation**
  - Cost of “physical” reproduction trends to 0

6

Past

- **Much of value in physical construction of objects**
  - Bridge, house, car, screwdriver
- **Expensive to reproduce / copy**
- **Reproductions imperfect**
  - 5th generation analog recording
  - 4th generation photocopy of text
- **Inherent barrier to making copies**
  - Value to buying original

Digital Representation

- **Can represent perfectly in bits**
  - Including sound, words
- **Can make perfect copies**
- **Bits are cheap…and getting cheaper**
  - Copying "free"
- **Intellectual value disconnected from physical reproduction**

What else has this property?

Digital Intellectual Property	Physical IP Renderer
Novel	eReader
Song (MP3)	MP3 Player
JPEG Photo	
	Video Player
Video Game	
	Arduino or Personal Computer
Verilog digital circuit	
	Web Server
STL (3D CAD drawing)	
DNA Sequence	DNA Printer

Intellectual Property

- **Intangible creations of human intellect**
- **Have value**
- **Don't necessarily have physical embodiment on their own**

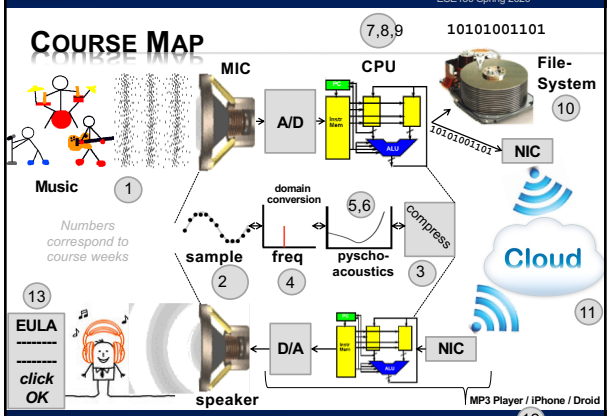
Intellectual Property Creators

- **As Engineers**
  - Program, develop algorithms, design circuits
- **Almost everything we create will have this property**
  - Value added is intellectual
  - Can be represented digitally in bits
  - Can (increasingly) be copied/reproduced cheaply
- **Easy to have impact**
  - Our solutions can reach millions, billions
  - Decreasing physical barriers to propagation of solutions
- **Challenge to protect and reward IP creators**

Outline

- **Setup Need / Opportunity – What is IP**
- **Where are we**
- **Rationale for IP Protection – Why Protect**
- **How protect?**
  - Patents
  - Copyrights
  - Open Source
  - NDA
  - Licensing

COURSE MAP



RATIONALE

PRICING CHALLENGE

- **When cost of copying → 0**
  - Inventor/author must recover development cost
    - Price must include develop cost + copy cost
  - Copier does not have development cost
    - Price = copy cost + epsilon
    - Competition of copiers will drive epsilon down near 0
  - Inventor/author not compensated for development
    - Remove incentive/reward for development
- **Demand: developers need way to exclude others from copying to incentivize creation**

ARROW'S INFORMATION PARADOX

- **Customer not know how to value information until see information (see details of product)**
  - Enough information to decide to buy
  - Enough information to decide what will pay for it
- **Once show customer information, sufficient detail, they have enough information to reproduce**
  - Could walk away and produce their own without paying for it
- **Disclosure of what effectively transfers technology**
- **Demand: protection for developer**
- Arrow, Kenneth J. Economic Welfare and the Allocation of Resources for Invention, in *The Rate and Direction of Inventive Activity*, 609 (Nat'l Bureau of Econ. Research ed. 1962).

BALANCE INDIVIDUAL AND SOCIETAL GOOD

- **Individual should benefit form their own effort**
- **Society advances with the accumulation of knowledge**

BEFORE COPYING WAS AN ISSUE

- **Concern that new developments/ideas would be lost when inventor die**
  - Techniques could remain secret for decades!
- **Incentive to make inventions known**
  - Advance the general welfare

US Constitution

- **Article 1, Section 8, Clause 8:**
  - To promote the Progress of Science and useful Arts, by securing for limited Times to Authors and Inventors the exclusive Right to their respective Writings and Discoveries

Mechanisms (To support)

- **Patents**
  - Cover inventions
  - E.g., Flying Machine (US 821,393), ENIAC (US 3,120,606),
- **Copyrights**
  - Creative expression
  - E.g., novel, song, movie

Mechanisms for Protection

- **Messy and imperfect**
- **Haven't kept up with technology**
- **Likely need (and will need) innovation and refinement**

Interlude: NIL
Nikolai Ivanovich Lobachevsky

https://www.youtube.com/watch?v=gXIfXirQF3A

Patents

Patent

- **Inventions**
- **Non-obvious to one "ordinary skill in art"**
- **Reduced to practice**
- **Cannot patent**
  - Abstract ideas
  - Laws of nature
- **US: First to file**
  - (prior to 2013 was first to invent)
- **Exclusive rights 20 years from filing**

WHAT MIGHT BE TRICKY / NON-SATISFYING?

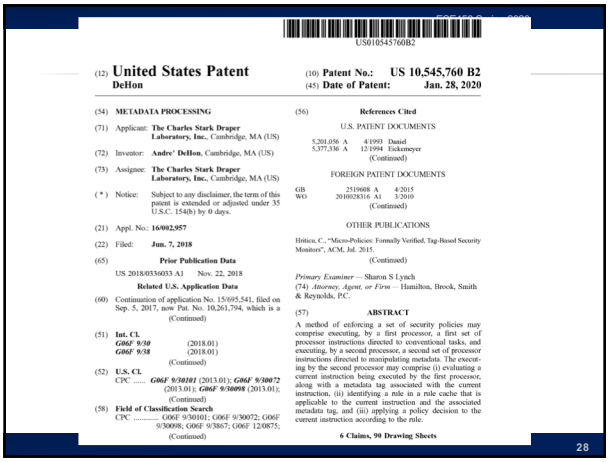
- First to file? (even invent?)
- 20 year term?

PATENT

- **Identification of problem is part of invention**
- **Claims**
  - Define the invention
  - Technical coverage
- **Requires disclosure**
  - If really believe no one else will figure it out…or can copy it, maybe better to keep as a *trade secret*
- **License to litigate**
  - Recover damages is through litigation
  - Establish violation
  - Validity of many patents overturned in litigation

PATENT PROCESS

- **US have one year from first-public disclosure to file**
  - Many places – public disclosure prevent patent
  - https://www.uspto.gov/web/offices/pac/mpep/s2153.html
- **May file provisional patent to get filing date**
- **File patent with claims**
- **Reviewed by examiner**
- **Examiner reports on what may be allowable**
  - As-is
  - With tighter qualifications
  - Not-at-all
  - On a per-claim basis
- **Typically requires several iterations**
- **Often year(s) before patent issues**
- **Filing costs thousands of dollars**
  - With lawyer/legal fees tens to hundreds of thousands



US010545760B2

(12) **United States Patent**
DeHon

(10) **Patent No.: US 10,545,760 B2**
(45) **Date of Patent: Jan. 28, 2020**

(54) **METADATA PROCESSING**

(71) Applicant: **The Charles Stark Draper Laboratory, Inc.**, Cambridge, MA (US)

(72) Inventor: **Andre' DeHon**, Cambridge, MA (US)

(73) Assignee: **The Charles Stark Draper Laboratory, Inc.**, Cambridge, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/002,957**

(22) Filed: **Jun. 7, 2018**

(65) **Prior Publication Data**

US 2018/0336033 A1 Nov. 22, 2018

Related U.S. Application Data

(60) Continuation of application No. 15/695,541, filed on Sep. 5, 2017, now Pat. No. 10,261,794, which is a (Continued)

(51) **Int. Cl.**
G06F 9/30 (2018.01)
G06F 9/38 (2018.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G06F 9/30101*** (2013.01); ***G06F 9/30072*** (2013.01); ***G06F 9/30098*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC G06F 9/30101; G06F 9/30072; G06F 9/30098; G06F 9/3867; G06F 12/0875;
(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,201,056 A 4/1993 Daniel
5,377,336 A 12/1994 Eickemeyer
(Continued)

FOREIGN PATENT DOCUMENTS

GB 2519608 A 4/2015
WO 2010028316 A1 3/2010
(Continued)

OTHER PUBLICATIONS

Hritcu, C., "Micro-Policies: Formally Verified, Tag-Based Security Monitors", ACM, Jul. 2015.
(Continued)

Primary Examiner — Sharon S Lynch
(74) *Attorney, Agent, or Firm* — Hamilton, Brook, Smith & Reynolds, P.C.

(57) **ABSTRACT**

A method of enforcing a set of security policies may comprise executing, by a first processor, a first set of processor instructions directed to conventional tasks, and executing, by a second processor, a second set of processor instructions directed to manipulating metadata. The executing by the second processor may comprise (i) evaluating a current instruction being executed by the first processor, along with a metadata tag associated with the current instruction, (ii) identifying a rule in a rule cache that is applicable to the current instruction and the associated metadata tag, and (iii) applying a policy decision to the current instruction according to the rule.

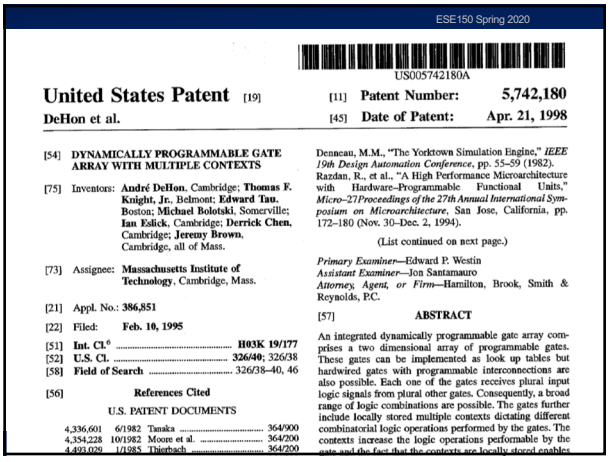
6 Claims, 90 Drawing Sheets

What is claimed is:

1. A method of obtaining control flow information for an application, comprising:

executing a loader that loads the application for execution by a processor, wherein executing the loader comprises executing a first code portion of the loader that includes one or more instructions configured to trigger metadata processing of a first set of one or more rules in a metadata processing domain, the metadata processing of the first set of one or more rules includes collecting and storing the control flow information for the application as application metadata accessible to the metadata processing domain and inaccessible to a code execution domain, wherein collecting and storing the control flow information further comprises tagging, by the metadata processing domain, a first target location with first metadata identifying a set of one or more allowable source locations that are allowed to transfer control to the first target location and storing the first metadata as a portion of the control flow information, wherein each allowable source location of the set is further tagged with a corresponding source metadata tag;

executing instructions of the application in the code execution domain, wherein executing the instructions of the application triggers metadata processing of a second set of rules that use at least a portion of the control flow information including the first metadata to determine whether to allow a transfer of control from a first source location to the first target location based on whether the first source location is included in the set of one or more allowable source locations, wherein the second set of rules corresponds to a control flow policy.



US005742180A

United States Patent [19]
DeHon et al.

[11] **Patent Number: 5,742,180**
[45] **Date of Patent: Apr. 21, 1998**

[54] **DYNAMICALLY PROGRAMMABLE GATE ARRAY WITH MULTIPLE CONTEXTS**

[75] Inventors: **André DeHon**, Cambridge; **Thomas F. Knight, Jr.**, Belmont; **Edward Tau**, Boston; **Michael Bolotski**, Somerville; **Ian Eslick**, Cambridge; **Derrick Chen**, Cambridge; **Jeremy Brown**, Cambridge, all of Mass.

[73] Assignee: **Massachusetts Institute of Technology**, Cambridge, Mass.

[21] Appl. No.: **386,851**

[22] Filed: **Feb. 10, 1995**

[51] **Int. Cl.**[6] **H03K 19/177**
[52] **U.S. Cl.** **326/40**; 326/38
[58] **Field of Search** 326/38–40, 46

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,336,601 6/1982 Tanaka 364/900
4,354,228 10/1982 Moore et al. 364/200
4,493,026 1/1985 Dierbach 364/200

Denneau, M.M., "The Yorktown Simulation Engine," *IEEE 19th Design Automation Conference*, pp. 55–59 (1982).
Razdan, R., et al., "A High Performance Microarchitecture with Hardware–Programmable Functional Units," *Micro–27Proceedings of the 27th Annual International Symposium on Microarchitecture*, San Jose, California, pp. 172–180 (Nov. 30–Dec. 2, 1994).
(List continued on next page.)

Primary Examiner—Edward P. Westin
Assistant Examiner—Jon Santamauro
Attorney, Agent, or Firm—Hamilton, Brook, Smith & Reynolds, P.C.

[57] **ABSTRACT**

An integrated dynamically programmable gate array comprises a two dimensional array of programmable gates. These gates can be implemented as look up tables but hardwired gates with programmable interconnections are also possible. Each one of the gates receives plural input logic signals from plural other gates. Consequently, a broad range of logic combinations are possible. The gates further include locally stored multiple contexts dictating different combinatorial logic operations performed by the gates. The contexts increase the logic operations performable by the

CLAIMS

We claim:

1. An integrated dynamically programmable logic array, comprising:

at least a two dimensional array of programmable logic elements, each one of the logic elements receiving plural input logic signals from plural other logic elements and including locally stored multiple contexts dictating different combinatorial logic operations performed by the logic elements; and

a context signal source that provides a context signal, indicating an active one of the contexts, commonly to the programmable logic elements of the array; and

wherein the contexts for each one of the logic elements are individually accessible so that a new context can be loaded into the logic elements while another context is controlling logic operations of the logic elements.

2. A programmable logic array as described in claim 1, wherein the context signal source provides the context signal up to every cycle of the programmable logic array.

3. A programmable logic array as described in claim 1, wherein the context signal source generates plural context signals that dictate contexts for regions of the array of the logic elements.

XILINX FPGA US 4,870,302

[57] **ABSTRACT**

A configurable logic array comprises a plurality of configurable logic elements variably interconnected in response to control signals to perform a selected logic function. Each configurable logic element in the array is in itself capable of performing any one of a plurality of logic functions depending upon the control information placed in the configurable logic element. Each configurable logic element can have its function varied even after it is installed in a system by changing the control information placed in that element. Structure is provided for storing control information and providing access to the stored control information to allow each configurable logic element to be properly configured prior to the initiation of operation of the system of which the array is a part. Novel interconnection structures are provided to facilitate the configuring of each logic element.

I claim:

1. An interconnect structure for programmably interconnecting lines within an integrated circuit comprising:

at least three sets of interconnect line including a first set, a second set, and a third set;

programmable means, not including said sets of interconnect lines, for connecting at least one of said lines in said first set to at least one of said lines in said second set, for connecting at least one of said lines in said first set to at least one of said lines in said third set, and for connecting at least one of said lines in said second set to at least one of said lines in said third set.

2. An array of interconnect structures, each said interconnect structure as in claim 1, and each interconnect structure in said array having its own selected number of interconnect lines and its own programmable means for connecting interconnect lines in its own first, second and third sets.

https://patents.google.com/patent/US4870302A/en?oq=us+4870302

ENIAC US 3,120,606

- 1. MEANS FOR PRODUCING ELECTRIC PULSES IN SEQUENCE, ELECTRONIC MEANS FOR ALTERNATELY TRANSMITTING CERTAIN ONES OF SAID PULSES AS RECURRENT DIFFERENTIATED GROUPS, ELECTRONIC MEANS FOR SELECTING PARTICULAR PULSES FROM ONE OF SAID DIFFERENTIATED GROUPS TO REPRESENT QUANTITATIVE VALUES, ELECTRONIC MEANS FOR SELECTING PARTICULAR PULSES FROM ANOTHER OF SAID DIFFERENTIATED GROUPS TO REPRESENT CERTAIN QUALITATIVE VALUES, READING MEANS RESPONSIVE TO PULSES REPRESENTING BOTH THE QUALITATIVE AND QUANTITATIVE VALUES FOR READING DATA TO BE PROCESSED UPON COMMAND OF AT LEAST ONE OF SAID QUALITATIVE PULSES, STORING THE DATA THUS READ, AND MAKING THE DATA AVAILABLE IN THE FORM OF DATA PULSES IN RESPONSE TO AT LEAST ONE OTHER OF SAID QUALITATIVE PULSES, AND ELECTRONIC MEANS FOR RECEIVING SAID DATA PULSES AND RESPONSIVE THERETO FOR PERFORMING ELECTRICAL SWITCHING OPERATIONS OF A NATURE DETERMINED BY SELECTED ONES OF SAID QUALITATIVE VALUES AND OF A DEGREE DETERMINED BY SELECTED ONES OF SAID QUANTITATIVE VALUES.

https://www.computerhistory.org/revolution/birth-of-the-computer/4/99/387

WHAT'S PATENTABLE

- **Not law's of nature**
- **Not abstract ideas**
- **Cannot patent pi (π)**
- **Software?**
  - Originally not
  - With reference to machine, can often manage
- **Genetic sequences?...**
- **…evolving…**

COPYRIGHT

COPYRIGHT

- **Cover particular, original expression**
  - Including software
- **Technically don't need to register**
  - But should…
  - Must register before sue for infringement
  - $35
  - No review, just registration
- **Life of author + 70 years**
- **Work for hire: 95 years from publication**

TRADITIONALLY: TRANSFER COPYRIGHT …

- **Publish in ACM, IEEE journal**
  - Transfer copyright to them, they license you back rights for derived work and post on person web site.

RECENT: LICENSE TO ACM, IEEE

- **Author retain copyright, license to publisher**

FPGA '17, February 22 - 24, 2017, Monterey, CA, USA

ISBN 978-1-4503-4354-1/17/02…$15.00

DOI: http://dx.doi.org/10.1145/3020078.3026124

LICENSING

South Park: Human CenitPad

https://southpark.cc.com/clips/382781/business-casual-g-men

LICENSE

- **Where have you seen licenses?**

LICENSES

- **How get right to use**
  - Something patented, copyrighted by someone else
- **Between companies**
  - Get IP need to build a product
- **To consumers**
  - Technically, most software is licensed, not sold
  - …shrink-wrap licensing agreements…
- **Define terms of use**
  - What you are paying for (one copy, many, resale…)
  - What uses (dis)allowed

DIRECT LICENSING/SALES

PAST

- **Selling a product require huge infrastructure and up-front capital costs**
  - Manufacture (physical things)
  - Marketing
  - Distribution
  - Sales
- **Demand large business to support infrastructure**
- **Not easy for individual**

TODAY (EMERGING)

- **Eliminate infrastructure needs with ubiquitous networking, IP products, service businesses**
  - Manufacture (physical things) → not issue for IP
    - …or licensed manufacturing
  - Marketing → still need to get the word out
    - …can use web at low cost
  - Distribution → not an issue for IP
    - …leverage common carriers
  - Sales
    - Handle online, eBusiness support
- **Becomes possible for individuals/small businesses to sell IP directly to consumers**

DIRECT IP BUSINESSES TODAY

- **Examples?**

DIRECT IP BUSINESSES TODAY

- **Kindle Direct Publishing**
- **App Store / Google Play**
- **AWS Marketplace**
- **Café Press**
- **Shapeways**

OPEN SOURCE / CREATIVE COMMONS

SHARING

- **Sometimes we want to share**
  - Isn't it great doesn't cost us anything to give away digital products?
  - Isn't it great can build on work of others without necessary cost?
  - Cooperation on standards create opportunities for everyone, for an industry

Challenge

- **Patents cost money**
- **Business (people making money) will spend money to patent things**
  - …and typically incentivized to patent everything they can
- **Company (individual) could patent something and grant free license**
- **How does individual, non-profit, etc.**
  - Create something and protect right to share?
- **Variety of Open-Source/Public Domain licenses**

Creative Commons

- **Framework and set of licenses for clearly expressing intent**
- **Issues**
  - Attribution
  - Share-Alike
  - (Non-)commercial
  - (No)Derivatives
- **Apps to choose, logos to show, legal backing to define precisely**
- **https://creativecommons.org/share-your-work/licensing-types-examples/**

Non-Disclosure Agreement (NDA)

NDA

- **Tool for protecting IP**
- **Legal agreement that you won't disclose someone information shared with you**
  - Prevent loss of IP
- **Typical for collaborating companies**
- **Typical for employers**
- **In part to make sure sharing with you doesn't count as "disclosure" to preclude patents**
- **Define scope of disclosure**

Administrative Interlude: Final

Final

- **Final Office Hours: (see piazza)**
  - Saturday 5/9
  - Sunday 5/10
- **Final: Monday (5/11) Online**
  - Regulations posted
  - 15% of grade
  - Comprehensive (intent…does tend to weight 2nd half)
  - Last few years final and answers linked to Spring 2018 syllabus
    - Probably mix ideas from first and second half
  - Poll for when you plan to take
    - So someone might be awake to answer questions…

FINAL TOPICS

Pre Midterm

- Data representation in bits
- Sounds waves
- Sampling
- Quantization
- Nyquist
- Lossy/lossless compression
- Common case
- Frequency domain
- Psychoacoustics
- Perceptual coding

Post midterm

- Combinational Logic
- Finite-State Machines
- Stored-Program Processors
- Processing Requirements
- Process Virtualization
- Networking
- User Interface
- Intellectual Property

WHO OWNS IP?

US010261794B2

(12) **United States Patent**
DeHon

(10) **Patent No.: US 10,261,794 B2**
(45) **Date of Patent: Apr. 16, 2019**

(54) **TECHNIQUES FOR METADATA PROCESSING**

(71) Applicant: **The Charles Stark Draper Laboratory, Inc.**, Cambridge, MA (US)

(72) Inventor: **Andre' DeHon**, Philadelphia, PA (US)

(73) Assignee: **The Charles Stark Draper Laboratory, Inc.**, Cambridge, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/695,541**

(22) Filed: **Sep. 5, 2017**

(65) **Prior Publication Data**

US 2018/0011708 A1 Jan. 11, 2018

Related U.S. Application Data

(60) Division of application No. 15/426,098, filed on Feb. 7, 2017, now Pat. No. 9,785,440, which is a (Continued)

(51) **Int. Cl.**

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,201,056 A 4/1993 Daniel et al.
6,298,432 B1 10/2001 Goto
(Continued)

FOREIGN PATENT DOCUMENTS

GB 2519608 A 4/2015
WO 2010028316 A1 3/2010
(Continued)

OTHER PUBLICATIONS

Udit Dhawan, et al., "PUMP: A Programmable Unit for Metadata Processing. In Proceedings of the 3rd International Workshop on Hardware and Architectural Support for Security and Privacy", Jun. 2014.
(Continued)

Primary Examiner — Sharon S Lynch
(74) *Attorney, Agent, or Firm* — Hamilton, Brook, Smith & Reynolds, P.C.

(57) **ABSTRACT**

Techniques are described for metadata processing that can be used to encode an arbitrary number of security policies for code running on a processor. Metadata may be added to

US005742180A

United States Patent [19]
DeHon et al.

[11] **Patent Number: 5,742,180**
[45] **Date of Patent: Apr. 21, 1998**

[54] **DYNAMICALLY PROGRAMMABLE GATE ARRAY WITH MULTIPLE CONTEXTS**

[75] Inventors: **André DeHon**, Cambridge; **Thomas F. Knight, Jr.**, Belmont; **Edward Tau**, Boston; **Michael Bolotski**, Somerville; **Ian Eslick**, Cambridge; **Derrick Chen**, Cambridge; **Jeremy Brown**, Cambridge, all of Mass.

[73] Assignee: **Massachusetts Institute of Technology**, Cambridge, Mass.

[21] Appl. No.: **386,851**

[22] Filed: **Feb. 10, 1995**

[51] **Int. Cl.**[6] **H03K 19/177**
[52] **U.S. Cl.** **326/40**; 326/38
[58] **Field of Search** 326/38–40, 46

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,336,601 6/1982 Tanaka 364/900
4,354,228 10/1982 Moore et al. 364/200
4,493,029 1/1985 Thierbach 364/200

Denneau, M.M., "The Yorktown Simulation Engine," *IEEE 19th Design Automation Conference*, pp. 55–59 (1982).
Razdan, R., et al., "A High Performance Microarchitecture with Hardware–Programmable Functional Units," *Micro–27Proceedings of the 27th Annual International Symposium on Microarchitecture*, San Jose, California, pp. 172–180 (Nov. 30–Dec. 2, 1994).

(List continued on next page.)

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[57] **ABSTRACT**

An integrated dynamically programmable gate array comprises a two dimensional array of programmable gates. These gates can be implemented as look up tables but hardwired gates with programmable interconnections are also possible. Each one of the gates receives plural input logic signals from plural other gates. Consequently, a broad range of logic combinations are possible. The gates further include locally stored multiple contexts dictating different combinatorial logic operations performed by the gates. The contexts increase the logic operations performable by the gate and the fact that the contexts are locally stored enables

WORK SCENARIOS

- **Hired/paid by company to invent**
  - Belongs to company
- **Invent on side on free time**
  - …may depend on employment agreement
  - …whether or not subject matter overlaps with company
- **Consultant**
  - By default yours, but consulting agreement may define

UNIVERSITY

- **Based on grant funds and resources**
  - Typically goes to university and funding source
  - Right of first refusal…won't always pursue
- **Undergraduate**
  - Invent in class, senior-design → yours
- **Graduate students paid RA from grant**
  - Typically funded by grant and go to University
- **Undergraduate paid research (employee)**
  - Typically funded by grant and go to University
- **Graduate students in class, using class resources**
  - Goes to University

Lab Due

- **Note: Lab due Today (by midnight)**
  - Last day of classes (not have due during reading period)
  - ***Final office hours now to 8pm***
- **Remember Lecture and Lab feedback form**

Big Ideas

- **We (engineers…particularly in computing space) are knowledge workers, producing IP**
- **IP carries great value**
  - That is less and less tied to physical objects
- **Need to equitably reward and encourage IP creation**
- **Patents, Copyrights, Licenses …**
  - Attempts to provide framework for IP ownership, sharing, monetization
  - …probably not the final answer, particularly as technology landscape continues to evolve.

Learn More

- **EAS 507 – IP and Business Law for Engineers**
- **EAS 545 – Engineering Entrepreneurship**
  - Has sections on IP

Topic	CIS	CMPE	EE	SSE
Analog Circuits		**ESE215**	**ESE215**	
Compress	**CIS121**	**CIS121**		
Nyquist, Fourier			**ESE224**, ESE325	**ESE224**, ESE325
Optimization	**CIS320**	(many)		**ESE204**
Digital Logic	**CIS240**	**CIS240, ESE370,** ESE532		
Processor	**CIS371**	**CIS371**		
OS	**CIS380**	**CIS380**		
File System	**CIS380, CIS121**	**CIS380, CIS121**		
IP		EAS545	ESE545	ESE545
Networking		**ESE407** or **CIS553**	ESE407	ESE407
Embedded		**ESE350 CIS441**	ESE350	ESE350
UI				ESE543

(Notes for previous slide)

- **Bold – required**
- Not bold – restricted elective
- Simplified to fit on one slide
  - (e.g. should show many more analog circuits courses as restricted-electives for EE)