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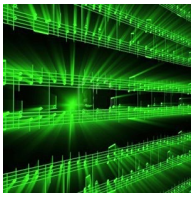

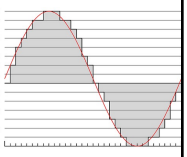

Lecture #13 – Combinational Logic

ESE 150 – Digital Audio Basics

ESE150 Spring 2022

Based on slides © 2009--2022 DeHon

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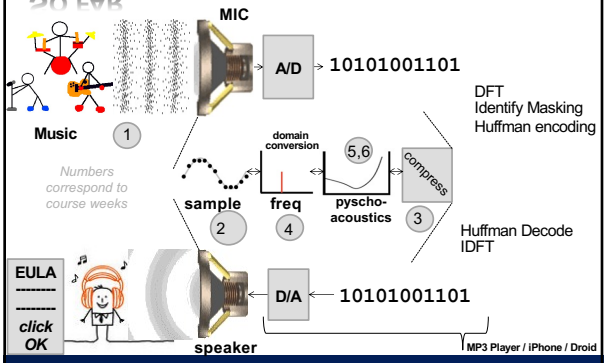
So far



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How Process

- **How do we build a machine to perform these operations?**
  - From Digital Samples → compressed digital data → Digital Samples
- **Down to bottom**
  - If we can build **one** kind of primitive element (maybe 2),
    - …and connect together large collections of them
  - can build a machine to perform *any* digital computation

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Lecture Topics

- Setup
- **Where are we?**
- **Combinational Logic**
- **Arithmetic (Part 2)**
- **Accumulator (Part 3)**
- **Next Lab**

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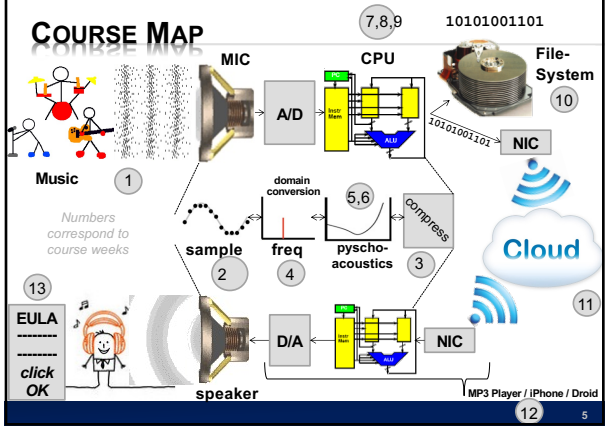
Course Map



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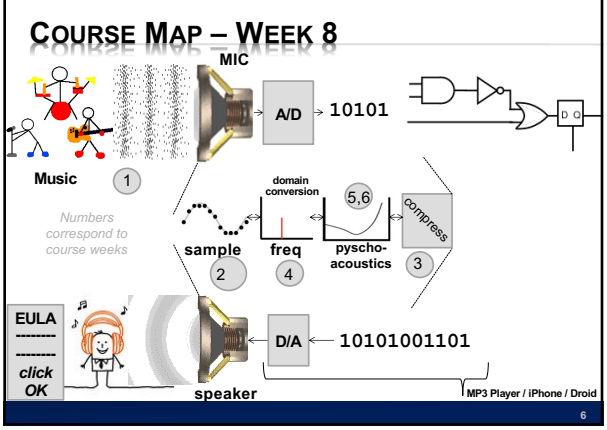
Course Map – Week 8



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COMBINATIONAL LOGIC

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GATE

- **Primitive binary function**
  - Computes a binary output from a small number of binary inputs
- **Can specify function with a Truth Table**
  - Defines the output for each input combination

Input 0	Input 1	Output
0	0	
0	1	
1	0	
1	1	

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AND GATE

- **AND**
  - Output is 1 (true) when all inputs are 1 (true)

Input 0	Input 1	AND
0	0	0
0	1	0
1	0	0
1	1	1

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NOT GATE

- **Not**
  - Output is opposite of input

input	NOT
0	1
1	0

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OR GATE

- **OR**
  - Output is 1 (true) when any input is 1 (true)
  - (fillin truth table for OR)

Input 0	Input 1	OR
0	0	
0	1	
1	0	
1	1	

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CLAIM

- **Can compute any Boolean Function from AND, OR, NOT**
  - (actually from NAND)

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Model: Combinational Logic

- **Compute some "function"**
  - $f(i_0,i_1,\ldots i_n) \rightarrow o_0,o_1,\ldots o_m$
- **Each unique input vector**
  - implies a particular, deterministic, output vector

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Big AND

- **AND**
  - Output is 1 (true) when all inputs are 1 (true)
- **How build n-input AND from AND2 gates?**

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Big OR

- **OR**
  - Output is 1 (true) when any input is 1 (true)
- **How build n-input OR from OR2?**

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Input Case

- **How can we create an expression that is true for a specific input case?**
  - E.g. have a function of 4 inputs: a, b, c, d
    - Want identify case a=0, b=1, c=1, d=0
- **How many potential values for a, b, c, d?**
  - Rows in our truth table
- **How create an expression (in and and not) that is true for the a=0, b=1, c=1, d=0 case?**

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Single Output Digital Function

- **Given have logic to identify each input case where output is a 1:**
- **How implement entire function?**

a	b	c	F(a,b,c)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

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Multiple Output Function

- **What do you do if your Digital Function needs multiple output bits?**

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Combinational Logic as Gates

- **Start with truth table**
- **Single output {0, 1}**
  - Use inverters to produce complements of inputs
  - For each input case
    - If output is a 1
      - Develop an AND to detect that case
        - Decompose AND into gates
  - OR together the output of all such AND functions
    - Decompose OR into gates
- **Multiple outputs**
  - Repeat for each output

This solution won't typically be the smallest or fastest…

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Conclude

- **Can implement any combinational logic function out of a collection of**
  - OR2, AND2, NOT gates

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Part 2

Arithmetic

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Arithmetic

- **Addition is also a digital (combinational) logic function**
  - Maps set of inputs (a3 a2 a1 a0 b3 b2 b1 b0)
  - To an output bit vector (c4 c3 c2 c1 c0)
- **…as is subtraction, multiplication, division, square root….**

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Positional Binary Numbers

- Binary number: $a_{n-1}\ a_{n-2}\ \ldots a_0$
  - *Eg.*, 01101
  - n=5 a_4=0, a_3=1, a_2=1, a_1=0, a_0=1
- $value = \sum_{i=0}^{i \le n} a_i \times 2^i$
- What value 01101?

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Addition

- **Add two binary digits, what do we get?**
  - 0 + 0 =
  - 0 + 1 =
  - 1 + 0 =
  - 1 + 1 =
- **Conclude:** May get two-bit result

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ADDITION

- **Add three binary digits, what's largest binary result?**
  - 1 + 1 + 1 =
- **Conclude:** Also get two-bit result adding 3 bits

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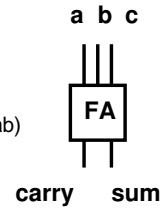
FULL ADDER

- **Adds 3 inputs to produce 2b output**
  - Binary inputs: a, b, c
  - Binary outputs: carry, sum
  - Two bit result:
    - carry*2 +sum = a+b+c
  - It's just another gate we can define
  - Can produce truth table and logic (Lab)



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EXAMPLE: BIT-LEVEL ADDITION

- **Addition** **S = A + B**
- $s_{n-1}\ s_{n-2}\ \ldots s_0 = a_{n-1}\ a_{n-2}\ \ldots a_0 + b_{n-1}\ b_{n-2}\ \ldots b_0$
  - Base 2 example
  - Work together

C	1	1	1	1	1	1	0	0	0
A	0	1	1	1	0	1	1	1	0
B	0	0	1	1	1	0	1	0	0
S	1	0	1	1	0	0	0	1	0

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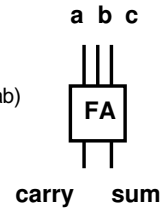
FULL ADDER

- **Adds 3 inputs to produce 2b output**
  - Binary inputs: a, b, c
  - Binary outputs: carry, sum
  - Two bit result:
    - carry*2 +sum = a+b+c
  - Can produce truth table and logic (Lab)
- **Natural primitive for bit-level addition with carry**



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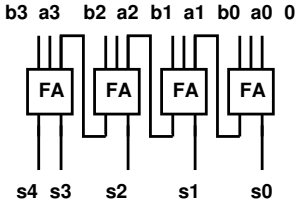
N-BIT ADDER

- **Given Full Adders**
  - Can build N-bit adder by connecting N full adders



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Part 3

ACCUMULATOR

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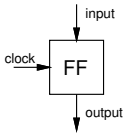
REGISTER

- **Clock**
  - Defines the rate of the computation
  - Typically a square wave
  - Rising clock edge defines beginning of new cycle
- **State Element – Flip-Flop (FF) or Register**
  - Returns the value it was given on previous cycle = before the last rising clock edge
- **More Details next time**



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ACCUMULATOR

- **Sum a sequence of values**
  - **a=0**
  - **while (true)**
    - a=a+getInput();

$$a = \sum_{i=0} input[i]$$

Input[i]	a
	0
1	
	1
3	
	4
1	
	5

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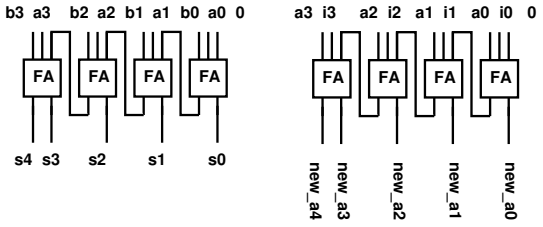
ACCUMULATOR

- **Start with an Adder**



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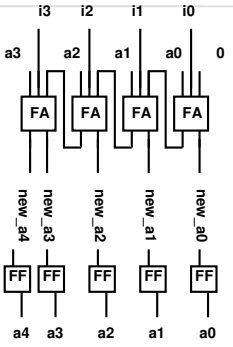
ACCUMULATOR

- **Store running sum as state in registers**
- **Sum up new values provided on successive cycles**

Input[i]	a
	0
1	
	1
3	
	4
1	
	5



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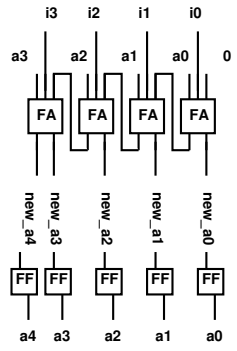
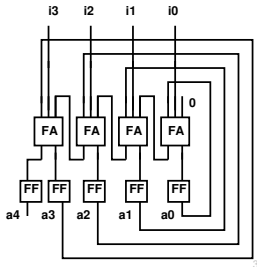
ACCUMULATOR



- Wrap register outputs back to inputs



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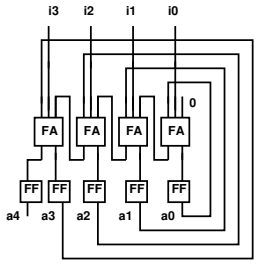
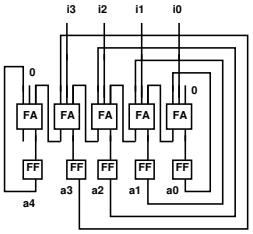
ACCUMULATOR



- Maybe extend accumulator bits to hold larger sum



- Maybe more…

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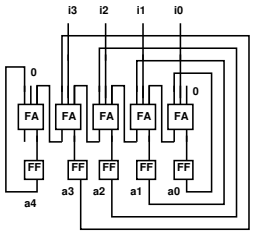
ACCUMULATOR

Input[i]	a
	0
15	
	15
15	
	30
15	
	45
15	
	60
15	
	75

- Maybe extend accumulator bits to hold larger sum



- Why want more?

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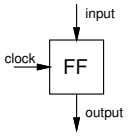
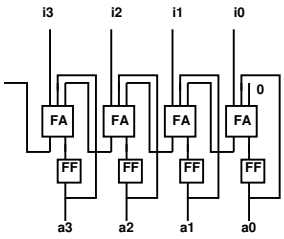
ACCUMULATOR

- **What happens:**
  - Start with a3:a0 at 0
  - CLK low
  - I3:i0=2 (0010)
  - FF inputs?





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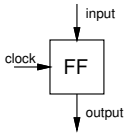
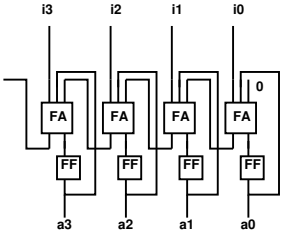
ACCUMULATOR

- **What happens:**
  - Start with a3:a0 at 0
  - CLK low
  - I3:i0=2 (0010)
  - FF inputs?
  - CLK goes high: a3:a0?





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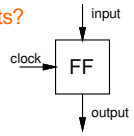
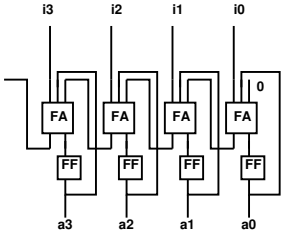
ACCUMULATOR

- **What happens:**
  - Start with a3:a0 at 0
  - CLK low
  - I3:i0=2 (0010)
  - CLK goes high: a3:a0?
  - I3:0=3 (0011)
  - FF inputs?





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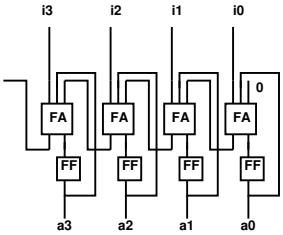
ACCUMULATOR

- **What happens:**
  - Start with a3:a0 at 0
  - CLK low
  - I3:i0=2 (0010)
  - CLK goes high: a3:a0?
  - I3:0=3 (0011)
  - FF inputs?
  - CLK goes high: a3:a0?



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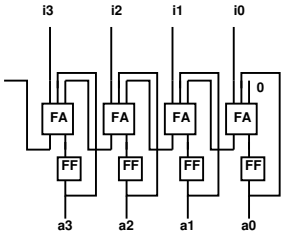
ACCUMULATOR

- **a=0**
- **while (true)**
  - a=a+getInput();

$$a = \sum_{i=0} input[i]$$



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Next Lab (after Spring Break)

- **Lab 7 posted on web**
- **Program an FPGA in Verilog**
  - Build an adder
  - Build an accumulator

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Big Ideas

- **Can implement any combinational digital logic function from (and, or, not) gates**
- **Can store previous values**
  - Flip-flops or registers
- **Enough to perform math we need for audio processing (…and much more…)**

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Learn More

- **CIS240 – do a bit more logic**
- **ESE370 – how to implement gates, latches, and memories from transistors**
- **ESE532 – how to build large-scale computations from logic**

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Reminder

- **Feedback including lab**
- **Spring Break next week**
- **Lab today**
- **Formal Lab Report Due Monday after break**
  - Office hours Thursday and Friday this week
  - Office hours Sunday 3/13 (after Spring Break)

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