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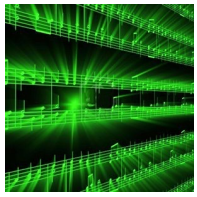

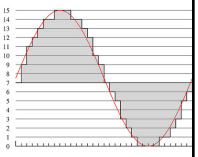

Lecture #14 – Sequential Logic, FPGAs

ESE 150 – Digital Audio Basics

ESE150 Spring 2022

Based on slides © 2009--2022 DeHon

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Lecture Topics

- Setup
- **Where are we?**
- **Part 1:**
  - Review: Combinational Logic
  - Registers
- **Part 2:**
  - FPGAs
- **Part 3:**
  - Finite-State Machines (FSM)

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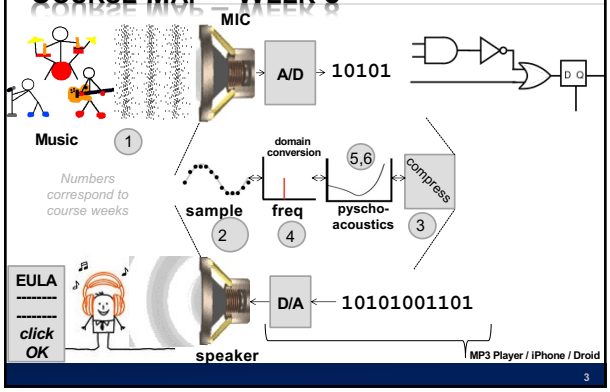
Course Map – Week 8



3

Combinational Logic

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Gate

- **Primitive binary function**
  - Computes a binary output from a small number of binary inputs
- **Can specify function with a Truth Table**
  - Defines the output for each input combination

Input 0	Input 1	Output
0	0	
0	1	
1	0	
1	1	

5

Conclude

- **Can implement any combinational logic function out of a collection of**
  - OR2, AND2, NOT gates

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ARITHMETIC

- **Addition is also a digital logic function**
  - Maps set of inputs (a3 a2 a1 a0 b3 b2 b1 b0)
  - To an output bit vector (c4 c3 c2 c1 c0)
- **…as is subtraction, multiplication, division, square root….**

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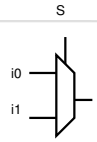
MULTIPLEXER GATE



- **MUX**
  - When S=0, output=i0
  - When S=1, output=i1

S	i0	i1	Mux2(S,i0,i1)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Truth Table?

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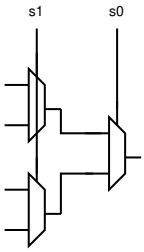
PRECLASS 3

- **How build 4-input mux from 2-input muxes?**



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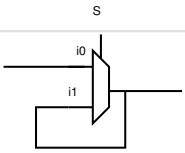
REGISTERS AND CLOCKING

10

MUX WITH FEEDBACK



- **What happens when S=0?**
- **What happens when S=1?**

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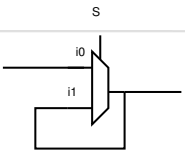
MUX WITH FEEDBACK



- **Assuming i0 doesn't change what happens when S goes from 0 to 1?**

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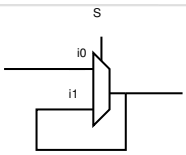
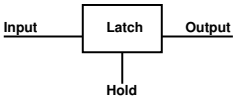
LATCH

- **Element that can hold a previous value of an input**





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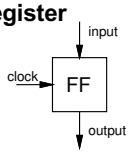
REGISTER

- **Clock**

  - Defines the rate of the computation
  - Typically a square wave
  - Rising clock edge defines beginning of new cycle

- **State Element – Flip-Flop (FF) or Register**
  - Returns the value it was given on previous cycle = before the last rising clock edge



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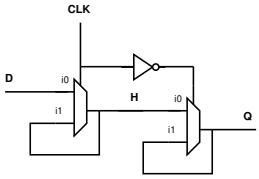
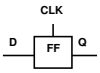
FLIP-FLOP (FF)

- **Use a pair of latches to create a flip-flop**
  - Also call register





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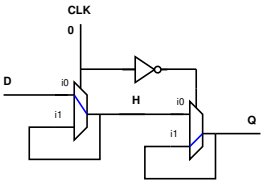
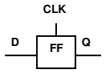
FLIP-FLOP (FF)

- **Use a pair to create a flip-flop**
  - Also call register
- **What happens when**
  - CLK is low (0) ?





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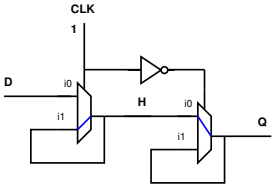
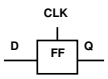
FLIP-FLOP (FF)

- **Use a pair to create a flip-flop**
  - Also call register
- **What happens when**
  - CLK is high (1) ?





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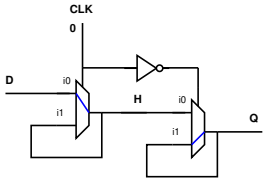
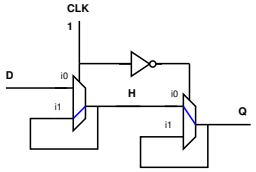
FLIP-FLOP (FF)

- **Use a pair to create a flip-flop**
  - Also call register
- **What happens when**
  - CLK transitions from 0 to 1?





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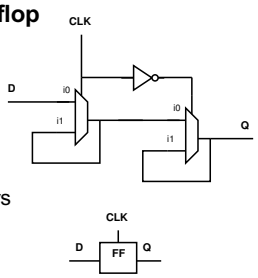
Flip-Flop (FF)

- **Use a pair to create a flip-flop**
  - Also call register
- **Sample D input on 0→1 transition of clock (CLK)**
- **Never an open path from D→Q**
  - One of the mux latches always in hold state



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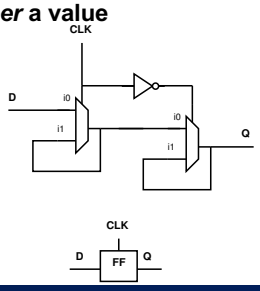
State Element

- **Latch or Register is a state element**
- **Allows circuit to *remember* a value**
- **Build computations that**
  - Depend on past inputs
  - Reuse hardware in time



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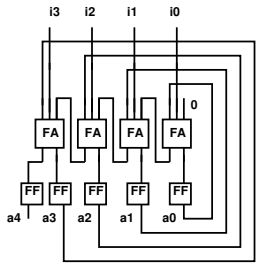
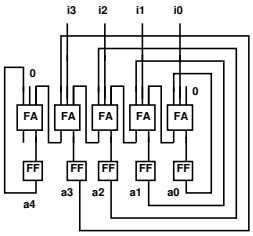
Accumulator Revisited

- Maybe extend accumulator bits to hold larger sum





- Maybe more…

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Part 2

Programmable Logic

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Preclass 2

- **How build 4-input mux from 2-input muxes?**

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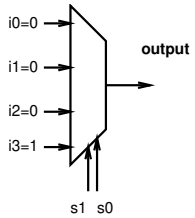
Preclass 4

- **What function of s0, s1 is this circuit configuration computing?**



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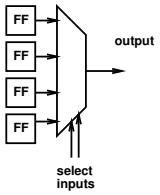
MUX CAN BE A PROGRAMMABLE GATE

- **Programmable Gate**
  - Can be programmed to act as any gate
  - Use state (e.g. FF) to "program" truth table of a gate

Input 0	Input 1	Output
0	0	
0	1	
1	0	
1	1	



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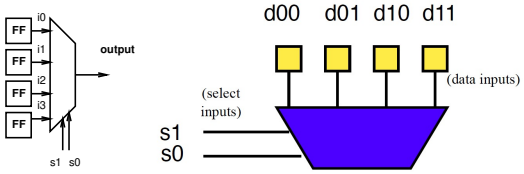
EXAMPLE: OR (PRECLASS 5)

- **How do we program to behave as OR2?**



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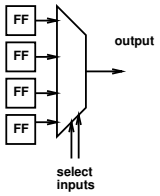
LOOK-UP TABLE (LUT)

- **Can generalize to any number of inputs**



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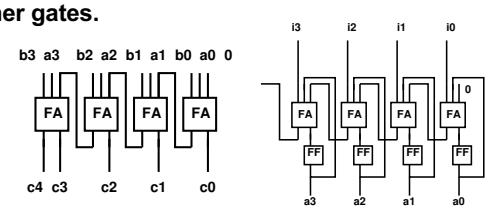
CONNECTING GATES

- **Once we can build gates**
- **…still need to connect the gates together.**
- **Select which gate outputs become inputs to other gates.**



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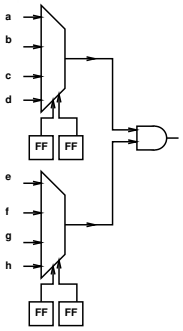
MUX CAN BE PROGRAMMABLE INTERCONNECT

Trick: Use multiplexer to programmably select gate input.



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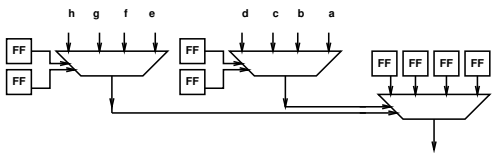
PROGRAMMABLE BLOCKS



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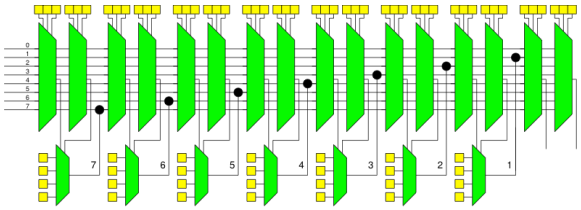
Programmable Gates and Interconnect

Preclass 6:
How program (fill in yellow programmable cells) to implement a full adder?



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Field-Programmable Gate Array (FPGA)

- **Collection of Programmable Gates**
  - Can "program" by setting state bits
  - LUTs that can be programmed to be any gate
    - With optional Flip-Flops to use for state
  - Programmable interconnect to "wire" the gates together

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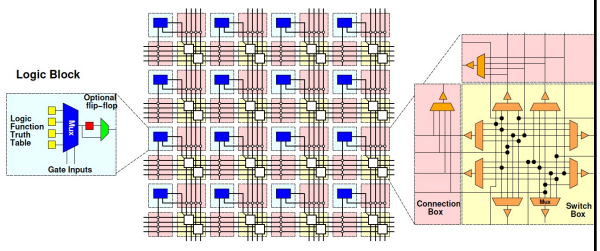
Field-Programmable Gate Array (FPGA)



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Part 3

Finite State Machines (FSMs)

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State for Sequencing and Control

- **Useful when trying to control things**
  - E.g. Perform a sequence of operations
- **Robot**
  - Open-gripper
  - Move-forward
  - Close-gripper
  - Lift

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State for Conditional Control

- **Useful when need to behave differently based on something in the past**
  - Remember if elevator going up or down
  - Remember/count coins from consumer
  - Remember some mode set by user
    - Displaying in Centigrade or Fahrenheit
- **Idea**
  - Store state
  - Use as input to logic

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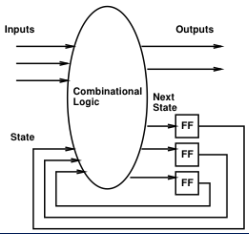
Finite-State Machine (FSM)

- **Sequential model of computation**
- **State (in registers) + combinational logic**
- **Compute outputs and next state from inputs and state**



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FSM Example

- **Simplified Vending Machine**
  - Only input quarters
  - Only vend one item (output signal to indicate vending)
  - Item costs 2 quarters
  - Coin Return request and control
- **Two states: waiting, one-quarter (one)**
- **Two inputs: quarter, coin-return (creturn)**
- **Two outputs: vend, return-quarter (qreturn)**

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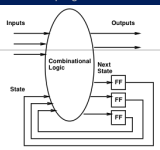
Truth Table Model

Complete together



state	quarter	creturn	vend	qreturn	next
waiting	0	0	0	0	waiting
waiting	0	1			
waiting	1	0	0	0	one
waiting	1	1			
one	0	0			
one	0	1			
one	1	0			
one	1	1			

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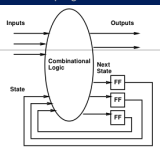
Truth Table Model

Complete together



state	quarter	creturn	vend	qreturn	next
waiting	0	0	0	0	waiting
waiting	0	1	0	0	waiting
waiting	1	0	0	0	one
waiting	1	1			
one	0	0			
one	0	1			
one	1	0			
one	1	1			

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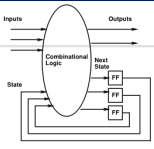
Truth Table Model

Complete together



state	quarter	creturn	vend	qreturn	next
waiting	0	0	0	0	waiting
waiting	0	1	0	0	waiting
waiting	1	0	0	0	one
waiting	1	1	0	1	waiting
one	0	0			
one	0	1			
one	1	0			
one	1	1			

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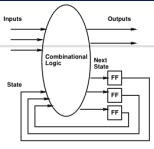
Truth Table Model

Complete together



state	quarter	creturn	vend	qreturn	next
waiting	0	0	0	0	waiting
waiting	0	1	0	0	waiting
waiting	1	0	0	0	one
waiting	1	1	0	1	waiting
one	0	0	0	0	one
one	0	1			
one	1	0			
one	1	1			

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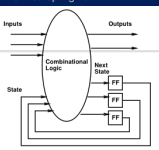
Truth Table Model

Complete together



state	quarter	creturn	vend	qreturn	next
waiting	0	0	0	0	waiting
waiting	0	1	0	0	waiting
waiting	1	0	0	0	one
waiting	1	1	0	1	waiting
one	0	0	0	0	one
one	0	1	0	1	waiting
one	1	0			
one	1	1			

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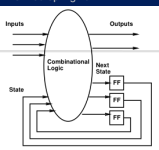
Truth Table Model

Complete together



state	quarter	creturn	vend	qreturn	next
waiting	0	0	0	0	waiting
waiting	0	1	0	0	waiting
waiting	1	0	0	0	one
waiting	1	1	0	1	waiting
one	0	0	0	0	one
one	0	1	0	1	waiting
one	1	0	1	0	waiting
one	1	1			

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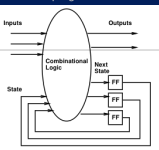
Truth Table Model



state	quarter	creturn	vend	qreturn	next
waiting	0	0	0	0	waiting
waiting	0	1	0	0	waiting
waiting	1	0	0	0	one
waiting	1	1	0	1	waiting
one	0	0	0	0	one
one	0	1	0	1	waiting
one	1	0	1	0	waiting
one	1	1	0	1	one

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Switch-Statement Model

```
While (true)
  switch (state) {
    case waiting:
        if (quarter && !creturn)
            state=one;
        else
            state=waiting;
        qreturn=quarter && creturn;
        vend=0;
        break;
```


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Switch-Statement Model (cont.)

```
    case one:
        if ((quarter && !creturn)||
           (!quarter&&creturn))
            state=waiting;
        else
            state=one;
        qreturn=creturn;
        vend=quarter&& !creturn;
        break;
  } // switch
} // while
```


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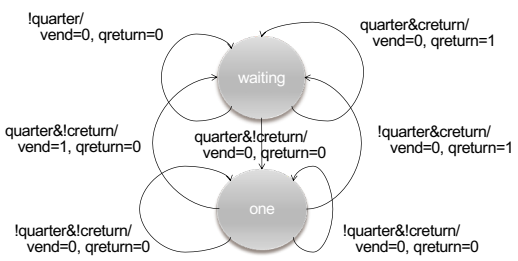
FSM Graph Model



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BIG IDEAS

- **Can implement any combinational digital logic function from:**
  - and, or, not gates
- **Can implement any FSM from:**
  - and, or, not gates and registers
- **Can build a single chip that can be programmed to behave as any collection of gates**
  - As long as don't need more gates than it provides

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LEARN MORE

- **CIS240 – do a bit more logic**
- **ESE370 – how to implement gates, latches, and memories from transistors**
- **CIS471 – implement processor (next time) using Verilog mapped to FPGAs**
- **ESE532 – how to build large-scale computations from logic**

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REMINDER

- **Feedback including Lab**
- **Lab 6 Report/formal writeup due tonight**
  - Before midnight
- **Lab 7 on Wednesday**
  - Prelab (with canvas/quiz turnin)

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