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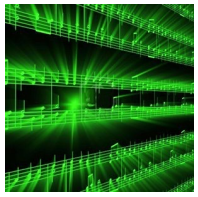

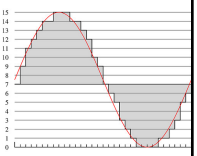

Lecture #24 – Intellectual Property 1

ESE150 Spring 2022

Slides 2018--2022 DeHon

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ESE 150 – Digital Audio Basics

1

Preclass

- **Cost to develop and write a book?**
  - 200 days @ $500/day
- **Cost per book (assume $1 to print book)**
  - Total volume 1
  - Total volume 10,000
  - Total volume 1 million
- **Book sells $10**
  - Value added by writer?
  - Copies sold to break even at $2/copy to writer?

2

Economic Terms

- **Production cost – expense to produce**
- **Price – what consume will pay for it**
  - Value to consumer
- **Profit = Price – cost**

3

Observe

- **Creative / Intellectual work produces most of value**
- **At least in volume, physical costs of reproduction is small part of product price**

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Preclass Continued

- **Cost to photocopy 200 page book at $0.05/page?**
- **Cost to scan book at 10page/minute?**
- **Cost to perform a 10s copy onto flash drive?**
- **Cost of portion of flash drive used**
  - $4 for 32GB drive, 0.5MB file

5

Observe

- **With digital representation**
  - Cost of “physical” reproduction trends to 0

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Past

- **Much of value in physical construction of objects**
  - Bridge, house, car, screwdriver
- **Expensive to reproduce / copy**
- **Reproductions imperfect**
  - 5th generation analog recording
  - 4th generation photocopy of text
- **Inherent barrier to making copies**
  - Value to buying original

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Digital Representation

- **Can represent perfectly in bits**
  - Including sound, words
- **Can make perfect copies**
- **Bits are cheap…and getting cheaper**
  - Copying "free"
- **Intellectual value disconnected from physical reproduction**

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What else has this property?

Digital Intellectual Property	Physical IP Renderer
Novel	eReader
Song (MP3)	MP3 Player
JPEG Photo	
	Video Player
Video Game	
	Arduino or Personal Computer
Verilog digital circuit	
STL (3D CAD drawing)	
DNA Sequence	DNA Printer

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Intellectual Property

- **Intangible creations of human intellect**
- **Have value**
- **Don't necessarily have physical embodiment on their own**

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Intellectual Property Creators

- **As Engineers**
  - Program, develop algorithms, design circuits
- **Almost everything we create will have this property**
  - Value added is intellectual
  - Can be represented digitally in bits
  - Can (increasingly) be copied/reproduced cheaply
- **Easy to have impact**
  - Our solutions can reach millions, billions
  - Decreasing physical barriers to propagation of solutions
- **Challenge to protect and reward IP creators**

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Outline

- Setup Need / Opportunity – What is IP
- **Where are we**
- **Rationale for IP Protection – Why Protect**
- **How protect?**
  - Patents
  - Copyrights
  - Open Source
  - NDA
  - Licensing

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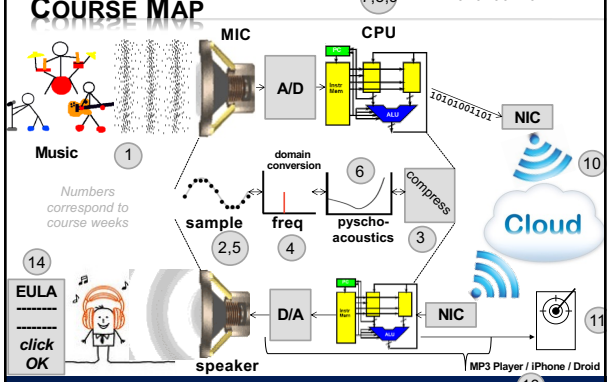
COURSE MAP



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Part 2

RATIONALE

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PRICING CHALLENGE

- **When cost of copying → 0**
  - Inventor/author must recover development cost
    - Price must include develop cost + copy cost
  - Copier does not have development cost
    - Price = copy cost + epsilon
    - Competition of copiers will drive epsilon down near 0
  - Inventor/author not compensated for development
    - Remove incentive/reward for development
- **Demand: developers need way to exclude others from copying to incentivize creation**

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ARROW'S INFORMATION PARADOX

- **Customer not know how to value information until see information (see details of product)**
  - Enough information to decide to buy
  - Enough information to decide what will pay for it
- **Once show customer information, sufficient detail, they have enough information to reproduce**
  - Could walk away and produce their own without paying for it
- **Disclosure of what effectively transfers technology**
- **Demand: protection for developer**
- Arrow, Kenneth J. Economic Welfare and the Allocation of Resources for Invention, in *The Rate and Direction of Inventive Activity*, 609 (Nat'l Bureau of Econ. Research ed. 1962).

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BALANCE INDIVIDUAL AND SOCIETAL GOOD

- **Individual should benefit form their own effort**
- **Society advances with the accumulation of knowledge**

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INTERLUDE: NIL NIKOLAI IVANOVICH LOBACHEVSKY

https://www.youtube.com/watch?v=gXlfXirQF3A

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Before copying was an issue

- **Concern that new developments/ideas would be lost when inventor die**
  - Techniques could remain secret for decades!
- **Incentive to make inventions known**
  - Advance the general welfare

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US Constitution

- **Article 1, Section 8, Clause 8:**
  - To promote the Progress of Science and useful Arts, by securing for limited Times to Authors and Inventors the exclusive Right to their respective Writings and Discoveries

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Mechanisms (To support)

- **Patents**
  - Cover inventions
  - E.g., Flying Machine (US 821,393), ENIAC (US 3,120,606),
- **Copyrights**
  - Creative expression
  - E.g., novel, song, movie

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Mechanisms for Protection

- **Messy and imperfect**
- **Haven't kept up with technology**
- **Likely need (and will need) innovation and refinement**

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Part 3

Patents

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Patent

- **Inventions**
- **Non-obvious to one "ordinary skill in art"**
- **Reduced to practice**
- **Cannot patent**
  - Abstract ideas
  - Laws of nature
- **US: First to file**
  - (prior to 2013 was first to invent)
- **Exclusive rights 20 years from filing**

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What might be tricky / non-satisfying?

- First to file? (even invent?)
- 20 year term?

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Patent

- **Identification of problem is part of invention**
- **Claims**
  - Define the invention
  - Technical coverage
- **Requires disclosure**
  - If really believe no one else will figure it out…or can copy it, may be better to keep as a *trade secret*
- **License to litigate**
  - Recover damages through litigation
  - Establish violation
  - Validity of many patents overturned in litigation

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Patent Process

- **US have one year from first-public disclosure to file**
  - Many places – public disclosure prevents patent
  - https://www.uspto.gov/web/offices/pac/mpep/s2153.html
- **May file provisional patent to get filing date**
- **File patent with claims**
- **Reviewed by examiner**
- **Examiner reports on what may be allowable**
  - As-is
  - With tighter qualifications
  - Not-at-all
  - On a per-claim basis
- **Typically requires several iterations**
- **Often year(s) before patent issues**
- **Filing costs thousands of dollars**
  - With lawyer/legal fees tens to hundreds of thousands

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US010725778B2

(12) **United States Patent**
DeHon et al.

(10) **Patent No.: US 10,725,778 B2**
(45) **Date of Patent: Jul. 28, 2020**

(54) **PROCESSING METADATA, POLICIES, AND COMPOSITE TAGS**

(71) Applicants: **The Charles Stark Draper Laboratory, Inc.**, Cambridge, MA (US); **The Trustees of the University of Pennsylvania Penn Center for Innovation**, Philadelphia, PA (US)

(72) Inventors: **Andre' DeHon**, Cambridge, MA (US); **Udit Dhawan**, New Delhi (IN)

(73) Assignees: **The Charles Stark Draper Laboratory, Inc.**, Cambridge, MA (US); **The Trustees of the University of Pennsylvania Penn Center for Innovation**, Philadelphia, PA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/002,642**

(22) Filed: **Jun. 7, 2018**

(65) **Prior Publication Data**

US 2018/0336031 A1 Nov. 22, 2018

Related U.S. Application Data

(60) Continuation of application No. 15/05,541, filed on Sep. 5, 2017, now Pat. No. 10,261,794, which is a (Continued)

(51) **Int. Cl.**
G06F 9/30 (2018.01)
G06F 9/38 (2018.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G06F 9/30101*** (2013.01); ***G06F 9/30072*** (2013.01); ***G06F 9/30098*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC G06F 12/0875; G06F 12/1408; G06F 12/1458; G06F 15/78; G06F 21/52;
(Continued)

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Nickolai Zeldovich et. al, Hardware Enforcement of Application Security Policies Using Tagged Memory, Proceedings of the 8th USENIX conference on Operating systems design and implementation pp. 225-240 (2008).*
(Continued)

Primary Examiner — Sharon S Lynch
(74) *Attorney, Agent, or Firm* — Hamilton, Brook, Smith & Reynolds, P.C.

(57) **ABSTRACT**

A method includes receiving, for metadata processing, a current instruction with a associated metadata tags. The metadata processing is performed in a metadata processing domain isolated from a code execution domain including the current instruction. Each respective associated metadata tag representing a respective policy of the composite policy. The associated metadata tags further including pointers to tags of a component policy of the composite policy. For each respective metadata tag, the method includes determining, in the metadata processing domain and in accordance with the metadata tag and the current instruction, whether a rule exists in a rule cache for the current instruction. The rule cache including rules on metadata used by said metadata processing to define allowed instructions. The determination of whether a rule exists resulting in a respective output. The method further includes generating a composite result tag by combining the respective outputs into a single metadata tag
(Continued)

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What is claimed is:

1. A method of processing instructions comprising:

receiving, for metadata processing, a plurality of metadata tags associated with a current instruction, said metadata processing being performed in a metadata processing domain isolated from a code execution domain including the current instruction, each of the plurality of metadata tags relating to a respective component policy of a composite policy;

processing the plurality of metadata tags in parallel by respective rule cache miss handlers comprising a plurality of hardware rule handlers, wherein processing, for each metadata tag of the plurality of metadata tags, comprises:

determining, by a respective rule cache miss handler, in the metadata processing domain and in accordance with the metadata tag and the current instruction, whether a rule exists in a rule cache for the current instruction, said rule cache including rules on metadata used by said metadata processing to define allowed instructions; and

providing a respective output;

generating a composite result tag by combining the respective outputs into a single metadata Tag for the composite policy including each respective policy; and

simultaneously enforcing, by the plurality of hardware rule cache miss handlers, each of the policies for the current instruction, each of the policies enforced by a respective hardware rule cache miss handler.

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US005742180A

United States Patent [19]
DeHon et al.

[11] **Patent Number: 5,742,180**
[45] **Date of Patent: Apr. 21, 1998**

[54] **DYNAMICALLY PROGRAMMABLE GATE ARRAY WITH MULTIPLE CONTEXTS**

[75] Inventors: **André DeHon**, Cambridge; **Thomas F. Knight, Jr.**, Belmont; **Edward Tau**, Boston; **Michael Bolotski**, Somerville; **Ian Eslick**, Cambridge; **Derrick Chen**, Cambridge; **Jeremy Brown**, Cambridge, all of Mass.

[73] Assignee: **Massachusetts Institute of Technology**, Cambridge, Mass.

[21] Appl. No.: **386,851**

[22] Filed: **Feb. 10, 1995**

[51] **Int. Cl.**[6] **H03K 19/177**
[52] **U.S. Cl.** **326/40**; 326/38
[58] **Field of Search** 326/38–40, 46

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Razdan, R., et al., "A High Performance Microarchitecture with Hardware–Programmable Functional Units," *Micro–27Proceedings of the 27th Annual International Symposium on Microarchitecture*, San Jose, California, pp. 172–180 (Nov. 30–Dec. 2, 1994).
(List continued on next page.)

Primary Examiner—Edward P. Westin
Assistant Examiner—Jon Santamauro
Attorney, Agent, or Firm—Hamilton, Brook, Smith & Reynolds, P.C.

[57] **ABSTRACT**

An integrated dynamically programmable gate array comprises a two dimensional array of programmable gates. These gates can be implemented as look up tables but hardwired gates with programmable interconnections are also possible. Each one of the gates receives plural input logic signals from plural other gates. Consequently, a broad range of logic combinations are possible. The gates further include locally stored multiple contexts dictating different combinatorial logic operations performed by the gates. The contexts increase the logic operations performable by the gate and the fact that the contexts are locally stored enables

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CLAIMS

We claim:

1. An integrated dynamically programmable logic array, comprising:

at least a two dimensional array of programmable logic elements, each one of the logic elements receiving plural input logic signals from plural other logic elements and including locally stored multiple contexts dictating different combinatorial logic operations performed by the logic elements; and

a context signal source that provides a context signal, indicating an active one of the contexts, commonly to the programmable logic elements of the array; and

wherein the contexts for each one of the logic elements are individually accessible so that a new context can be loaded into the logic elements while another context is controlling logic operations of the logic elements.

2. A programmable logic array as described in claim 1, wherein the context signal source provides the context signal up to every cycle of the programmable logic array.

3. A programmable logic array as described in claim 1, wherein the context signal source generates plural context signals that dictate contexts for regions of the array of the logic elements.

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XILINX FPGA US 4,870,302

[57] **ABSTRACT**

A configurable logic array comprises a plurality of configurable logic elements variably interconnected in response to control signals to perform a selected logic function. Each configurable logic element in the array is in itself capable of performing any one of a plurality of logic functions depending upon the control information placed in the configurable logic element. Each configurable logic element can have its function varied even after it is installed in a system by changing the control information placed in that element. Structure is provided for storing control information and providing access to the stored control information to allow each configurable logic element to be properly configured prior to the initiation of operation of the system of which the array is a part. Novel interconnection structures are provided to facilitate the configuring of each logic element.

I claim:

1. An interconnect structure for programmably interconnecting lines within an integrated circuit comprising:

at least three sets of interconnect line including a first set, a second set, and a third set;

programmable means, not including said sets of interconnect lines, for connecting at least one of said lines in said first set to at least one of said lines in said second set, for connecting at least one of said lines in said first set to at least one of said lines in said third set, and for connecting at least one of said lines in said second set to at least one of said lines in said third set.

2. An array of interconnect structures, each said interconnect structure as in claim 1, and each interconnect structure in said array having its own selected number of interconnect lines and its own programmable means for connecting interconnect lines in its own first, second and third sets.

https://patents.google.com/patent/US4870302A/en?oq=us+4870302

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ENIAC US 3,120,606

- 1. MEANS FOR PRODUCING ELECTRIC PULSES IN SEQUENCE, ELECTRONIC MEANS FOR ALTERNATELY TRANSMITTING CERTAIN ONES OF SAID PULSES AS RECURRENT DIFFERENTIATED GROUPS, ELECTRONIC MEANS FOR SELECTING PARTICULAR PULSES FROM ONE OF SAID DIFFERENTIATED GROUPS TO REPRESENT QUANTITATIVE VALUES, ELECTRONIC MEANS FOR SELECTING PARTICULAR PULSES FROM ANOTHER OF SAID DIFFERENTIATED GROUPS TO REPRESENT CERTAIN QUALITATIVE VALUES, READING MEANS RESPONSIVE TO PULSES REPRESENTING BOTH THE QUALITATIVE AND QUANTITATIVE VALUES FOR READING DATA TO BE PROCESSED UPON COMMAND OF AT LEAST ONE OF SAID QUALITATIVE PULSES, STORING THE DATA THUS READ, AND MAKING THE DATA AVAILABLE IN THE FORM OF DATA PULSES IN RESPONSE TO AT LEAST ONE OTHER OF SAID QUALITATIVE PULSES, AND ELECTRONIC MEANS FOR RECEIVING SAID DATA PULSES AND RESPONSIVE THERETO FOR PERFORMING ELECTRICAL SWITCHING OPERATIONS OF A NATURE DETERMINED BY SELECTED ONES OF SAID QUALITATIVE VALUES AND OF A DEGREE DETERMINED BY SELECTED ONES OF SAID QUANTITATIVE VALUES.

https://www.computerhistory.org/revolution/birth-of-the-computer/4/99/387

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WHAT'S PATENTABLE

- **Not law's of nature**
- **Not abstract ideas**
- **Cannot patent pi (π)**
- **Software?**
  - Originally not
  - With reference to machine, can often manage
- **Genetic sequences?...**
- **…evolving…**

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COPYRIGHT

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COPYRIGHT

- **Cover particular, original expression**
  - Including software
- **Technically don't need to register**
  - But should…
  - Must register before sue for infringement
  - $35
  - No review, just registration
- **Life of author + 70 years**
- **Work for hire: 95 years from publication**

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TRADITIONALLY: TRANSFER COPYRIGHT …

- **Publish in ACM, IEEE journal**
  - Transfer copyright to them, they license you back rights for derived work and post on person web site.

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RECENT: LICENSE TO ACM, IEEE

- **Author retain copyright, license to publisher**

FPGA '17, February 22 - 24, 2017, Monterey, CA, USA

ISBN 978-1-4503-4354-1/17/02…$15.00

DOI: http://dx.doi.org/10.1145/3020078.3026124

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BIG IDEAS

- **We (engineers…particularly in computing space) are knowledge workers, producing IP**
- **IP carries great value**
  - That is less and less tied to physical objects
- **Need to equitably reward and encourage IP creation**
- **Patents, Copyrights…**two of the things that
  - Attempts to provide framework for IP ownership, sharing, monetization
  - …probably not the final answer, particularly as technology landscape continues to evolve.

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REMEMBER

- **Feedback including Lab**
- **Lab 11 due today**
- **Lab 12 Wednesday**

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