

University of Pennsylvania
ESE206: Electrical Circuits and Systems II – Lab

MOSFET (Field Effect Transistor) Lab

Biasing and Amplification of a Common-Source Voltage Amplifier

1. Objectives

The objectives of this second MOSFET lab are:

1. To bias a NMOS transistor.
2. To use a NMOS transistor in a common-source amplifier configuration and to measure its amplification.
3. To study the effect of the source resistor and bypass capacitor on the amplification.
4. To study the effect of a load resistor on the amplification.
5. To build a common-source amplifier with active load (PMOS) and to measure the amplification. (BONUS assignment only).

2. Background

In class you learned how a MOSFET could be used as a basic common-source amplifier. You noticed that choosing a proper bias point on the transfer characteristic is very important to ensure good amplification and reduce the amount of distortion while allowing for a good output voltage swing. In today's lab you will learn how to properly bias a NMOS transistor in a common-source configuration and use this circuit to amplify an input signal.

2.1 Biasing

The common-source amplifier with a NMOS transistor is shown in Figure 1. The biasing is done by fixing the gate voltage with a voltage divider and also by using a source resistor R_S . The source resistor gives negative feedback and stabilizes the bias current as a function of temperature variations and transistor characteristics. This is a popular biasing scheme for discrete transistor circuits. Other biasing methods are possible, such as using a drain-to-gate feedback resistor, or using a constant-current source. The latter one is popular in integrated circuits. We will focus on the first method, illustrated in Figure 1.

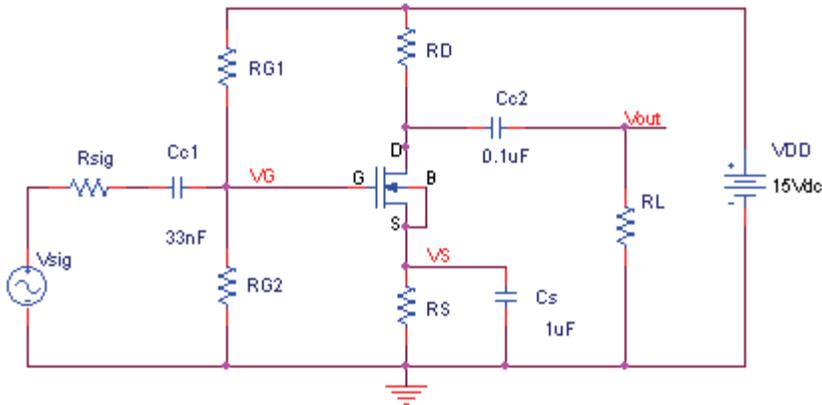


Figure 1: Common-source amplifier in which biasing is done through a voltage divider and a source resistor. The input signal v_{sig} is coupled to the gate through a coupling capacitor C_{C1} . In this circuit we have connected the body terminal to the source terminal.

Biasing: Rule of Thumb

For proper biasing we can use the following rule-of-thumb. We select the source resistor value such that the voltage V_S at the source terminal is about one third to one fifth of the power supply V_{DD} . The resistance R_D is chosen such that the drain voltage V_D is about in the middle of V_{DD} and V_S . This is done so that the signal at the drain has a relatively large and symmetrical output swing. These two conditions give us the resistor values of R_S and R_D for a specified drain current. The gate voltage can then be easily calculated as follows. Since the transistor is operating in the saturation region (see previous lab), we know that the current-voltage relationship is given by,

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 \quad \text{when } v_{DS} > (v_{GS} - V_t) \quad (1)$$

Thus to obtain a certain bias current I_D we need to apply a gate-source voltage V_{GS} equal to,

$$V_{GS} = V_t + \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}} \quad (2)$$

The corresponding gate voltage V_G is then equal to,

$$V_G = V_S + V_{GS} = V_S + V_t + \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}} \quad (3)$$

Once the gate voltage V_G is known, one can find the values of the resistor R_{G1} and R_{G2} . We choose the resistors such that the parallel resistor is relatively large to ensure a large input resistance of the amplifier and prevent loading of the signal source $R_{in} = R_{G1} || R_{G2}$.

The factor $(V_{GS}-V_t)$ is called the saturation voltage and corresponds to the minimal drain-source voltage required to keep the transistor in saturation. It is sometimes called the overdrive voltage.

$$V_{GS} - V_t = \sqrt{\frac{2I_D}{k'_n \frac{W}{L}}} = V_{DSat} \quad (4)$$

For the amplifier to operate properly one should make sure that the drain voltage does not go lower than

$$V_D > V_S + V_{DSat} = V_G - V_t. \quad (5)$$

This voltage will determine the output voltage swing.

2.2 Amplification

For signal frequencies of interest we can assume that the capacitors act as a short circuit what implies that the AC circuit can be drawn as shown in Figure 2a. . The transistor can be replaced by its small signal equivalent circuit of Figure 2b.

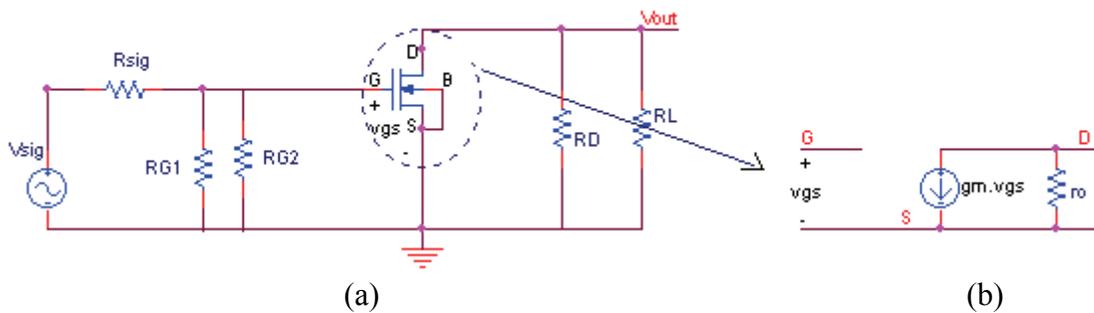


Figure 2 (a) AC circuit of the common-source amplifier and (b) the small signal equivalent transistor model.

One of the most important characteristics of a transistor is its *transconductance* g_m that is a measure of how much the output current will vary when its input voltage v_{gs} changes. The transconductance g_m can be written as follows,

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \Big|_Q = k'_n \frac{W}{L} (V_{GS} - V_t) = \sqrt{2I_D k'_n \frac{W}{L}} \quad (6)$$

$$g_m = \frac{2I_D}{V_{GS} - V_t}$$

Thus the value of the transconductance depends on the bias current I_D .

The output resistor r_o is given by the ratio of the Early voltage ($=1/\lambda$) over the bias current,

$$r_o = V_A/I_D = 1/\lambda I_D. \quad (7)$$

One can then easily calculate the expression of the amplification A_v ,

$$A_v = -g_m (R_D \parallel R_L \parallel r_o) \approx -g_m (R_D \parallel R_L) \quad (8)$$

The last approximation assumes that $r_o \gg R_D \parallel R_L$.

The open-circuit voltage gain A_{vo} is the gain when R_L is removed $A_{vo} = -g_m R_D$.

In case the signal source has an internal resistance R_{sig} (not shown in Fig. 1 and 2), the value of the overall amplification will become,

$$G_v = -\frac{R_G}{R_G + R_{sig}} g_m (R_D \parallel R_L \parallel r_o) \approx -\frac{R_G}{R_G + R_{sig}} g_m (R_D \parallel R_L) \quad (9)$$

Notice that the internal resistance forms a voltage divider with the resistance $R_G = R_{G1} \parallel R_{G2}$ which attenuates the input signal. It is for that reason that we need to keep the parallel resistance $R_{G1} \parallel R_{G2}$ large as compare to R_{sig} (see section on biasing).

The input resistance of the amplifier is equal to $R_G = R_{G1} \parallel R_{G2}$ and the output resistance $R_{out} = r_o \parallel R_D$. For a voltage amplifier one likes to keep the input resistance large and the output resistor small. For the common-source amplifier, the input resistance is large. However, the output resistance is also large. It is for this reason that by adding a load resistor R_L at the output, the output voltage and thus the amplification reduces. In order to obtain a small output resistance, one can add a common-drain (or source follower) configuration after the common-source amplifier.

3. Pre-lab assignment

3.1 Read the section on "Biasing by Fixing V_G and connecting a Resistance on the Source" (section 4.5.2) and "The Common-Source Amplifier" (section 4.7.3, Sedra-Smith, 5th ed.).

3.2 Your task is to design the common-source amplifier of [Figure 1](#) with a bias current $I_D = 0.6\text{mA}$. The source voltage V_S should be 3V and the drain voltage V_D should be chosen such that it is in the middle of V_S and V_{DD} . The input resistance should be larger than 15 kOhm.

The NMOS transistor (CD4007CN array) has the following characteristics:

$$V_t = 1.2\text{V}$$

$$k_n'W/L=0.7\text{mA/V}^2$$

$$\lambda=0.004\text{V}^{-1}$$

$$\gamma=1.9\text{V}^{0.5}$$
 (note: since source-bulk terminal are shorted you won't need to use to calculate the threshold voltage).

- Find the value of V_D .
- Find the resistor values R_S , and R_D . Select values that are available in the lab (check the [available resistor values](#) in the RCA lab).
- Using the actual resistor value of R_S find V_S and V_G .
- Find the values of the resistors R_{G1} , and R_{G2} .
- What is the total DC power dissipation in the amplifier? (hint: power dissipation is $V_{DD}I_{\text{total}}$).

3.3 Using the values of the resistors and the bias current I_D , find the amplification of the amplifier:

- Calculate the value of the transconductance g_m and small signal output resistor r_o .
- Assume that no load resistance R_L is present, find the value of A_{v0} .
- Calculate the voltage gain A_v for the case of a load resistance $R_L=10\text{ k}\Omega$ is added as shown in Figure 1.
- Assume that a source resistance R_{sig} of $5\text{ k}\Omega$ is present, what is the effect on the overall amplification G_v ? What is the value of the overall voltage gain G_v with both R_{sig} and R_L present?
- What is the minimum voltage at the source in order to keep the transistor in saturation? What is the corresponding voltage swing?
- Summarize the amplifier characteristics in table form: DC current and voltages (I_D , V_D , $V_{D\text{min}}$), total power dissipation, transconductance g_m , input resistance R_{in} , output resistance $R_o=R_D||r_o$, amplification with and without load resistance R_L . Assume that signal source has a negligible internal resistance.

3.4 **Verify your design using PSpice.** You will need to use a model for the CD4007 transistor. The models can be found in the ESE216LIB library which can be downloaded from the website. Save both the [cd4007.lib](#) and [cd4007.olb](#) files in your directory. The transistors are called nmMos for the NMOS and ppMos for the PMOS. You will need to add this library when drawing the schematic. Also, when creating a new Simulation Profile, while doing the simulation, you will need to add the library path and Filename (under the Libraries tab). See [PSpice Primer](#), section 4 on "Using and Adding Vendor Libraries"

- Enter the schematic of [Figure 1](#) without the load resistor R_L and coupling capacitor C_{C2} . For the transistor you need to add the CD4007 Library.
- Bias simulation. Simulate the circuit of Figure 1 (without the load resistor R_L). Do a BIAS simulation and find the DC voltages at each node and current I_D . Compare the results with the one you calculated in section 3.2 above.
- Next, do a transient simulation. Use as input signal a sinusoidal source (V_{sin}) of 5 kHz frequency and amplitude of 0.2V . Do this first without a load resistor and next with a load R_L of $10\text{ k}\Omega$. Find the output voltage. What is the voltage amplification A_{v0} and A_v ? Compare the simulation results with your hand calculations.

- d. Do a frequency sweep (AC simulation) by replacing the input source by an AC source, Vac. Simulate the circuit with the load resistor of 10kOhm connected. Sweep the frequency from 10 Hz up to 100 kHz. Find the low-frequency cut-off point. Plot the Bode diagram of the amplification. Determine the low-frequency cut-off and mid-frequency amplification. How does the amplification compare with the one of the transient simulation?
- e. Summarize the simulation results in table form on a separate sheet and hand it in together with the calculations and the simulation print-outs. Label each graph clearly.

4. In-Lab Experiments

Parts

1 - HFC4007UB MOS transistor array ([data sheet](#) from National Semiconductor)
1 - 33 nF capacitor
1 - 0.1 microFarad capacitor
1 - 1 microFarad capacitor
1 - 10 kOhm resistor
1 - 50 kOhm resistor
2 - resistors: TBD
1 - 100 kOhm potentiometer
Power supplies
Oscilloscope with FFT module
Digital multimeter (Voltage and Current meter)

Procedure

You will be using the same CD4007 MOSFET array as in the previous lab. This array contains three NMOS and three PMOS transistors as shown in Figure 3. Again, the key point to remember is that the bulk (or substrates) of all NMOS transistors are connected to the VSS (pin 7) and all PMOS substrates are connected to VDD (pin 14). When using this array pin 7 should be connected to the most negative supply voltage or to the source of the transistor. Pin 14 is the substrate of the PMOS and must be connected to the most positive supply voltage in the circuit!

It should be mentioned that the transistor characteristics of the CD4007 could vary considerably from chip to chip. The transistors may come from a different batch, what can explain why the threshold voltage, the transconductance parameter and the output resistance is different from the one used in the hand calculations and Spice simulation.

Precaution: MOSFET transistors are very susceptible to breakdown due to electrostatic discharge. It is recommended that you always ground yourself before picking up the MOSFET chip. Do not touch any of the pins of the chip.

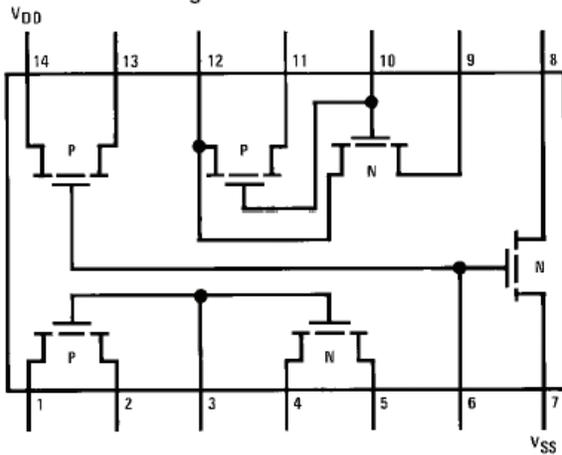


Figure 3: The HFC4007UB MOSFET array. Pin 7 is connected to the substrate of the NMOS and *should be connected to the most negative voltage of the circuit (Or in some cases can be shorted to the source if and only if you use one NMOS transistor on the array!)*; pin 14 is the bulk of the PMOS and should be connected to the most positive voltage in the circuit. (Source: National Semiconductor [HFC4007 Datasheet](#))

4.1. Biasing of the transistor

The goal of this experiment is to bias the transistor of Figure 1 according to the calculations of the pre-lab. After building the circuit you will verify the biasing voltages and currents..

- a. Build the circuit of Figure 4. Use the transistor between the pins 3, 4 and 5. Notice that we have connected the bulk (pin 7) to the source (pin 5) of the NMOS transistor. This can be done since we are only using a single NMOS transistor in the array. The reason for shorting drain-to-bulk is to eliminate the back-gate (body) effect on the threshold voltage. For the biasing resistor R_{G2} , use a 100 kOhm potentiometer.
- b. Measure the DC voltage at the drain. Important is to position the drain voltage V_D around 9 or 10 V. Adjust the potentiometer R_{G2} so that V_D is around 9V. After adjusting the gate voltage, measure the gate and source voltages. What is the corresponding drain current I_D ?

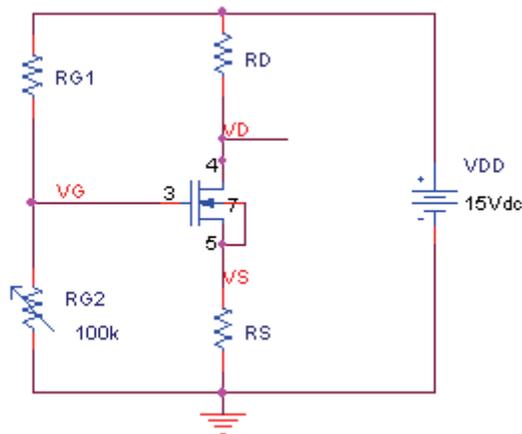


Figure 4: Biasing circuit of the common-source amplifier..

4.2 Common-Source Amplifier with Resistive load

Next you will use the transistor as an amplifier and measure its amplification and frequency response. You will also study the effect of the source and load resistors on the amplification.

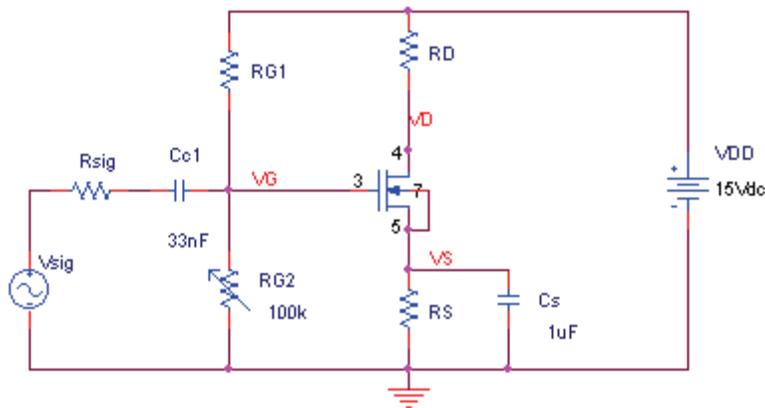


Figure 5: Common-source amplifier (R_{sig} is the internal resistor of the function generator and is about 50 Ohm).

- Modify the circuit of Figure 4 by adding the capacitors C_{C1} , and C_S as shown in Figure 5. Connect a sinusoidal input signal of 0.2V amplitude (0.4Vpp) and 5kHz frequency.
- Measure the voltage swing at the drain using the oscilloscope. Display the v_D on one channel and the input voltage v_{sig} on the other channel. Measure the peak to peak values of the input and output signal. What is the open-circuit amplification (voltage gain) A_{vo} ? Notice the phase relationship. Take a snapshot for your report. How does it compare to the calculated one? It should be mentioned that the transistor characteristics can vary considerably from chip to chip. It is not unusual the measured values differ by as much as 10-20% from the specified ones.
- Increase the amplitude of the input signal and observe the output signal. When does the output signal start to distort? What is the maximum output voltage swing before considerable distortion occurs?
- Reduce the input signal so that the output signal looks undistorted. Measure the FFT of the output signal and determine the total harmonic distortion (to be done in your report). Write down how many dB the amplitude of the harmonics are below the amplitude of the fundamental frequency. Take a snapshot of the FFT (include the vertical scale in dB).
- Let's remove the bypass capacitor C_S over the source resistor. Measure the output signal. What is the amplification? Notice the strong effect of removing the capacitor on the amplification. Take a snapshot.
- Replace the capacitor C_S over the source resistor. Add the coupling capacitor C_{C2} and the load resistor R_L , as shown in [Figure 1](#). Use of C_{C2} a value of 0.1 uF and for R_L a value of 10 kOhm. Measure the output voltage v_O and the corresponding amplification A_v . Notice that the DC voltage has been removed from the output voltage. What happened to the amplification? For your report, include a brief discussion on the effect of R_L .

- g. Measure the frequency response of the amplifier with the load resistor connected. Change the frequency of the input signal. Starting from 5 kHz, reduce the frequency till the amplitude of the output has decreased by a factor of 0.707 (or 3dB). Record this 3dB frequency. What is the phase relationship between input and output signal? Next, increase the value of the input frequency till the amplification A_v reduces to 0.707 of its value at 5kHz. Record the high-frequency 3dB point. What is the bandwidth of the amplifier? What is the Gain-Bandwidth product? For your report, can you explain the measured value of the low-frequency 3dB point? What causes this frequency cut-off?

For your report, include the results of your measurement and compare with hand calculations. Discuss the results when appropriate. Include also the calculation of the total harmonic distortion. Explain the low-frequency roll-off.

4.3 BONUS Assignment Common-Source Amplifier with active PMOS Load (extra 20 pts)

This part is not required but can be done for extra credit (20 pts).

The goal of this experiment is to replace the drain resistor R_D by a PMOS transistor. We call this an active load. The advantage of doing so is: (1) larger resistor (i.e. the output resistance r_o) and thus a larger amplification; (2) no need to use a resistor. The latter is of particular importance for integrated circuits where large resistors are hard to make and occupy a large area.

The basic amplifier transistor is still the NMOS. However a current source has been replaced the load resistor R_D , as schematically shown in Figure 6a. The resistor R_G sets the gate voltage V_G and is kept very large in order not to load the input source. A current source can be implemented with a PMOS current mirror as shown in Figure 6b.

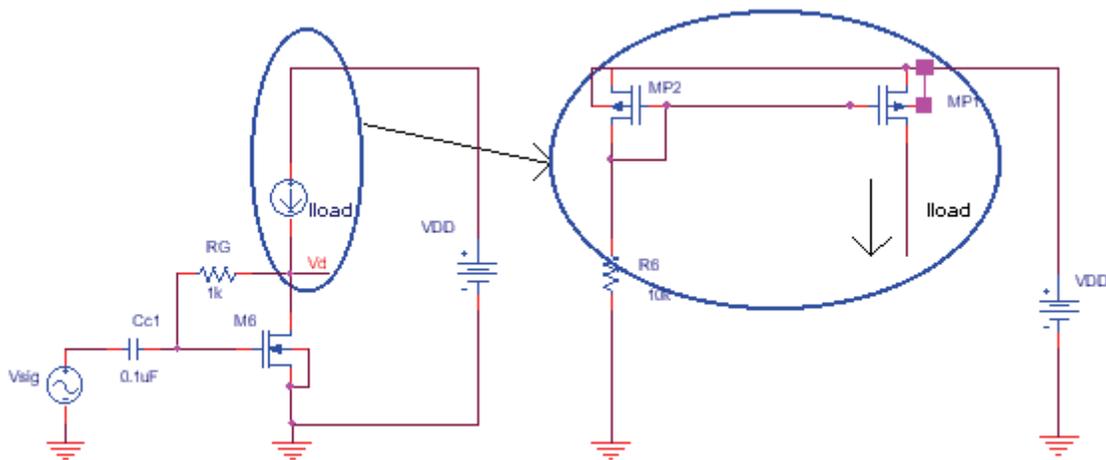


Figure 6 (a) Common-Source amplifier with a current source as the load; (b) the current source can be implemented by a PMOS current mirror.

By replacing the current source by the current mirror, we obtain the complete amplifier with active load as shown in Figure 7. We have also added a load resistor R_L and a coupling capacitor C_{C2} .

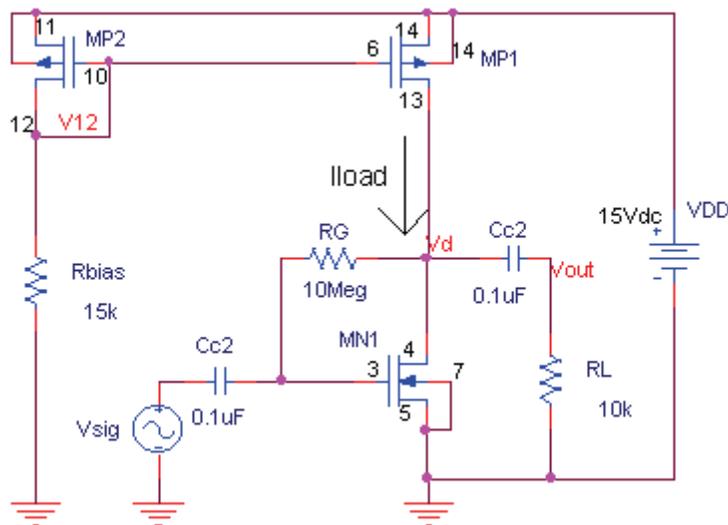


Figure 7: Common-Source amplifier with active load.

- Build the circuit of Figure 7. For now do not include the load resistor R_L and a coupling capacitor C_{C2} . The pins of the transistor of the CD4007 array are given in the schematic. Use short jumpers on your protoboard to connect the pins of the transistors.
- Measure the DC voltages V_{12} , and V_D . (and thus V_G) What is the corresponding drain current $I_D = I_{load}$?
- Apply a sinusoidal input source V_{sig} with amplitude of 50mV and frequency 5kHz. Measure the output voltage v_d (do not include the load resistor or C_{C2}). If needed adjust the input amplitude to prevent distortion of the output signal. What is the open-circuit voltage amplification A_{v_o} ? What do you notice about the magnitude of the amplification, as compared to the one you measure on amplifier of Figure 1? Take a snapshot for your report.
- Now connect C_{C2} and the load resistor $R_L = 10 \text{ k}\Omega$. Measure the output voltage V_{out} over the resistor R_L . What is the amplification A_v ? Notice the effect of the load on the amplification. Take a snapshot for your report.
- For your report discuss the effect of the active load on the amplification. Can you calculate the value of the amplification? (Hint: replace R_D in the expression of the amplification (8) by the parallel of the output resistances of the PMOS and NMOS transistors. Assume that the PMOS has the following characteristics: $V_t = -1.0 \text{ V}$, $k_p' W/L = 0.7 \text{ mA/V}^2$ and $\lambda = 0.035 \text{ V}^{-1}$.

References

1. "Microelectronic Circuits, Sedra, Smith, 5th edition, Oxford University Press, New York, 2004.
2. "The Art of Electronics", Horowitz and Hill, Cambridge University Press.
3. "CD4007M/CD4007C Dual Complementary Pair Plus Inverter" [Datasheet](#), National Semiconductor, 1995.
4. "HCF4007UB Dual Complementary Pair Plus Inverter," Datasheet, ST Microelectronics, 2004.

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