Common Base BJT Amplifier
Common Collector BJT Amplifier

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## Basic Single BJT Amplifier Features

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<td>r_o$)</td>
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CE BJT amplifier => CS MOS amplifier  
CC BJT amplifier => CD MOS amplifier  
CB BJT amplifier => CG MOS amplifier
Common Collector (Emitter Follower) Amplifier

In the emitter follower, the output voltage is taken between emitter and ground. The voltage gain of this amplifier is nearly one – the output “follows” the input - hence the name: emitter “follower.”
**DC Bias**

The diagram shows a circuit with various components labeled:

- $100\,\text{k\Omega}$
- $R_E$
- $R_S$
- $V_{cc}$
- $v_s$
- $C_{in}$
- $i_C$
- $v_O$
- $R_{B}$
- $R_{E}$
- $V_{cc}/2$
- $6\,\text{V}$

The circuit includes:

- A resistor labeled $100\,\text{k\Omega}$
- A resistor labeled $R_E$
- A capacitor labeled $C_{in}$
- A voltage source $V_{cc}$
- A voltage source $v_s$
- A resistor labeled $R_S$
- A resistor labeled $R_B = R_1 \parallel R_2$
- A voltage source $v_O$
- A resistor labeled $R_E$
- A voltage source $V_{cc}/2$
- A resistor labeled $5.1\,\text{k\Omega}$

The circuit is designed to illustrate the concept of DC bias in electronic circuits.
Follower Small Signal Analysis - Voltage Gain

Circuit analysis:

\[ v_s = (R_s + r_\pi) i_b + R_E i_e = (R_s + r_\pi + (\beta + 1) R_E) i_b \]

Solving for \( i_b \):

\[ i_b = \frac{v_s}{R_s + r_\pi + (\beta + 1) R_E} \]

\[ v_o = R_E i_e = R_E (1 + \beta) i_b \]

\[ v_o = \frac{R_E (\beta + 1) v_s}{R_s + r_\pi + (\beta + 1) R_E} \]

for Current Bias Design replace \( R_E \) with \( r_o || r_o = r_o / 2 >> R_E \)

\[ \text{Av} = \frac{v_o}{v_s} = \frac{R_E r_o || r_o}{R_s + r_\pi + (\beta + 1) R_E} \approx 1 \]

Kenneth R. Laker, updated 27Sep13 KRL
Small Signal Analysis – Voltage Gain - cont.

\[ \frac{v_o}{v_s} = \frac{R_E}{R_s + r_\pi + R_E} \]

Since, typically:

\[ \frac{R_s + r_\pi}{(\beta + 1)} \ll R_E \quad \text{(or } r_o || r_o = r_o/2) \]

Note: \( A_V \approx 1 \)

Note: \( A_V \) is non-inverting
Of What value is a Unity Gain Amplifier?

CC Amplifier
- Voltage Gain ($A_v$): low (about 1)
- Current Gain ($A_i$): High ($\beta + 1$)
- Input Resistance: high ($R_B || \beta R_E$)
- Output Resistance: low ($r_e$)

Or Buffer
Emitter Follower Small Sig. Output Resistance

Assume:
\[ I_C = 1 \text{ mA} \Rightarrow r_\pi = \frac{V_T}{I_B} = \beta \frac{V_T}{I_C} = 2500 \Omega \]
\[ \beta = 100 \quad R_s = 50 \Omega \]

\[ R_{out} \approx r_e = \frac{2550}{100} = 25.5 \Omega \]

Recall \[ R_{in} = r_{bg} = r_\pi + (\beta + 1) R_E \]
Multisim Verification of $R_{out}$

Thevenin equivalent for the short-circuited emitter follower.

If $\beta = 200$, as for most good NPN transistors, $R_{out}$ would be lower - close to 12 $\Omega$.

Multisim short circuit check ($\beta = 100$, $v_{oc} = v_s$):

$$R_{out} = \frac{v_{oc}}{i_{sc}} = \frac{v_s(rms)}{i_{sc(rms)}} = \frac{1 V}{39.61 mA} = 22.25 \Omega$$
Consider the case where a $R_L = 50 \, \Omega$ load is connected through an infinite capacitor to the emitter of the follower. Using its Thevenin equivalent:

$$v_o = \frac{R_L}{R_L || R_E + R_{out}} A_v v_s = \frac{50}{75} v_s = \frac{2}{3} v_s$$

$$i_o = \frac{A_v v_s}{R_{out} + R_L || R_E} = \frac{v_s}{75}$$

$$P_o = v_o i_o = \frac{2}{225} v_s^2$$

At midband where $A_v = 1$

$$R_{out} \approx 25 \, \Omega$$

$$i_s = i_b = \frac{v_s}{R_{in}} \approx \frac{v_s}{(\beta + 1) R_L || R_E} \approx \frac{v_s}{101 \cdot 50} \approx \frac{v_s}{5000}$$

$$R_E || R_L = 5.1 \, k \, \Omega || 50 \, \Omega \approx 50 \, \Omega$$

$$P_s = v_s i_s \approx \frac{1}{5000} v_s^2$$

$$A_{pwr} = \frac{P_o}{P_s} = \frac{2(5000)}{225} = 44.4 \gg 1$$
Quick Review

Voltage Gain ($A_v$)?

Current Gain ($A_i$)?

Input Resistance?

Output Resistance?
Quick Review

CC Amplifier
- Voltage Gain ($A_v$): low (about 1)
- Current Gain ($A_i$): High ($\beta + 1$)
- Input Resistance: high ($\left(R_B || \beta R_E\right)$)
- Output Resistance: low ($r_o$)

VCVS or Buffer
Base Voltage Biasing – Typical Design

Split bias voltage drops about equally across the transistor \( V_{CE} \) (or \( V_{CB} \)) and \( V_{RE} \) (or \( V_B \)). For simplicity, choose:

\[
V_B = \frac{V_{CC}}{2} \quad \Rightarrow \quad R_1 = R_2
\]

Then, choose/specify \( I_E \), and the rest of the design follows:

\[
R_E = \frac{V_E}{I_E} = \frac{V_{CC}/2 - 0.7}{I_E}
\]

For an assumed \( \beta = 100 \):

As with CE bias design, stable op. pt. => \( R_B \ll (\beta + 1) R_E \), i.e.

\[
R_B = R_1 \parallel R_2 = \frac{R_1}{2} = \frac{(\beta + 1)}{10} R_E \approx 10 R_E
\]

\[
R_1 = R_2 = 20 R_E
\]
Typical Design - Cont.

Given:  \( R_{out} = r_e = 25 \, \Omega \)
\( V_{CC} = 12 \, V \)

And the rest of the design follows

\[
I_E \approx I_C = \frac{V_T}{r_e} = 1 \, mA
\]

\[
R_E = \frac{V_E}{I_E} = \frac{12/2 - 0.7}{10^{-3}} = 5.3 \, k\Omega
\]

Use standard sizes

\[
R_E = 5.1 \, k\Omega
\]
\( R_1 = R_2 = 100 \, k\Omega \)
Use the base current expression:

\[ v_{bg} = r_\pi i_b + R_E i_E = (r_\pi + (\beta + 1) R_E) i_b \]

This transistor input resistance \( r_{bg} \) is in parallel with \( R_B = 50 \, \text{k}\Omega \); 

\[ \frac{v_{bg}}{i_b} = r_\pi + (\beta + 1) R_E \approx (\beta + 1) R_E = 101 \cdot 5.1 \, \text{k} = 515 \, \text{k} \, \Omega \]

Ideally we want \( v_{bg} = v_s \) for \( f \geq f_{\text{min}} \)
Choose $C_{in}$ such that its reactance is $\leq 1/10$ of $R_B$ at $f_{\text{min}}$:

$$\frac{1}{2\pi f C_{in}} = \frac{R_B}{10}$$

$$C_{in} \geq \frac{10}{2\pi f_{\text{min}} R_B}$$

Assume $f_{\text{min}} = 20$ Hz

with $R_B = 50 \text{ k}\Omega$

$$C_{in} \geq \frac{10}{2\pi \cdot 20 \cdot 50 \cdot 10^{-3}} = 1.59 \mu F$$

Pick $C_{in} = 3.3 \mu F$), the nearest standard value in the Detkin Lab.

We could be (unnecessarily) more precise and include $r_{bg}$ and $R_s$ as part of the total resistance in the loop.
Final Design

![Circuit Diagram]

- $C_{in} = 3.3 \text{ uF}$
- $R_S = 50 \text{ Ohm}$
- $R_1 = 100 \text{ k Ohm}$
- $R_2 = 100 \text{ k Ohm}$
- $R_E = 5.1 \text{ k Ohm}$
- $V_{CC} = 12 \text{ V}$
**Multisim Simulation Results**

20.74 Hz Data \( A_v = 0.989 \)

1 kHz Data \( A_v = 0.995 \)
The Common Base Amplifier

Voltage Bias Design

Current Bias Design
Common Base Configuration

Both voltage and current biasing follow the same rules as those applied to the common emitter amplifier.

Insert a blocking capacitor in the input signal path to avoid disturbing the dc bias.

The common base amplifier uses a bypass capacitor – or a direct connection from base to ground to hold the base at ground for the signal only!

RECALL: The common emitter amplifier (except for $R_E$ feedback) holds the emitter at signal ground, while the common collector circuit does the same for the collector.
We keep the same bias (1/3, 1/3, 1/3) that we established for the gain of 10 common emitter amplifier.

All that we need to do is pick the capacitor values and calculate the circuit gain.
**Mid-band Small Signal Analysis**

**Input Impedance**

\[
\begin{align*}
\nu_{Re} &= r_e \parallel R_E i_s \\
Z_{in} &= \frac{\nu_{Re}}{i_s} = r_e \parallel R_E \approx r_e = \frac{V_T}{I_C} \\
Z_{out} &= \frac{\nu_o}{i_c} \approx R_C \parallel r_o
\end{align*}
\]

**Current Gain**

\[
A_i = \frac{i_c}{i_e} = \alpha \approx 1
\]

**Voltage Gain**

\[
\begin{align*}
\nu_s &= -i_e R_S - r_e \parallel R_E i_e \\
\nu_o &= -R_C i_c = -\alpha R_C i_e = \frac{1}{\alpha} \frac{R_C}{R_S + r_e \parallel R_E} \nu_s \\
A_v &= \frac{\nu_o}{\nu_s} \approx \frac{1}{\alpha} \frac{R_C}{R_S + r_e}
\end{align*}
\]

Note: \( R_B \) is shorted by \( C_b = \infty \)

\( C_{in} = \infty \)

\( Z_{in} = \infty \)

\( i_s = -i_e \)

\( R_E \gg r_e \)
Common Base Small Signal Analysis - $C_{in}$

NOTE: $C_b$ is short ckt

Determine $C_{in}$: (let $C_b = \infty$)

$$v_{Re} = \frac{R_E || r_e}{R_E || r_e + R_s + \frac{1}{j2\pi f C_{in}}} v_s$$

ideally

$$v_{Re} = \frac{R_E || r_e}{R_E || r_e + R_s} v_s \approx \frac{r_e}{r_e + R_s} v_s$$

for $f \geq f_{min}$

$$\frac{1}{2\pi f_{min} C_{in}} \ll R_s + r_e \Rightarrow \frac{1}{2\pi f_{min} C_{in}} = \frac{R_s + R_E}{10} \Rightarrow C_{in} = \frac{10}{2\pi f_{min} (R_s + r_e)}$$
Determine $C_{\text{in}}$ cont.

A suitable value for $C_{\text{in}}$ for a $20 \text{ Hz} f_{\text{min}}$ with $r_e = 25 \ \Omega$ and $R_s = 50 \ \Omega$:

$$2\pi f_{\text{min}} C_{\text{in}} (R_s + r_e) \gg 1 \Rightarrow C_{\text{in}} \geq \frac{10}{2\pi f_{\text{min}} (R_s + r_e)} = \frac{10}{2\pi 20 \cdot 75} \ F$$

$$C_{\text{in}} = \frac{10}{125.6 \cdot 75} \approx 1060 \ \mu F$$

Too Large to be Practical!

Choose $C_{\text{in}} = 220 \ \mu F$ (largest standard value in Detkin Lab)

$$X_{C_{\text{in}}} = \frac{1}{2\pi f_{\text{min}} C_{\text{in}}} \approx 36 \ \Omega$$
Small-signal Analysis - $C_b$

Determine $C_b$: (let $C_{in} = \infty$)

$$v_{Re} = \frac{R_E \parallel (r_e + \frac{1}{j 2\pi f C_b (\beta+1)})}{R_E \parallel (r_e + \frac{1}{j 2\pi f C_b (\beta+1)}) + R_S} \cdot v_s$$

ideally

$$v_{Re} = \frac{R_E \parallel r_e}{R_E \parallel r_e + R_S} \cdot v_s \quad \text{for } f \geq f_{min}$$

$$\frac{1}{2\pi f_{min} C_b (\beta+1)} \ll r_e \Rightarrow \frac{1}{2\pi f_{min} C_b (\beta+1)} = \frac{r_e}{10} \Rightarrow C_b = \frac{10}{2\pi f_{min} r_e (\beta+1)}$$

Ignore $R_B$
Choose (conservatively):

\[ C_b = \frac{10}{2\pi f_{\text{min}} ((\beta + 1) r_e)} \ F \]

for \( f_{\text{min}} = 20 \ Hz \)

i.e.

\[ C_b = \frac{10}{2\pi 20((100)(25))} = 31.8 \mu F \]
Multisim Simulation

\[ A_v = \frac{v_o}{v_s} = \frac{1}{\alpha \frac{R_C}{R_S + r_e}} \approx \frac{R_C}{R_S + r_e} = \frac{4700}{50 + 25} = 62.7 \]
Multisim Frequency Response

19.3 Hz response: \( A_{v(sim)} = 61.8 \)

1 kHz Response: \( A_{v(sim)} = 63.3 > A_{v(\text{theory})} = 62.7 \)

\( \delta < 1\% \)