ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Day 28: November 15, 2013
Memory Periphery

Today
Memory Periphery
- Sensing
- Driving
- Decode

Sensing

SRAM Memory bit

Simulation $W_{\text{access}} = 20$

Sense Small Swings
- What do we have to worry about?
Sense Small Swings

- Variation
  - Shift where inverter trip point is
- Systematic shifts that affect both lines
  - "Common mode" noise
  - E.g.
    - Noise
    - Voltage drop

Two Sense Amps
1. Clocked / Regenerative Feedback
2. Not clocked / Differential Sense Amp
- Goal: amplify small signal difference
  - reject common mode noise

Differential Sense Amp
- Goal:
  - Reject common shift

Voltage Controlled
- Consider Vctrl as an analog input between 0 and Vdd-Vth
  - What does this do?
  - How does the voltage on Vctrl control operation?

Warmup
- What does this do?
- How do we size transistor?

DC Transfer
- DC transfer plots for different Vctrl values
Idea

- Control Resistance to control trip point
- Set trip point based on second line

Q: how set Vctrl?

What does this do?

- Output when:
  - In=Gnd?
  - In=Vdd?
  - Transfer curve?

“Inverter”

- Input high
  - Ratioed like grounded P
- Input low
  - Pulls itself up
  - Until V_{dd}-V_{TP}

DC Transfer Function

Differential Sense Amp
Diffamp Transfer Function

- \( \text{in} = \overline{\text{in}}, \) looks like "inverter"
- Deliberately low gain in mid region
- Ideal might be flat?

Differential Sense Amp

- "Inverter" output controls PMOS for second inverter
- Sets PMOS operating point
  - Voltage controlled resistance
  - Sets trip point

Differential Sense Amp

- What happens when \( \overline{\text{in}} > \text{in} ? \)
- \( \overline{\text{in}} < \text{in}? \)

Differential Sense Amp

- View:
  - Current mirror
  - Biases where inverter operating

Differential Sense Amp

- View:
  - adjusting the pullup load resistance
  - Changing the trip point for "inverter"

DC Transfer /in with in=0.5V
DC Transfer Various in

- What is trip point when:
  - In=0.3V?
  - In=0.4V?
  - In=0.5V?
  - In=0.6V?
  - In=0.7V?

After Inverter

Differential Sense Amp

- Does need to be sized
- There is a ratioed logic effect here

Ramp 50mV Offset

Closeup 50mV Offset
Regenerative Feedback

Connect to Column
- Equalize lines during precharge

Singled-Ended Read

5T SRAM

Single Ended
- Given same problems
  - How sense small swing on single-ended case?

Single Ended
- Need reference to compare against
- Want to look just like bit line
- Equalize with bit line
Split Bit Line

- Split bit-line in half
- Precharge/equalize both
- Word in only one half
  - Only it switches
- Amplify difference

Open Bit Line Architecture

- For 1T DRAM
- Add dummy cells
- Charge dummy cells to \( V_{dd}/2 \)
- "read" dummy in reference half

Memory Bank

Row Select

- Logically a big AND
  - May include an enable for timing in synchronous

Row Select

How many transistors (per address bit)?
How tall is a row?

- Side length for cell of size:
  - $1000 \lambda^2$
  - $600 \lambda^2$
  - $100 \lambda^2$

Row Select

- How can we do better?
  - Area
  - Delay
  - Match to pitch of memory row

Row Select

- Compute inversions outside array
  - Just AND appropriate line (bit or /bit)

Row Select

- Share common terms
- Multi-level decode

Row Select

- Same number of lines
- Half as many AND inputs inside the row
Row Select: Precharge NAND

Row Select: Precharge NOR

Bus Drivers

Memory Bank

Tristate Driver

Tri-State Drivers
Idea

- Minimize area of repeated cell
- Compensate with periphery
  - Amplification (restoration)
- Match periphery pitch to cell row/column
  - Decode
  - Sensing
  - Writer Drivers

Admin

- Monday: in Detkin Lab
  - Read lab2 assignment before coming to class
- Tuesday: Proj2 Milestone due
- Wednesday: Lecture