ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Day 14: October 1, 2014 Layout and Area

Midterm 1
Average: 79.7 (of 85)
Std. Dev.: 4.4

Problem 4
• Failure – my fault
  – Should be: \( \min(\max(3(V_a-V_b),0),1) \)
• Failed to provide good diagnosis of restoration understanding
  – Noisy measurement
• Result
  – Exam not provide very high precision assessment of students
    • Cannot distinguish A from B students

Exam Successes (not fail)
• Does provide enough information to diagnose anyone in big trouble and should drop
  – separate the DF from AB
• Diagnose a few R C items
  – Need that down cold \( \Rightarrow \) will use heavily
• Did focus you on understanding these items, including restoration

Today
• Layout
  – Transistors
  – Gates
• Design rules
• Standard cells

Transistor

Layout
Layout

- Sizing & positioning of transistors
- Designer controls W, L
- $t_{ox}$ fixed for process
  - Sometimes thick/thin oxide "flavors"

NMOS Geometry

Top view

Perspective view

Color scheme
- Red: gate
- Green: source and drain areas (n type diffusion)

NMOS vs PMOS

- NMOS built on p substrate
- PMOS built on n substrate
  - Needs an N-well

Body Contact

"Fourth terminal"
- Needed to set voltage around device
  - PMOS: $V_b = V_{dd}$
  - NMOS: $V_b = GND$
- At right: PMOS (orange) with body contact (dark green)
Body Contact

- Needed to set voltage around device
  - PMOS: $V_b = V_{dd}$
  - NMOS: $V_b = \text{GND}$
- What happens if NMOS body contact is $V_{dd}$?

- Always to same supply as the transistor might be connected in CMOS

Interconnect

- Connect transistors
  - Different layers of metal
    - "Contact" - metal to transistor
    - "Via" - metal to metal
Masks

- Define areas want to see in layer
  - Think of “stencil” for material deposition
- Use photoresist (PR) to form the “stencil”
  - Expose PR through mask
  - PR dissolves in exposed area
  - Material is deposited
    - Only “sticks” in area w/ dissolved PR

Masking Process

- Goal: draw a shape on the substrate
  - Simplest example: draw a rectangle

Masking Process

- First: deposit photoresist

Masking Process

- Expose through mask
  - UV light

Masking Process

- Remove mask and develop PR
  - Exposed area dissolves
  - This is “positive photoresist”
Masking Process

- Deposit metal through PR window
  - Then dissolve remaining PR
- Why not just use mask?
  - Masks are expensive
  - Shine light through mask to etch PR
  - Can reuse mask

Reverse Engineer Inverter Layout

Layout Revisited

- How to “decode” circuit from layout?

Reverse Engineer Inverter Layout

Power (Vdd)

- Where is PMOS transistor?
- NMOS?

Layout to Circuit

- 1. Identify transistors
Inverter Layout

• Where is Input?

Layout to Circuit

• 2. Add wires

Inverter Layout

• Where is Output?

Layout to Circuit

• 2. Add wires

Inverter Layout

• What is structure at top and bottom?

Layout to Circuit

• 2. Add wires
Layout to Circuit

• 2. Add wires

Design Rules

• Why not adjacent transistors?
  – Plenty of empty space
  – If area is money, pack in as much as possible
• Recall: processing imprecise
  – Margin of error for process variation

Design Rules

• Contract between process engineer & designer
  – Minimum width/spacing
  – Can be (often are) process specific
• Lambda rules: scalable design rules
  – In terms of $\lambda = 0.5 L_{\text{min}} (L_{\text{drawn}})$
  – Can migrate designs from similar process
  – Limited scope: 22nm process $\neq 1 \mu m$

Design Rules: Some Examples

Layout #2 (practice)

• How many transistors?
  – PMOS?
  – NMOS?
• How connected?
  – PMOS, NMOS?
• Inputs connected?
• Outputs?
• What is it?
Standard Cells

- Lay out gates so that heights match
  - Rows of adjacent cells
  - Standardized sizes
- Motivation: automated place and route
  - EDA tools convert HDL to layout

Standard Cell Area

- All cells uniform height
- Width of channel determined by routing

Identify the full custom and standard cell regions on 386DX die
http://microscope.fsu.edu/chipshots/intel/386dxmlarge.html

Big Idea

- Layouts are physical realization of circuit
  - Geometry tradeoff
    - Can decrease spacing at the cost of yield
    - Design rules
  - Can go from circuit to layout or layout to circuit by inspection

Identify the full custom and standard cell regions on 386DX die
http://microscope.fsu.edu/chipshots/intel/386dxmlarge.html
Admin

• HW5 out
  – Due Tuesday
  – (Thursday next week is Fall Break)
• Here on Friday