ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Day 1: August 30, 2017
Introduction and Overview
Where I come from

- Analog VLSI Circuit Design (analog design)
- Convex Optimization (system design)
  - System Hierarchical Optimization
- Biomedical Electronics
- Biometric Data Acquisition (signal processing)
  - Compressive Sampling
- ADC Design (mixed signal)
- Low Energy Circuits (digital design)
  - Adiabatic Charging
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CIRCUITS, CIRCUITS, CIRCUITS
MicroImplant: An Electronic Platform for Minimally Invasive Sensory Monitors

Signal Sensing and Processing

Energy Management

Data Collection and Transmission

Bare die
Ultra-capacitor
Bio-friendly package

Power
Data
Reader

Impedance Matching
Modulator (ASK)

Digital Control
Lecture Outline

- Course Overview
  - Motivating questions
  - What this course is about
  - Learning objectives
  - What you need to know

- Course Details
  - Course structure
  - Course policies
  - Course content
VLSI Design

Oracle SPARC M7 Processor

300 mm (12 in.)

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Motivating Questions

- How fast can my computer run?
  - What limits this speed?
  - What can I do to make it run faster?
- How can I extend the battery life on my gadget?
  - How much energy must my computation take?
- How small can I make a memory?
  - Why does DRAM need to be refreshed?
    - What is DRAM? SRAM? EEPROM?
Motivating Questions (con’t)

- How many bits/second can I send over a communication link?
  - What limits this?
  - How do I maximize?

- How does technology scaling change these answers?
  - What can I rely on technology to deliver?
Sample Problems

What does this circuit do? How fast does it operate?
Sample Problems (con’t)

- What does this circuit do? How are A, B, C related?
Sample Problems (con’t)

- What’s wrong here? How do we fix it?
Limits?

- Consider a 22nm technology
- Typical gate with $W=3$, 2-input NOR
- Use chip in cell phone
- What prevents us from running 1 billion transistor chip at 10GHz?
Impact of Voltage?

- If have a chip running at 1GHz with a 1V power supply dissipating 1W.
- What happens to performance if we cut the power supply to 500mV?
  - Speed?
  - Power?
Course Deconstruction

- Circuit-Level Modeling, Design, and Optimization for Digital Systems

  - Look inside the digital gates (transistors, resistance, capacitance, inductance...)
  - Abstract and predict
  - Create
  - Make efficient (fast, low energy, small)
  - Compute, store, transmit binary values (0s, 1s)
What this course is about

- Modeling and abstraction
  - Predict circuit behavior
  - Well enough to know your design will work
  - …with given performance spec(ification)s
    - Performance, speed, energy, …. 
  - Well enough to reason about design and optimization
    - What knob can I turn to make faster?
    - How much faster can I expect to make it?
What this course is about (con’t)

- Modeling and abstraction
  - Back-of-the-envelope
    - Simple enough to reason about
      - …without a calculator…
  - Sensitive to phenomenology
    - Able to think through the details
  - With computer assistance
    - …understanding even that is a simplified approximation
We are here.

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Learning Objectives

- Disciplines for robust digital logic and signaling
  - (e.g., regeneration, clocking)
- Where delay, energy, area, and noise arise in gates, memory, and interconnect
- Modeling these physical effects
  - back-of-the-envelope design
    - (e.g. RC and Elmore delay)
  - detailed simulation (e.g. SPICE)
Learning Objectives (con’t)

- Tradeoffs in performance specs
  - Among delay, energy, area, noise
- How to design and optimize
  - logic, memory, and interconnect structures
  - at the gate, transistor, and wire level
- How technology scales
  - impact on digital circuits and computer systems
What you need to know

- See “knowledge roundup” topics page linked from course page
- ESE 150 (CIS 240*)
  - Gates, Boolean logic, DeMorgan’s, gate optimization
- ESE 215
  - RLC circuit analysis
- Diagnostic Quiz on Canvas
  - Not graded, weighted as a homework assignment
  - Complete by Monday midnight (Labor Day – no class)
Review Session Poll

- Review material from ESE 150 and ESE 215?
  - Poll posted on Piazza
Course Structure

- **Course Staff (complete info on course website)**
- **Instructor: Tania Khanna**
  - Office hours – Wednesday 1-3:00 pm or by appointment
  - Email: taniak@seas.upenn.edu
  - Best way to reach me
- **TAs: Martin Deng**
  - Office hours – MT 6:30-8:30pm
Course Structure

- MWF 12-1pm Lecture
  - Will start 5 minutes late and end 5 minutes early
- Readings from textbook
- 4 lecture periods → Detkin Lab
- Find entire schedule on course webpage

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<tr>
<th>Week</th>
<th>Lect.</th>
<th>Date</th>
<th>Lecture</th>
<th>Slides</th>
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<td>1</td>
<td>8/30</td>
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<td>Intro/Overview</td>
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<td>1 through 1.2; review course webpage completely</td>
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<td>Transistor Introduction (basics) and Gates from Transistors</td>
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<td>Review ESE215; 6.2 through static properties in 6.2.1</td>
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<td>9/4</td>
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<td>9/6</td>
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<td>Lab (Detkin): Gate from Discrete Transistors</td>
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<td>3</td>
<td>9/11</td>
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<td>Regenerative Property</td>
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<td>3</td>
<td>9/13</td>
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<td>Delay and RC Response</td>
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<td>4</td>
<td>9/18</td>
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Course Structure - Lectures

- Statistically speaking, you will do better if you come to lecture

- Better if interactive, **everyone** engaged
  - Asking and answering questions
  - Actively thinking about material

- Two things
  - Preclass exercises
    - Work during ~5 minutes before lecture starts
    - Primes you for topic of the day
  - Ask questions of individuals
Course Structure - Textbook

- Textbook
  - *Digital Integrated Circuits, A Design Perspective*, Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, 2\textsuperscript{nd} edition
    - Great reference text with great detail
    - REALLY!! useful for projects
Course Structure - SPICE

- Simulation Program with Integrated Circuit Emphasis
  - Industry standard analog circuit simulator
  - Non-linear, differential equation solver specialized for circuits
- Integrated circuits – simply impractical to build to debug
  - Must simulate to optimize/validate design
Course Structure - Assignments/Exams

- **Homework** – week long (8 total) [25%]
  - Due Wednesdays (mostly) at midnight
  - Submit in Canvas

- **Projects** – 2-3 weeks long (2 total) [30%]
  - Design oriented
  - On two main topics
    - Computation
    - Storage

- **Two midterms** [20%]
  - 2 hours in the evening

- **Final exam** [25%]
Course Structure - Websites

- Website (http://www.seas.upenn.edu/~ese370/)
  - Course calendar is used for all handouts (lectures slides, assignments, and readings)
  - Canvas used for assignment submission and grades
  - Piazza used for announcements and discussions

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Course Structure - Admin

- Use course calendar
  - Lectures online before class
    - Will post by 9am day of class
    - Reserve the right to change them
  - Homeworks linked
    - Homework 1 out now
    - Diagnostic quiz available now
  - Reading for whole term specified

- Take notes!
  - Especially on the examples we do in class
  - Slides have a lot of questions – not a lot of answers
Course Policies

See web page for full details

- Turn homework in on Canvas
  - Anything handwritten/drawn must be clearly legible
  - Submit CAD generated figures, graphs, results when specified
  - **NO LATE HOMEWORKS!**

- Individual work (HW & Project*)
  - CAD drawings, simulations, analysis, writeups
  - May discuss strategies, but acknowledge help
Course Content

- Logic (Computation) [8 weeks]
  - Combinational logic
  - Sequential logic
- Memory/Storage [2 weeks]
- Communication/Interconnect [3 weeks]
Course Content (con’t)

- Logic
  - Transistors → Gates
  - In Lab: build gate, measure delay
  - Regeneration
  - Delay
  - Area (no layout → ESE570)
  - Energy
  - Synchronous (flip-flops, clocking, dynamic)
  - Project 1: fast ripple-carry adder
Course Content (con’t)

- Memory/Storage
  - No Lab component
  - RAM Organization
  - Driving Large Capacitances
  - Signal amplification/regeneration
  - **Project 2:** design a SRAM Register File
Communication/Interconnect

- In Lab
  - Measure inductive ground bounce, crosstalk
  - Experiment with transmissions lines, termination

- Noise
  - Crosstalk
  - Inductive
  - Ionizing particles, shot

- Transmission Lines
Advice

- Course is hard (but valuable)
- Should be thinking about this material every day
- Go to office hours
- MUST READ TEXT!
- Learning is spread over all components
  - Lecture, reading, homeworks, projects, exams
- Must be able to get quantitative answers to get an A
  (maybe even for B)
Wrap up

- Admin
  - Find web, get text, assigned reading…
  - http://www.seas.upenn.edu/~ese370
  - https://piazza.com/upenn/fall2017/ese370/
  - https://canvas.upenn.edu/courses/

- Big Ideas/takeaway
  - Model (a.k.a. analysis and simulation) to enable real-life design

- Diagnostic Quiz in Canvas
  - Review as needed

- Remaining Questions?