Thus far...

- Understand how to model transistor behavior
- Given that we know its parameters
  - $V_{dd}$, $V_{dd}$, $C_{dss}$, $W$, $L$, $\mu$ ...

But...

- We don’t know its parameters (perfectly)
  - Fabrication parameters have nominal values and error range
  - Impact on $I_D$?
- Identically drawn devices differ because of fabrication techniques (e.g. process mismatch)
- Parameters change with environment (e.g. Temperature)
- Parameters change with time (aging)
Today

- Sources of Variation
  - Fabrication
  - Operation
  - Aging
- Designing to Account for Variation
  - Margin
  - Corners
  - Binning

Fabrication

Variation Types

- Many reasons why variation occurs and shows up in different ways
- Scales of variation
  - Wafer-to-wafer, die-to-die, transistor-to-transistor
- Correlations of variation
  - Systematic, spatial, random (uncorrelated)

Basic Fabrication: Two Steps

- (1) Transfer an image of the design to the wafer
- (2) Using that image (mask) as a guide, create the desired layers on silicon
  - Diffusion (add dopants to the silicon)
  - Oxide (create an insulating layer)
  - Metal (create a wire layer)

Wafer Scale: Process Shift

- Oxide thickness
- Doping level
- Layer alignment
- Growth and Etch rates and times
  - Depend on chemical concentrations
  - How precisely can we control these?
- Vary machine-to-machine, day-to-day
- Impact all transistors on wafer
Systematic Spatial Variation

- Parameters change consistently across wafer or chip based on location

- Sources
  - Chemical-Mechanical Polishing (CMP)
  - Dishing
  - Lens distortion

Random Transistor-to-Transistor

- Random dopant fluctuation
- Local oxide variation
- Line edge roughness
- Etch and growth rates
- Transistors differ from each other in random ways

Statistical Dopant Placement

Oxide Thickness and Interface roughness

[Asenov et al. TRED 2002]

Line Edge Roughness

Line Edge & Line-Width Roughness

- LER = lines of device features are not straight
- LWR = distance between lines is not uniform
- LER & LWR arise from the lithography and etching processes
- They are most pronounced in poly-gate patterning
- Effects
  - Increased $I_{on}$
  - Increased variation in $V_T$

Source: Kuhn et al.
Impact

- Changes parameters
  - $W, L, t_{OX}, V_{th}$, etc.
- Change transistor behavior
  - $W$ increase?
  - $L$ increase?
  - $t_{OX}$ increase?
  - $V_{th}$ increase?

\[
I_{DS} = V_{sat} C_{OX} W \left( V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)
\]

\[
I_{DS} = \mu C_{OX} \left( \frac{W}{L} \right) \left( V_{GS} - V_T - \frac{V_{DS}^2}{2} \right)
\]

Example: $V_{th}$

- Many physical effects impact $V_{th}$
  - Doping, dimensions, roughness
- Behavior highly dependent on $V_{th}$

\[
I_{DS} = V_{sat} C_{OX} W \left( V_{GS} - V_T - \frac{V_{DSAT}}{2} \right)
\]

\[
I_{DS} = \mu C_{OX} \left( \frac{W}{L} \right) e^{\left( \frac{V_{GS} - V_T}{V_{TH}} \right)}
\]

Impact of $V_{th}$ Variation?

- Higher $V_{th}$?
  - Not drive as strongly
  - $I_{DS} \propto (V_{gs} - V_{th})$
  - Performance?

Impact Performance

- $V_{th} \rightarrow I_{th} \rightarrow$ Delay ($R_{on} \ast C_{load}$)

V$_{th}$ Variability @ 65nm

[Bernstein et al, IBM JRD 2006]
Impact Performance

- $V_{th} \rightarrow I_{th} \rightarrow$ Delay ($R_{on} \times C_{load}$)

Impact of $V_{th}$ Variation?

- Lower $V_{th}$?
  - Not turn off as well $\Rightarrow$ leaks more

\[ I_{DS} = I_{S} \left( \frac{W}{L} \right) \left( \frac{V_{GS} - V_{TH}}{V_{TH}/q} \right) \]

Operation

Temperature

- Voltage

Temperature Changes

- Different ambient environments
  - January in Maine
  - July in Philly
  - Air conditioned machine room
- Self heat from activity of chip
- Quality of heat sink (attachment thereof)
  - E.g. cooling fan

Thermal Profile for Processor

How does temperature impact on-current?

- High temperature
  - More free thermal energy
    - Easier to conduct
    - Lowers $V_{th}$
  - Increase rate of collision
    - Lower saturation velocity
    - Lower saturation voltage
    - Lower peak $I_{th} \Rightarrow$ slower down
- One reason don't want chips to run hot
How does temp impact leakage current?

- High temperature lowers $V_{th}$

$$I_{ds} = I_d \left( \frac{W}{L} \right) \left( \frac{V_{GS} - V_T}{N^2/2} \right)$$

Voltage

- Power supply isn’t perfect
- Differs from design to design
  - Board to board?
  - How precise is regulator?
- IR-drop in distribution
- Bounce with current spikes

Aging

Hot Carrier Injection

- Trap electrons in oxide
  - Increases $V_{th}$
NBTI

- Negative Bias Temperature Instability
  - Interface traps, Holes
- Long-term negative gate-source voltage
  - Affects PFET most
- Increase $V_{th}$
- Temperature dependent

$\Delta V(t) \propto \exp(-\beta V_G) \exp\left(-\frac{E_A}{kT}t\right)$

[Stott, FPGA2010]

Coping with Variation

- See a range of parameters
  - $I_L$: $I_{min} \sim I_{min}$
  - $V_{th}$: $V_{th, min} \sim V_{th, max}$

Variation

- Margin for expected variation
  - Must assume $V_{th}$ can be any value in range
  - Speed $\Rightarrow$ assume $V_{th}$ slowest value

Variation

- $I_{on,min} = I_{on}(V_{th,max})$
  - $I_{on} \sim (V_G - V_{th})$

Impact of $V_{th}$ Variation

- Higher $V_{th}$
  - Not drive as strongly
  - $I_{d,v,sat} \propto (V_{GS} - V_{th})$

- Lower $V_{th}$
  - Not turn off as well $\Rightarrow$ leaks more

$\frac{I_{ds}}{I_L} = \frac{W}{L} \left( \frac{I_{on, min} - I_{off}}{I_{on, max} - I_{off}} \right)$

Measured Accelerated Aging
(Cyclone III, 65nm FPGA)
Impact

- Given
  - $V_{th,nom} = 250\, \text{mV}$
  - Standard deviation: $\sigma = 25\, \text{mV}$
- Probability of 100 transistor circuit in range when each has 96% prob.?
- …when each has 99.8% probability?

Variation

- See a range of parameters
  - L: $L_{\text{min}} - L_{\text{max}}$
  - $V_{th}$: $V_{th,\text{min}} - V_{th,\text{max}}$
- Validate design at extremes
  - Work for both $V_{th,\text{min}}$ and $V_{th,\text{max}}$?
  - Design for worst-case scenario

Margining

- Also margin for
  - Temperature
  - Voltage
  - Aging: end-of-life

Process Corners

- Many effects independent
- Many parameters
- With $N$ parameters,
  - Look only at extreme ends (low, high)
  - How many cases?
- Try to identify the {worst,best} set of parameters
  - Slow corner of design space, fast corner
- Use corners to bracket behavior

Simple Corner Example

- $350\, \text{mV}$
- $150\, \text{mV}$
Process Corners

- Many effects independent
- Many parameters
- Try to identify the \{worst, best\} set of parameters
  - E.g., Lump together things that make slow
  - Vth, Vpp, temperature, Voltage
  - Try to reduce number of unique corners
- Slow corner of design space
- Use corners to bracket behavior

Worst-case Corner Model

- corners for analog applications
  - For modeling worst-case speed
    - Slow NMOS and slow PMOS(SS) corner
  - For modeling worst-case power
    - Fast NMOS and fast PMOS(FP) corner
- corners for digital applications
  - For modeling worst-case 1
    - Fast NMOS and slow PMOS(FS) corner
  - For modeling worst-case 0
    - Slow NMOS and fast PMOS(SF) corner

Worst-case Corner Model

- Advantages
  - Worst case corner models give designers the capability to simulate the pass/fail results of a typical design and are usually pessimistic.
- Disadvantages
  - The fixed-corner method is too wide
  - Some valid designs can not be accepted in worst-case corner model
  - The correlations between the device parameters are ignored

Statistical Corner Model

- For more realistic modeling for process variability than worst-case corner model.
  - Using data from different dies, wafers, and wafer lots collected over a long enough period of time to represents realistic process variability of the target technology
- The difference between statistical corner model and worst-case corner-model
  - Statistical corner model use the realistic PDF of the corresponding model parameter of its typical model
  - PDF is obtained from the distribution of a large set of production data
  - Statistical models can pass a valid design, which were rejected in worst-corner model

Range of Behavior

- Still get range of performances
- Any way to exploit the fact some are faster?

Speed Binning

- Probability Distribution

```
Sell
Premium
Sell
nominal
Sell
cheap
Discard
```
Big Idea

- Parameters Approximate
- Differ
  - Chip-to-chip, transistor-to-transistor, over time
- Robust design accommodates
  - Tolerance and Margins
  - Doesn’t depend on precise behavior

Midterm 1 - Content

- Lec 1 - 9
  - Identify CMOS/non-CMOS
  - Identify CMOS function
  - Any logic function \( \rightarrow \) CMOS gate
  - Noise Margins / Restoration
  - Circuit first order switching rise/fall times
    - Output equivalent resistance
    - Load capacitance
  - MOS Model
  - Identify transistor region of operation
  - Analysis with transistor IV models
  - MOS capacitance models

Midterm 1 - Logistics

- M 10/1: 7-9pm in Moore 216 (no lecture, office hours)
  - Individual closed-book exam
  - Calculators allowed, no smart phone calculators
  - If caught cheating, all parties will get a zero and be reported to Office of Student Conduct
- Old exams and solutions posted
  - Focus on 2015-2018 exams
  - 2010 disclaimer: only 1 midterm so covered more material
- Angelina review session: Sunday 1-3pm location TBD
  - Check Piazza for location updates
  - Selection of old exam questions will be worked out