ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lee 29: November 13, 2019
RAM Core Part 2

Today
- 5T SRAM
- Multiported SRAM
- DRAM
- Memory Periphery
  - Sensing (time permitting)

5T SRAM

Charge Sharing (Preclass 1)

Initially
- A @ 1V
- B @ 0V
- \( Q_A = 1V \times C_1 = C_1 \)

Close switch
- \( Q_{\text{int}} = V_{\text{final}} \times (C_1 + C_0) \)

Charge conservation
- \( Q_A = Q_{\text{int}} \)
- \( C_1 = V_{\text{final}} \times (C_1 + C_0) \)

\[ V_{\text{final}} = \frac{C_1}{C_1 + C_0} \]

Consider (preclass 2)

- Read: What happens to voltage at A when WL turns from 0 to 1?
  - Assume \( W_{\text{access}} \) large
  - \( W_{\text{access}} \gg W_{\text{pull}} = 1 \)
  - BL initially 0

Voltage After enable Word Line

- \( Q_{\text{bl}} = 0 \)
- \( Q_A = (1V) \times (2C_0 + W_{\text{access}} C_0) \)
Voltage After enable Word Line

- $Q_{BL} = 0$
- $Q_A = (1V)(\gamma 2C_0 + \gamma W_{access} C_0)$
- $100fF = C_{BL} >> C_A = (\gamma (2 + W_{access}) C_0)$
- After enable $W_{access}$ ($W_{access}$ large)
  - Total charge $Q_{BL} + Q_A$ unchanged
  - Charge conservation
  - Distributed over larger capacitance $\approx C_{BL}$
  - $V_A \approx V_{BL} \approx \frac{C_A}{C_{BL}}$

Consider (5T SRAM)

- What happens to voltage at A when WL turns from 0 to 1?
  - Assume $W_{access}$ large
  - A initially 1
  - BL initially 0

Simulation: $W_{access} = 100$

Simulation $W_{access} = 20$

Simulation $W_{access} = 4$
Charge Sharing

- **Conclude**: charge sharing can lead to read upset
  - Charge redistribution/sharing adequate to flip state of bit

Charge to middle Voltage

- Pre-charge bitlines to $V_{dd}/2$ before begin read operation
- Now charge sharing doesn’t swing to opposite side of midpoint

Compare

- Both $W_{access} = 20$; vary BL precharge voltage

Multiple Ports

- We have considered single-ported SRAM
  - One read or one write on each cycle
- Multiple SRAM are needed for register files
- Examples:
  - Pipelined ALU register file:
    - add r1,r2,r3
    - sub r1,r2,r3
    - Requires two reads and one write
Dual-Ported SRAM

- Simple dual-ported SRAM
  - Two independent single-ended reads
  - Or one differential write

Multi-Ported SRAM

- Adding more access transistors hurts read stability
- Multiported SRAM isolates reads from state node
- Single-ended bitlines save area

Register File Cell

- Single-ended Read/Dual-ended Write

DRAM

- Smaller than SRAM
- Require data refresh to compensate for leakage
Transistor DRAM Cell
- Cell is inverting on read operation

Transistor DRAM Cell
- Cell is inverting on read operation

Transistor DRAM Cell
- Cell is inverting on read operation

1-Transistor DRAM Cell
- Cell is inverting on read operation

3-Transistor DRAM Cell
- No constraints on device ratios
- Reads are non-destructive
- Data stored has a Vn drop
- When storing a 1, value at X = VDD - Vn

Value stored at node X when writing a "1" = VDD

Voltage swing is small; typically around 250 mV.

When storing a 1, value at X = VDD - Vn

Write: Cn is charged or discharged by asserting WL and BL.
1-Transistor DRAM Cell

Write: $C_S$ is charged or discharged by asserting WL and BL.

Read: Charge redistribution takes places between bit line and storage capacitance

$$V_{\Delta V} = V_{PRE} - V_{BIT} - V_{PRE} \cdot C_{BL} / C_{BS}$$

Voltage swing is small; typically around 250 mV.

Write: $C_S$ is charged or discharged by asserting WL and BL.

Read: Charge redistribution takes places between bit line and storage capacitance

$$V_{\Delta V} = V_{PRE} - V_{BIT} - V_{PRE} \cdot C_{BL} / C_{BS}$$

Voltage swing is small; typically around 250 mV.

DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out
- DRAM memory cells are single ended in contrast to SRAM cells
- The read-out of the 1T DRAM cell is destructive; read and refresh operation are necessary for correct operation
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This loss can be circumvented by bootstrapping the word lines to a higher value than $V_{DD}$.

6T SRAM Memory bit

Simulation
Sense Small Swings

- What do we have to worry about?

Differential Sense Amp

- "se" – sense enable
  - Inputs precharged to common value
  - After read operation is initiated, bitlines begin to move in opposite directions
  - After bitlines have reached sufficient differential value, se is enabled and amplifier evaluates

Differential Sense Amp

- Does need to be sized
  - Make input nMOS devices larger than load devices pMOS
    - i.e. Larger input diffpair than load current mirror

Regenerative Feedback

- bit-lines disconnected at sensing to avoid their high capacitive load
- The regenerative feedback loop is now isolated
- When sense clock is high the values stored in bit-lines are regenerated, while the lines are disconnected, speeding up response

Idea

- Minimize area of repeated cell
  - 6T/5T SRAM
  - Multiport trade off area for function
  - 1T/3T DRAM helps but slower
- Compensate with periphery
  - Decoders
  - Bitline (column) drivers
  - Sensing/Amplification (regeneration/restoration)
- Match periphery pitch to cell row/column
  - Sensing
  - Decode

Friday ESE Seminar

- ESE Seminar: “Circuit Design at Extreme: Pushing the Limits of Silicon”
  - November 15 at 12:00 PM - 1:00 PM, Towne 337
Admin

- Friday class cancelled
  - Go to ESE Seminar instead
- Monday and Friday next week in Detkin Lab
  - Attendance and participation mandatory!
    - Can't get full HW8 points without coming to lab
- Project 2 out
  - Milestone due Wednesday 11/20
    - I will give feedback by Friday (night) 11/22
  - Final report due 12/2