Today

- 5T SRAM
- Multiported SRAM
- DRAM
- Memory Periphery
  - Sensing (time permitting)

5T SRAM

![5T SRAM Diagram]

 Charge Sharing (Preclass 1)

Initially
- A @ 1V
- B @ 0V
- \( Q_A = 1V \times C1 = C1 \)

Close switch
- \( Q_{\text{tot}} = V_{\text{final}} \times (C1 + C0) \)
- Charge conservation
  - \( Q = Q_{\text{tot}} \)
  - \( C1 = V_{\text{final}} \times (C1 + C0) \)

\[ V_{\text{final}} = \frac{C1}{C1 + C0} \]

Consider (preclass 2)

- Read: What happens to voltage at A when WL turns from 0 to 1?
  - Assume \( \text{Waccess} \) large
  - \( \text{Waccess} \gg \text{Wpu} = 1 \)
  - BL initially 0
Voltage After enable Word Line

- $Q_{BL} = 0$
- $Q_A = (1V)/(g_2C_0 + g_{W_{access}}C_0)$

Consider (5T SRAM) (preclass 3)

- What happens to voltage at A when WL turns from 0 to 1?
  - Assume $W_{access}$ large
  - $A$ initially 1
  - $BL$ initially 0

Simulation: $W_{access} = 100$

- Total charge $Q_{BL} + Q_A$ unchanged
  - Charge conservation
  - Distributed over larger capacitance $\approx C_{BL}$
  - $V_A = V_{BL} \approx C_A/C_{BL}$

Simulation $W_{access} = 20$

Simulation $W_{access} = 4$
Charge Sharing

- **Conclude:** Charge sharing can lead to read upset.
  - Charge redistribution/sharing adequate to flip state of bit

Charge to middle Voltage

- Pre-charge bitlines to $V_{dd}/2$ before begin read operation.
- Now charge sharing doesn’t swing to opposite side of midpoint.

Compare

- Both $W_{access}=20$; vary BL precharge voltage.

Simulation $W_{access}=20$ (precharge Vdd/2, reading 0)

Multiple Ports

- We have considered single-ported SRAM:
  - One read or one write on each cycle.
- Multiported SRAM are needed for register files.
- Examples:
  - Pipelined ALU register file:
    - add $r_1,r_2,r_3$
    - $R_3=R_1+R_2$.
    - Requires two reads and one write.
### Dual-Ported SRAM
- Simple dual-ported SRAM
  - Two independent single-ended reads
  - Or one differential write

### Multi-Ported SRAM
- Adding more access transistors hurts read stability
- Multiported SRAM isolates reads from state node
- Single-ended bitlines save area

### Register File Cell
- Single-ended 2-read/1-write ports (Slow-write)

### DRAM
- Smaller than SRAM
- Require data refresh to compensate for leakage
3-Transistor DRAM Cell (preclass 4)

- Cell is inverting on read operation

3-Transistor DRAM Cell

- Cell is inverting on read operation

1-Transistor DRAM Cell (preclass 5)

- Write: C_b is charged or discharged by asserting WL and BL.
1-Transistor DRAM Cell

Write: $C_S$ is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes place between bit line and storage capacitance

$$AV = V_{pp} - V_{pre} - \frac{B^2}{1+D^2}$$

Voltage swing is small; typically around 250 mV.

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DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out
- DRAM memory cells are single ended in contrast to SRAM cells
- The read-out of the 1T DRAM cell is destructive; read and refresh operation are necessary for correct operation
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This loss can be circumvented by bootstrapping the word lines to a higher value than $V_{DD}$. 

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6T SRAM Memory bit

Simulation

Precharge 6T SRAM Read
Sense Small Swings

- What do we have to worry about?

Differential Sense Amp

- "se" – sense enable
  - Inputs precharged to common value
  - After read operation is initiated, bitlines begin to move in opposite directions
  - After bitlines have reached sufficient differential value, se is enabled and amplifier evaluates

Differential Sense Amp

- Does need to be sized
- Make input nMOS devices larger than load devices pMOS
  - I.e. Larger input diffpair than load current mirror

Regenerative Feedback

- Bit-lines disconnected at sensing to avoid their high capacitive load
- The regenerative feedback loop is now isolated
- When sense clock is high the values stored in bit-lines are regenerated, while the lines are disconnected, speeding up response

Idea

- Minimize area of repeated cell
  - 6T/5T SRAM
  - Multiport trade off area for function
  - 1T/3T DRAM helps but slower
- Compensate with periphery
  - Decoders
  - Bitline (column) drivers
  - Sensing/Amplification (regeneration/restoration)
- Match periphery pitch to cell row/column
  - Sensing
  - Decoder

Admin

- Friday Lab Demo during lecture
  - Video posted after class
- Project 3 out
  - Milestone due Monday 11/23
  - I will give feedback by Wed (night) 11/25
- Final report due 12/4