ESE370: Circuit-Level Modeling, Design, and Optimization for Digital Systems

Lec 5: February 1, 2023

MOS Model and Transistor Operating Regions, Part I

Penn

You are Here: Transistor Edition

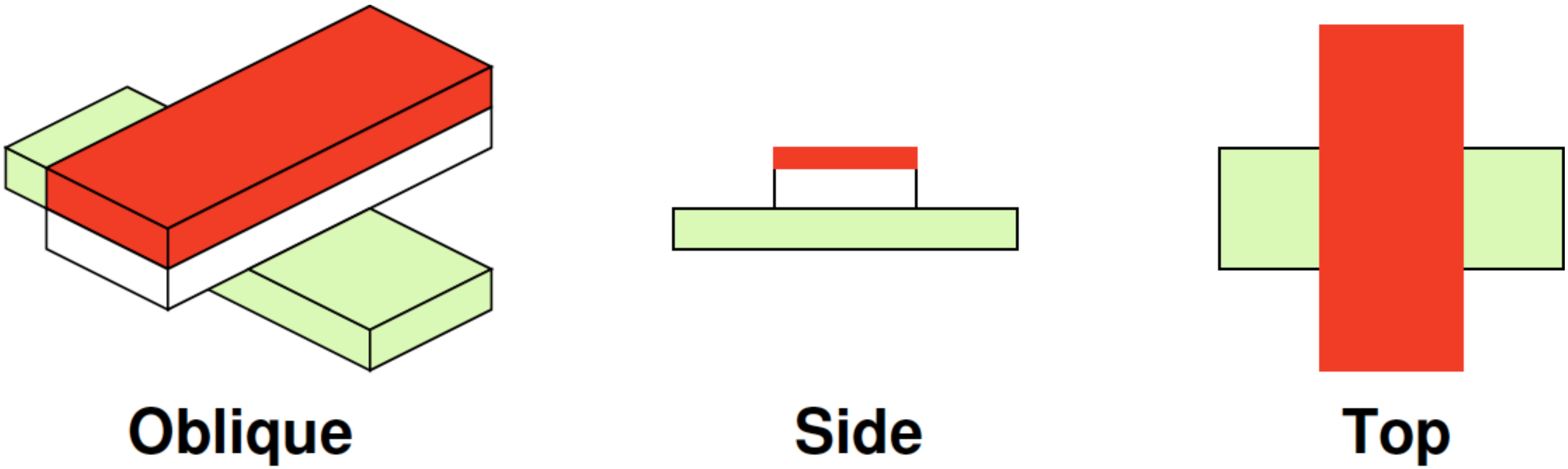
- Previously: simple models (0^{th} and 1^{st} order)
  - Comfortable with basic functions and circuits
- This lecture and the next one
  - Detailed semiconductor discussion
  - MOSFET phenomenology
- Rest of term
  - Implications of the MOS device

Today

- MOS Structure
- Basic Fabrication
- Threshold
- Operating Regions
  - Resistive
  - Saturation
  - Subthreshold
  - Velocity Saturation (next lecture)

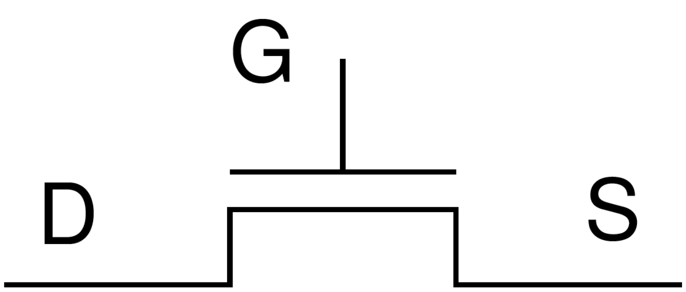
MOS

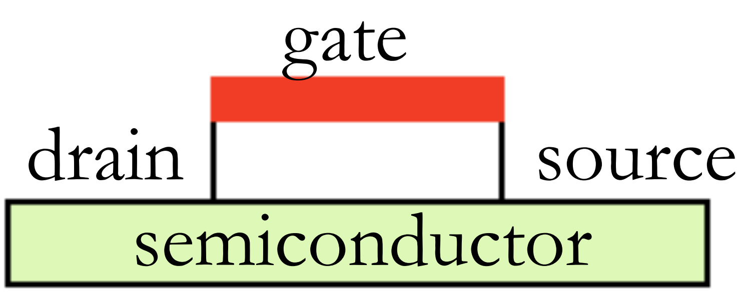
- Metal Oxide Semiconductor



MOS

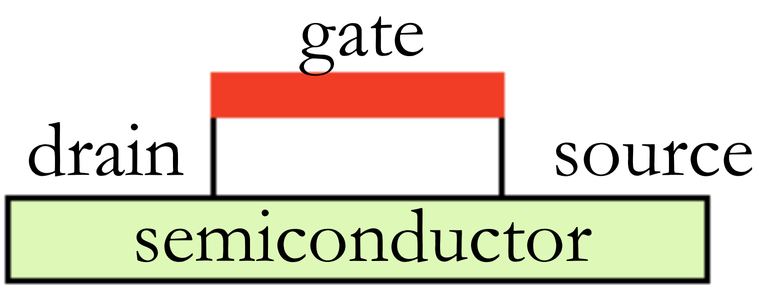
- **M**etal – gate
- **O**xide – insulator separating gate from semiconductor
  - Ideally: no conduction from gate to semiconductor
- **S**emiconductor – between source and drain
- See why gate input is capacitive?

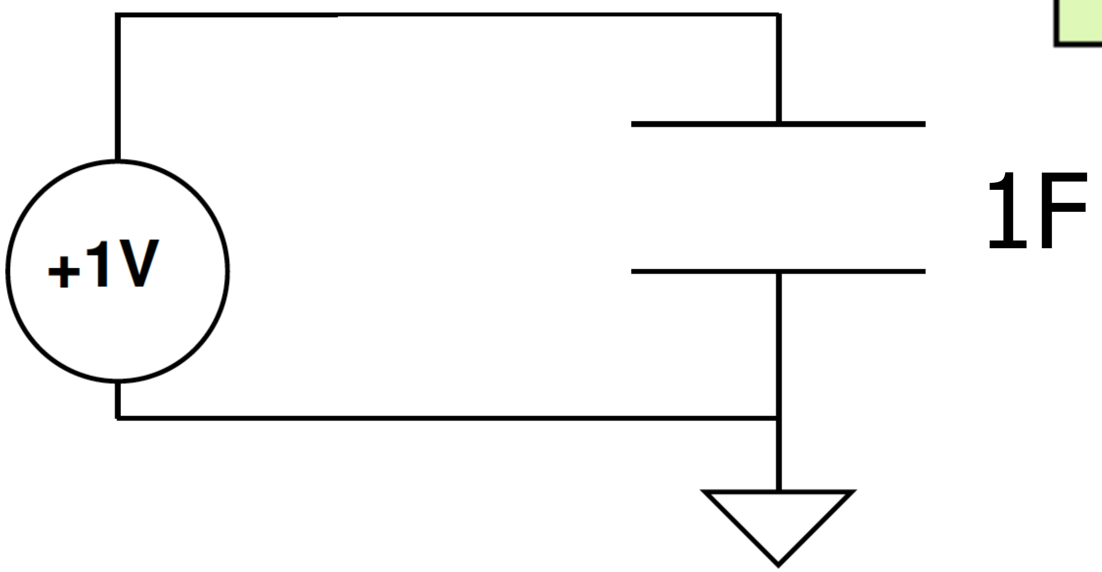




(MOS) Capacitor (preclass 1)

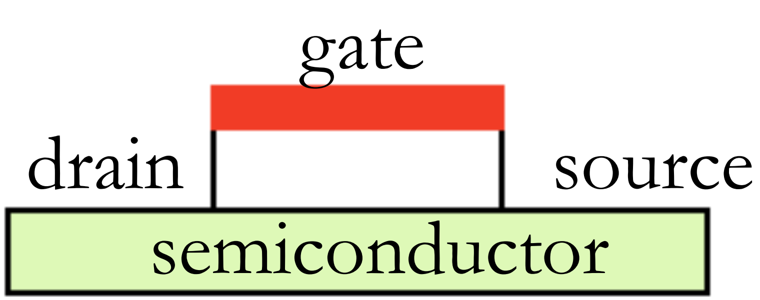
- Charge distribution and field?
- How much charge on plates?





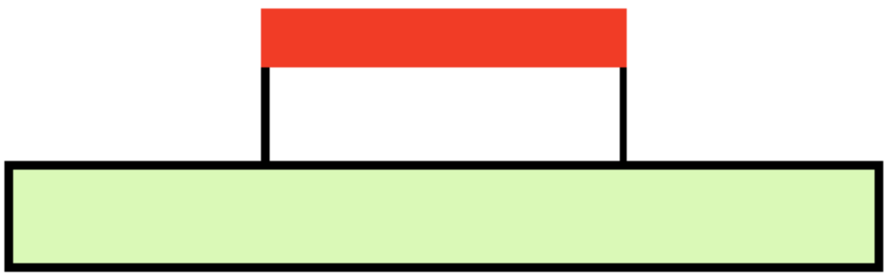
Idea

- Semiconductor – can behave as metal or insulator
- Voltage on gate induces an electrical field
- Induced field attracts (repels) charge in semiconductor to form a channel
  - Semiconductor can be switched between conducting and not conducting
  - Hence "Field-Effect" Transistor



Source/Drain Contacts

- Contacts: Conductors → metallic
  - Connect to metal wires that connect transistors

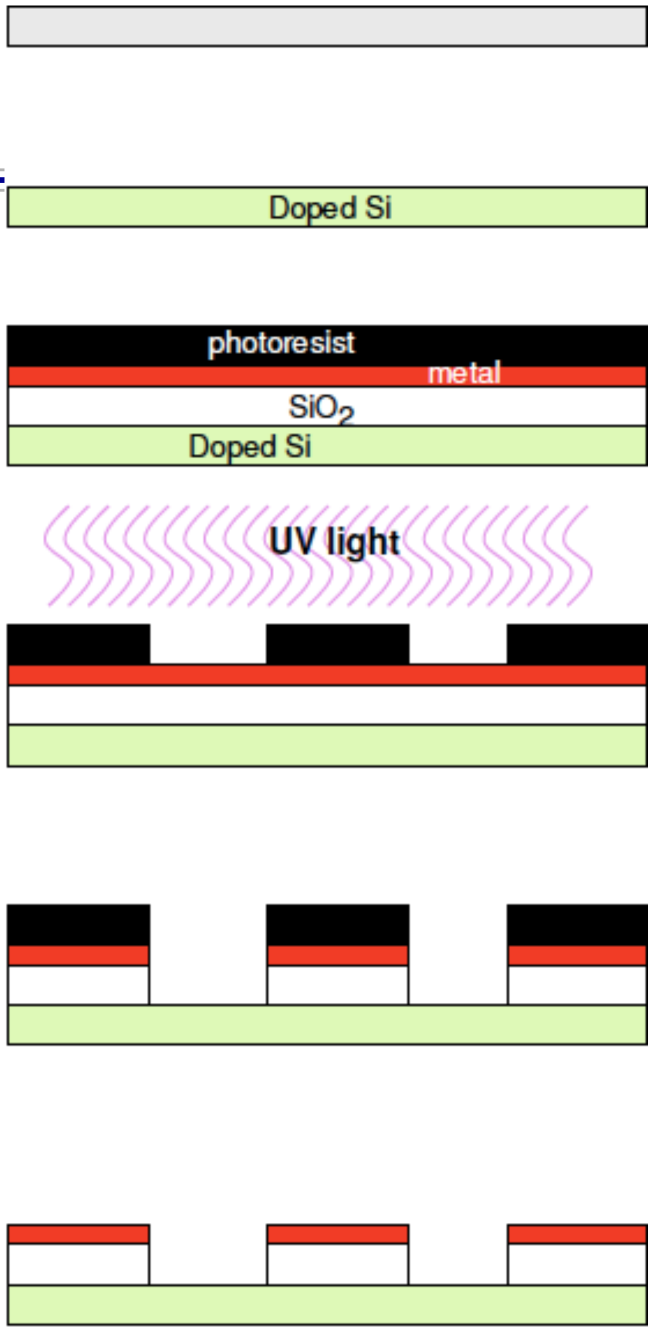


Fabrication

- Start with Silicon wafer
- Dope silicon
- Grow Oxide (SiO_2)
- Deposit Metal
- Photoresist mask and etch to define where features go

https://youtu.be/35jWSQXku74?t=119

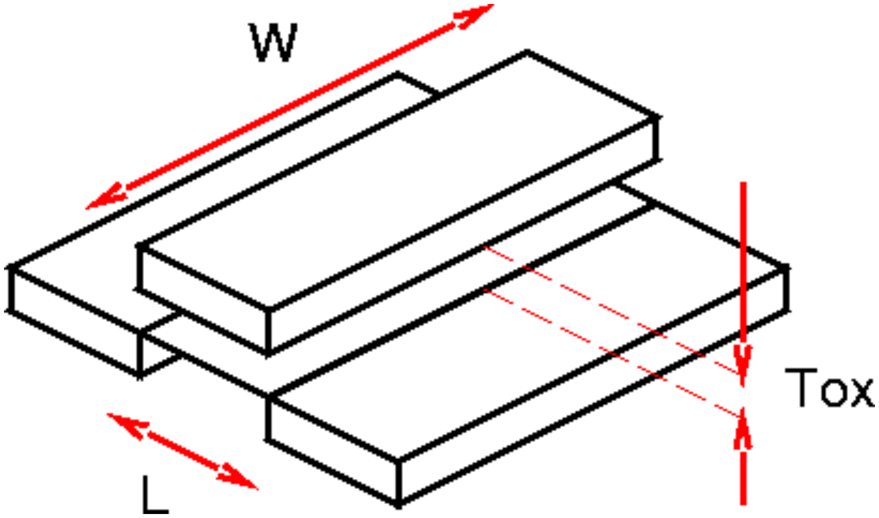
Time Code: 2:00-4:30



Dimensions

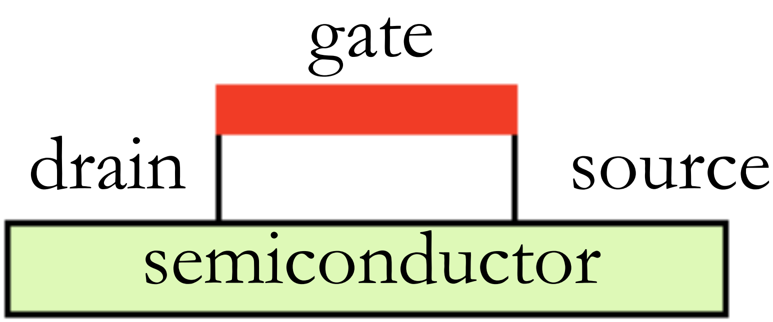
- Channel Length (L)
- Channel Width (W)
- Oxide Thickness (T_{ox})

- Process named by minimum length
  - 22nm → L=22nm

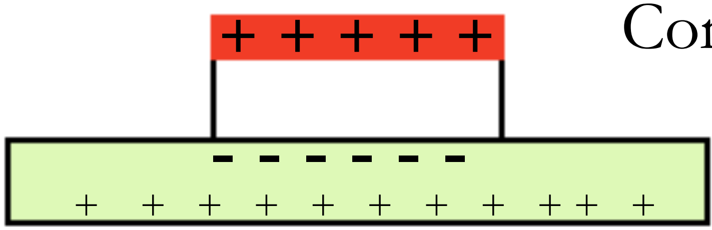


MOS Transistor Operation

So far– MOS model

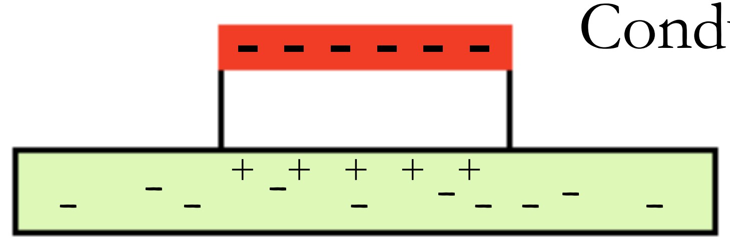


V_{gs} positive
Conducts



NMOS

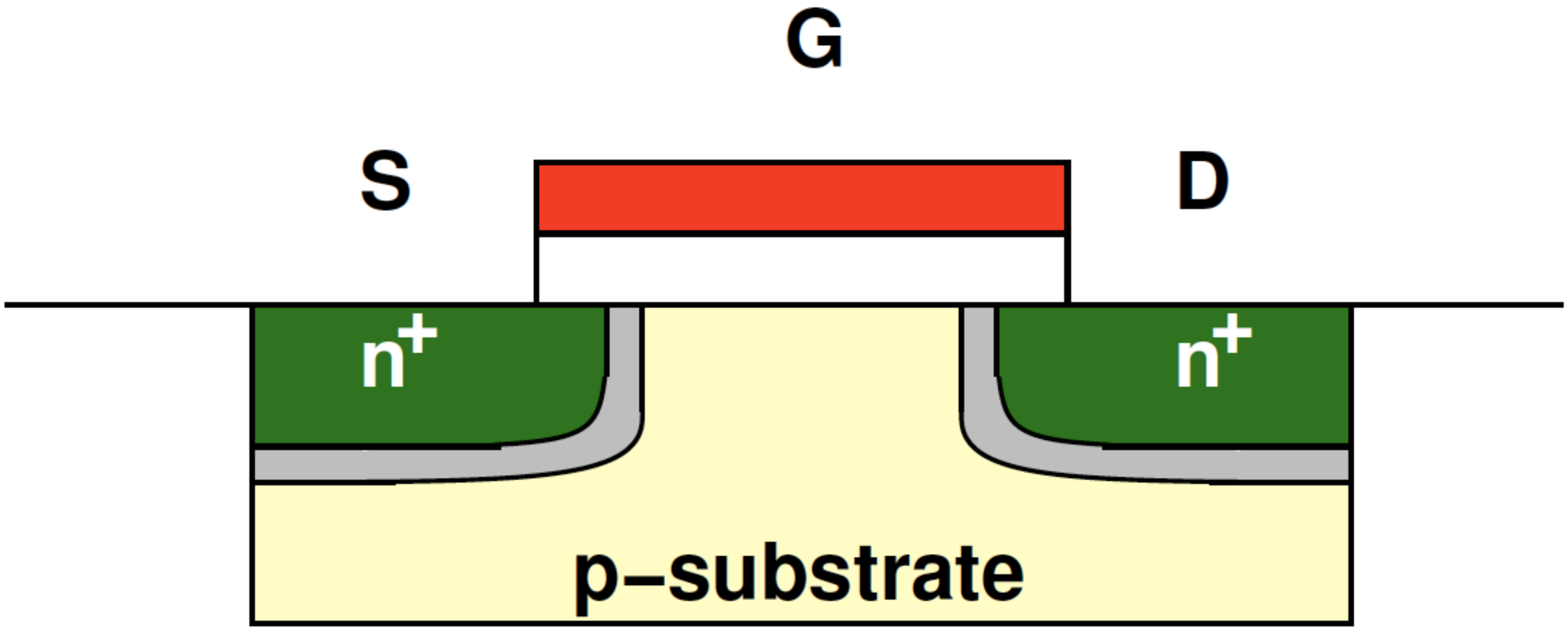
V_{gs} negative
Conducts



PMOS

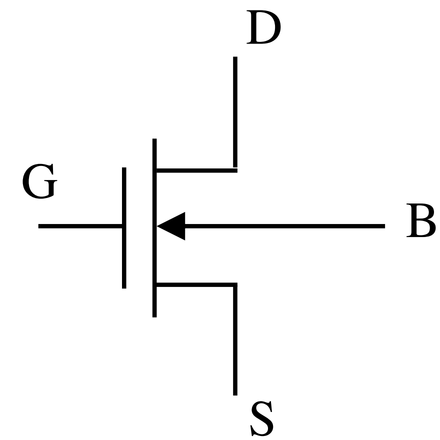
Refinement

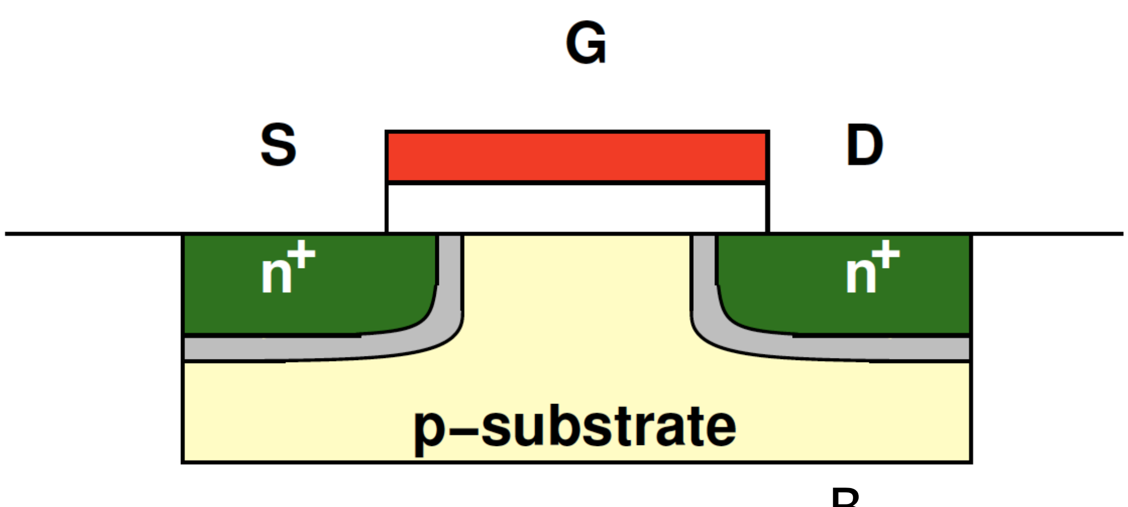
- Depletion region around D/S→ excess carriers depleted



Bulk/Body Contact

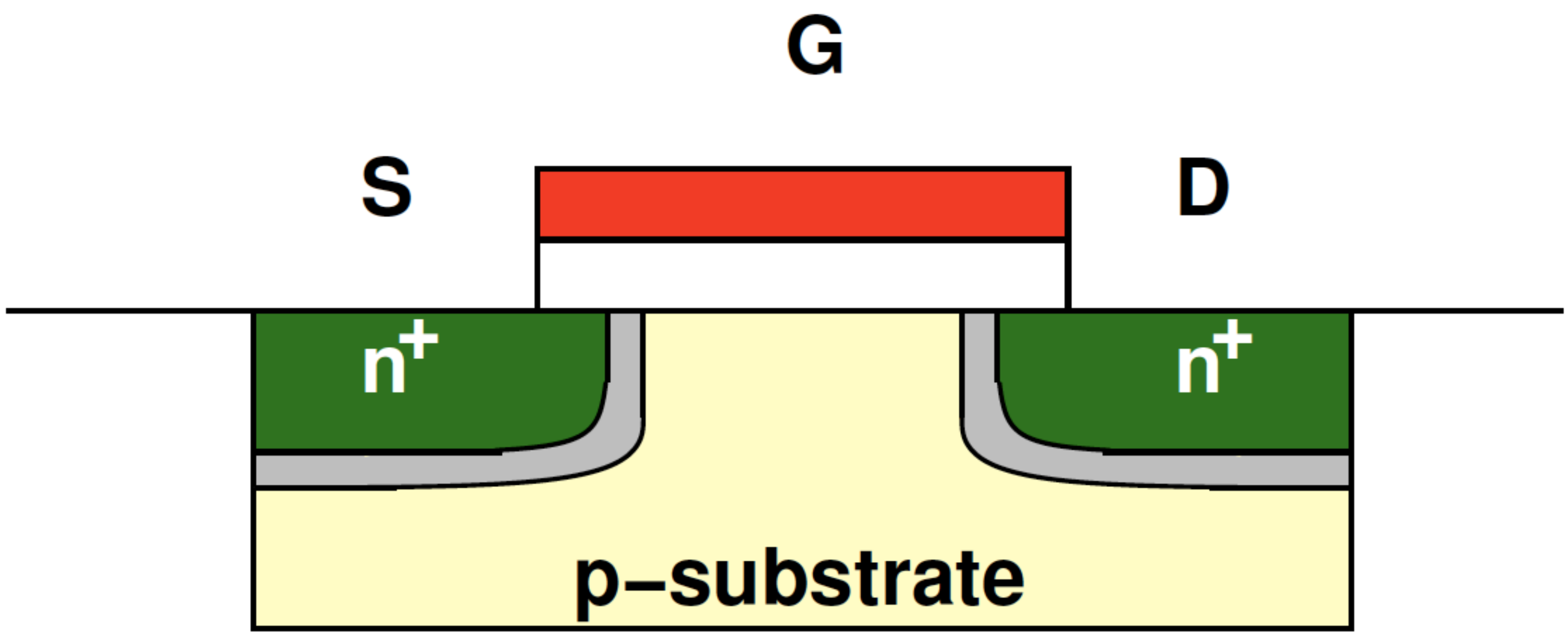
- MOS actually has four contacts
- Also effects fields
- Ideally substrate and source connected
  - Settle for substrate being <= source
  - Gnd for nmos (V_{dd} for pmos)





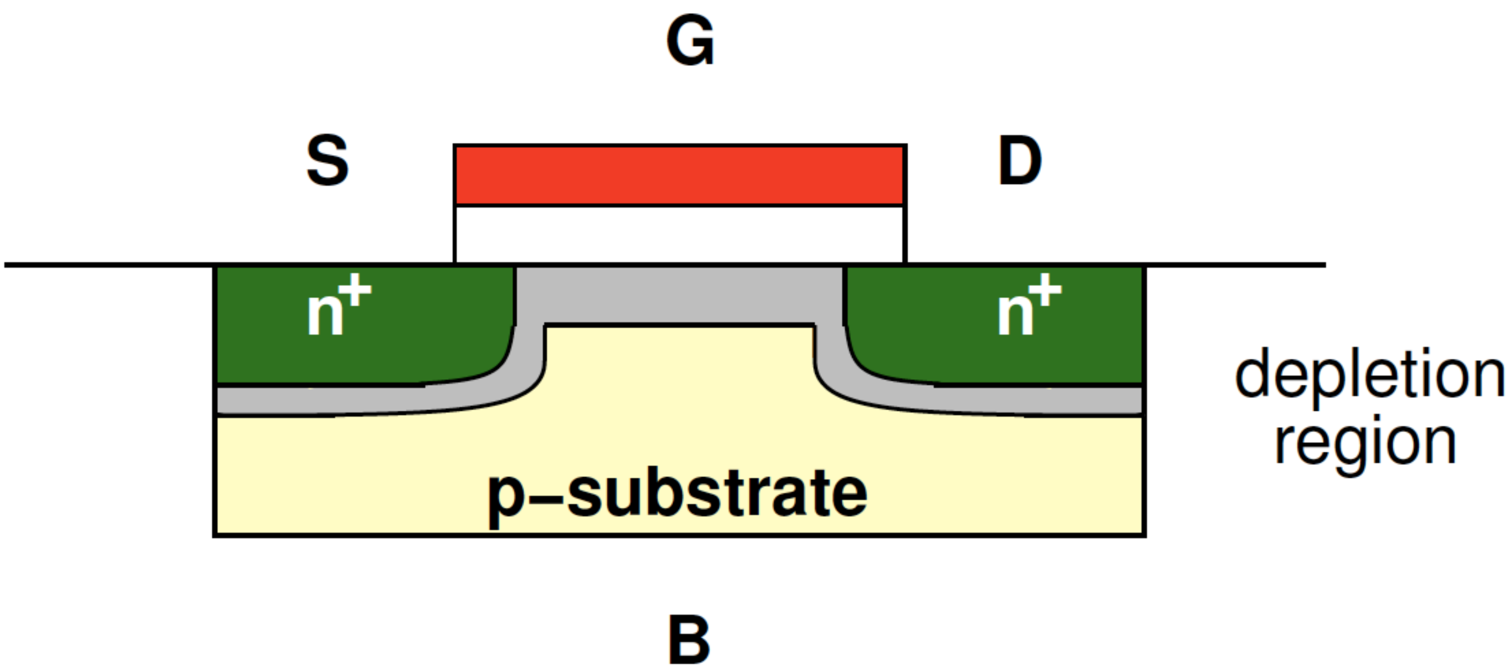
No Field

- $V_{GS}=0$, $V_{DS}=0$

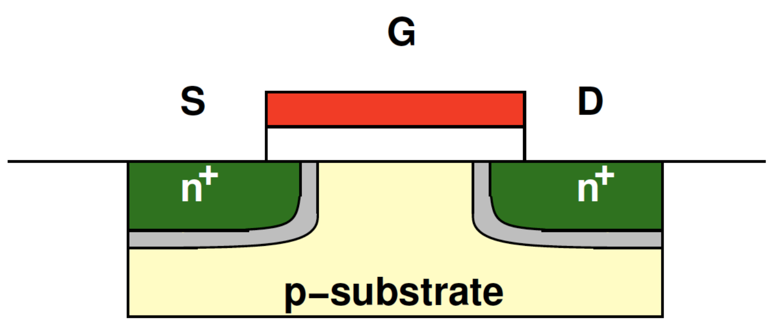


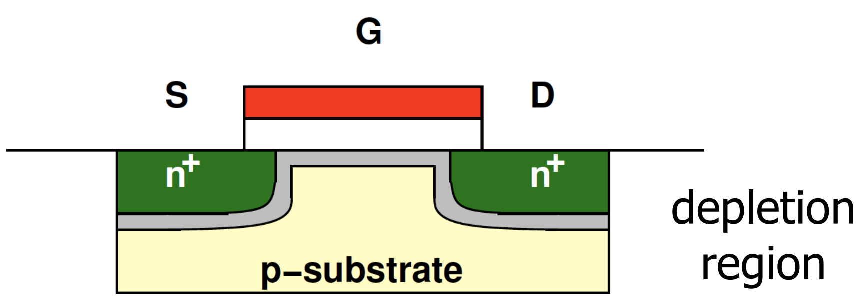
Apply $V_{GS}>0$

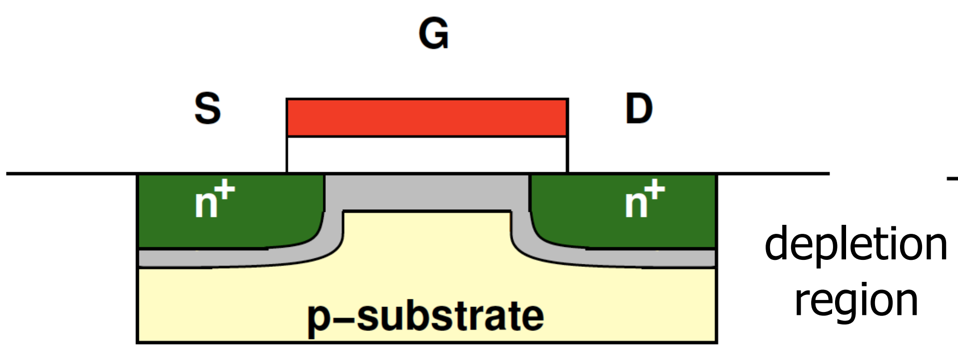
- Deplete excess positive charge under oxide
- Left with negative charge
  - Repel holes

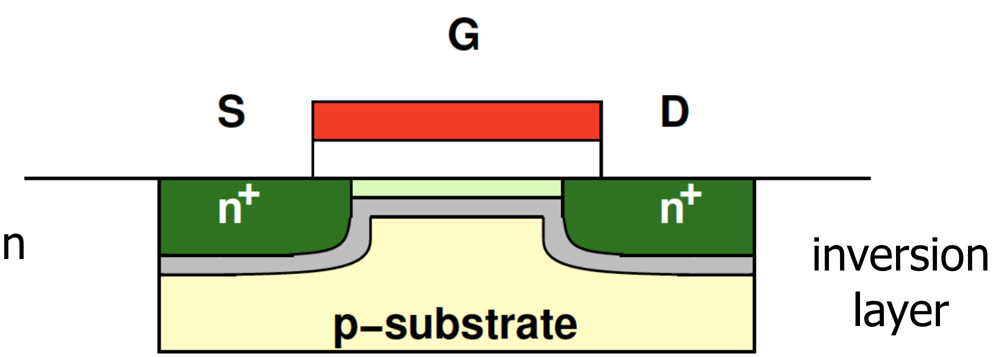


Channel Evolution -- Increasing Vgs



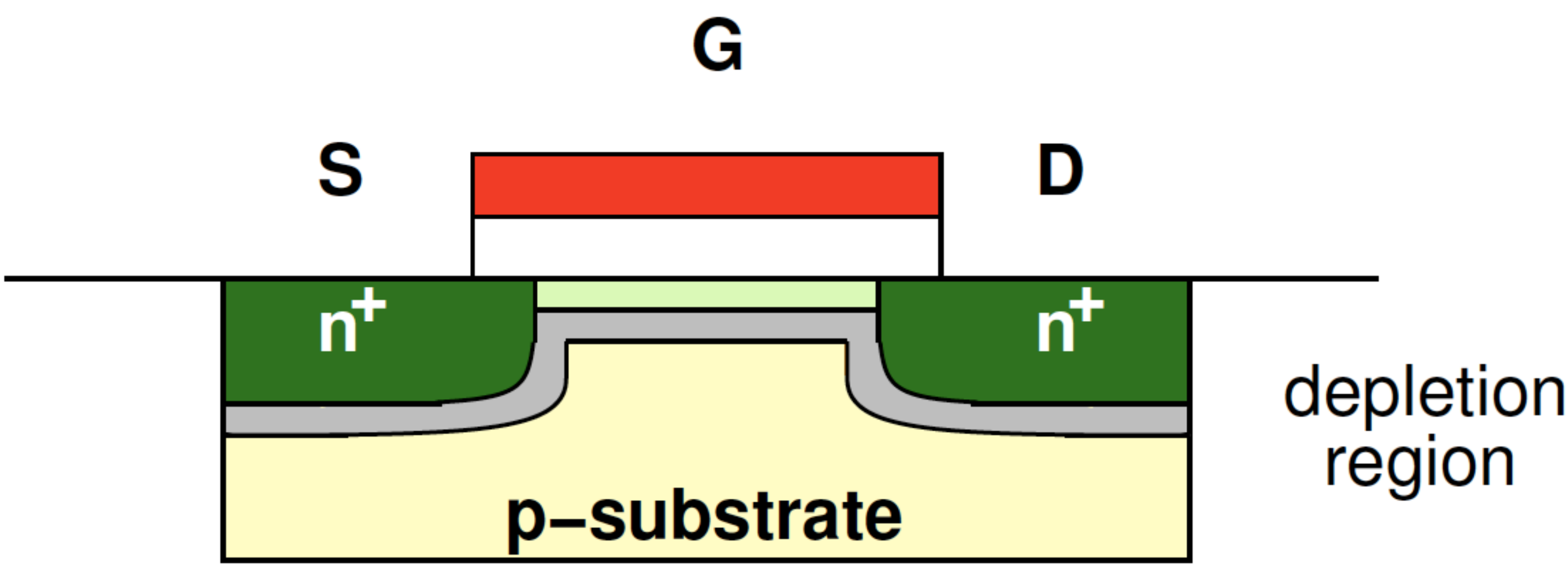






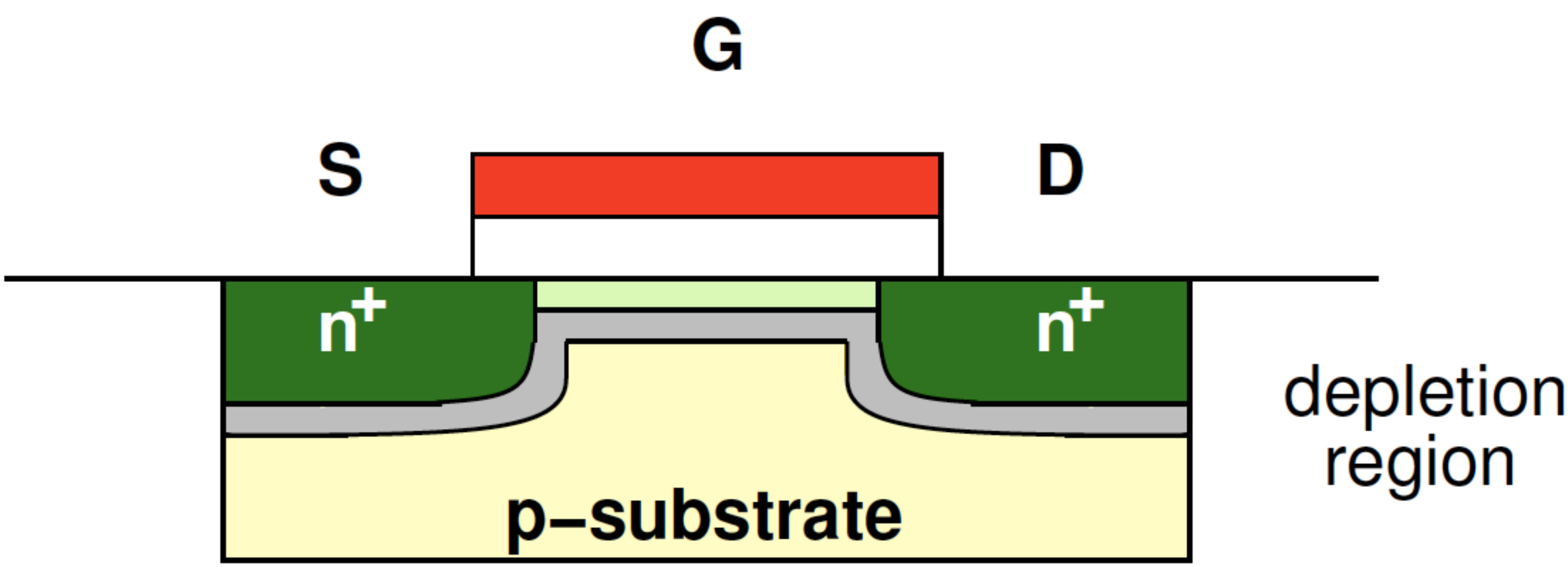
Inversion

- Surface builds electrons
  - Inverts to n-type
  - Draws electrons from n^+ source terminal



Threshold

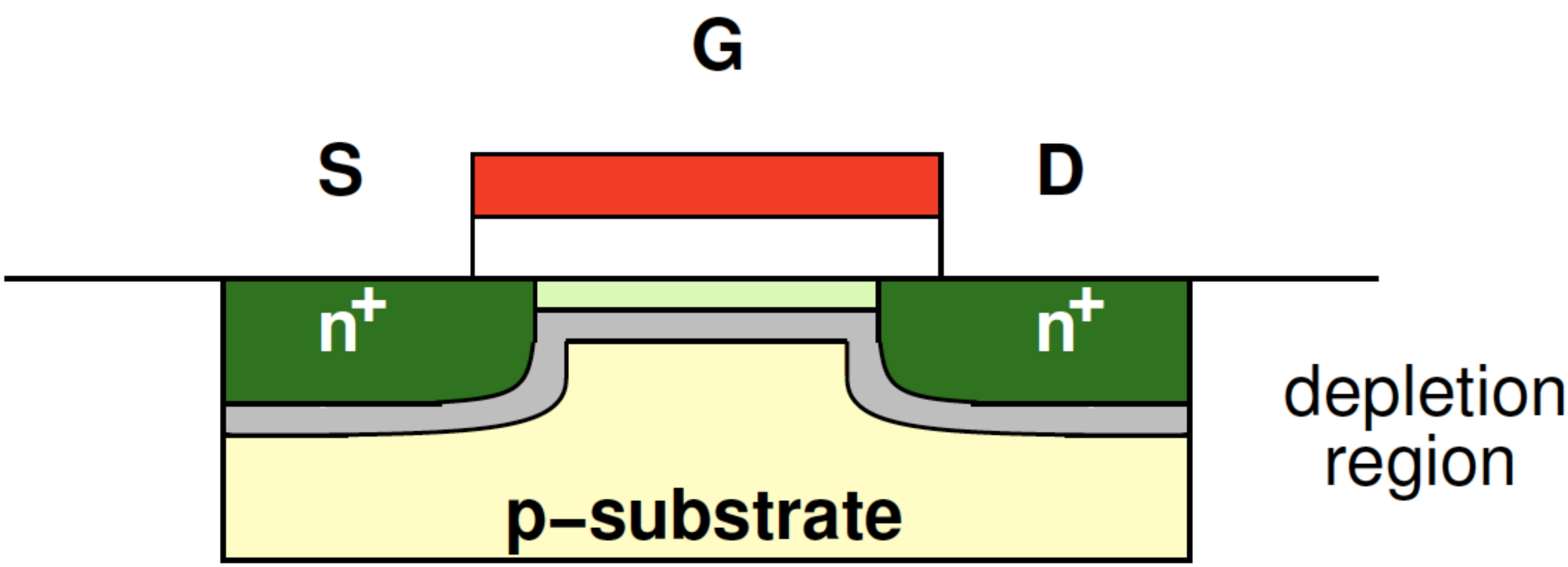
- Voltage where strong inversion occurs → threshold voltage
  - $V_{th} \sim= 2\phi_F$



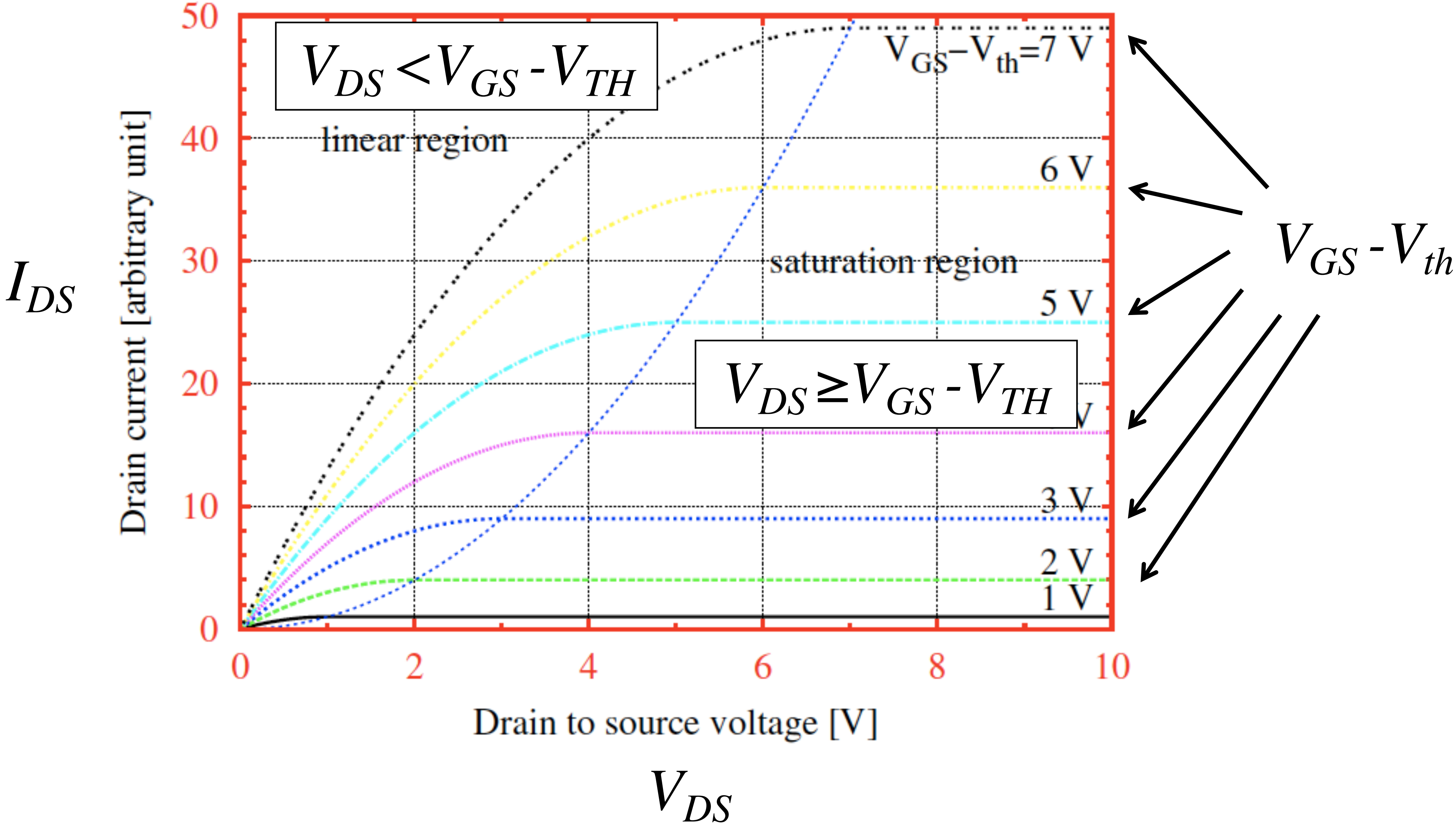
Threshold

- Voltage where strong inversion occurs → threshold voltage
  - $V_{th} \sim= 2\phi_F$
  - Engineer by controlling doping (N_A)

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

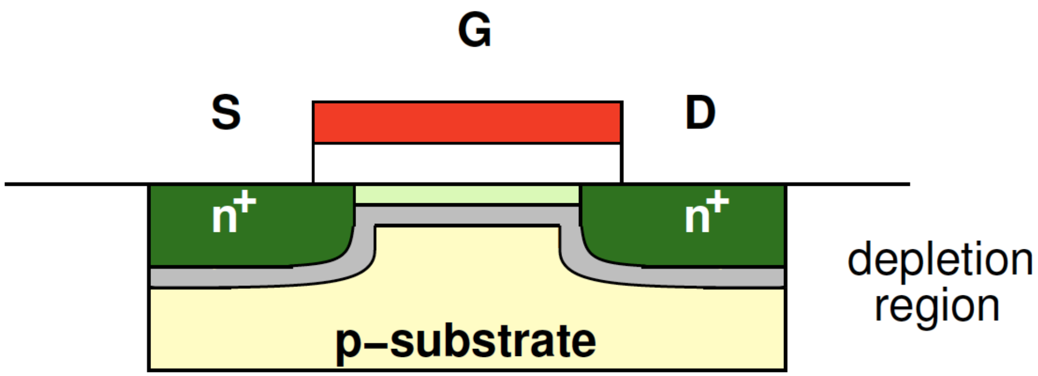


MOSFET – IV Characteristics



Linear Region

- $V_{GS} > V_{th}$ and V_{DS} small



$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Linear Region

- $V_{GS}>V_{th}$ and V_{DS} small
- V_{GS} fixed → looks like resistor
  - Current linear in V_{DS}

$$I_{DS}=\mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS}-V_{th}\right)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

Linear Region

- $V_{GS}>V_{th}$ and V_{DS} small
- V_{GS} fixed → looks like resistor
  - Current linear in V_{DS}

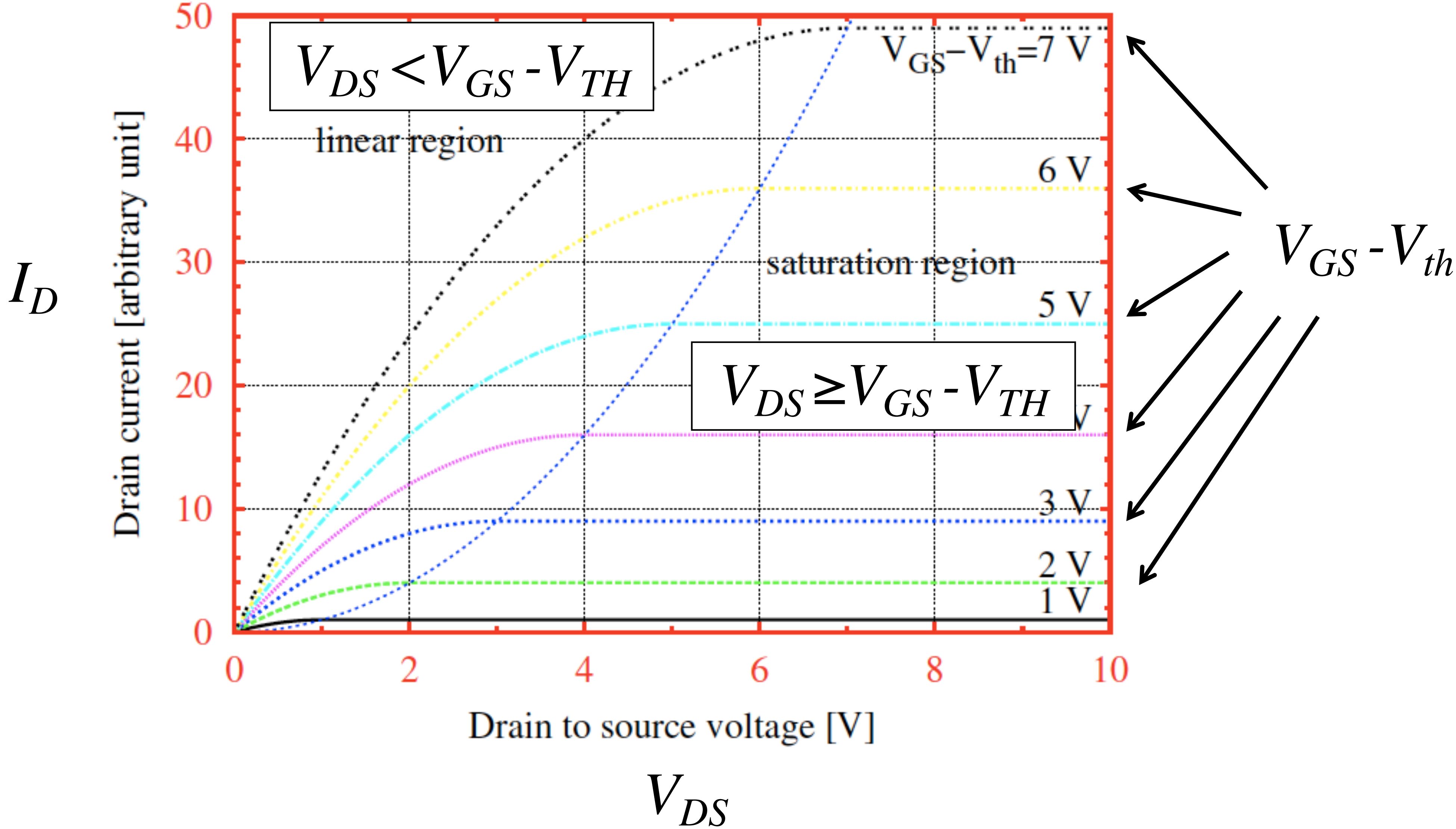
~0

$$I_{DS}=\mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS}-V_{th}\right)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

$$I_{DS}\approx\mu_n C_{OX}\left(\frac{W}{L}\right)\left(V_{GS}-V_{th}\right)V_{DS}$$

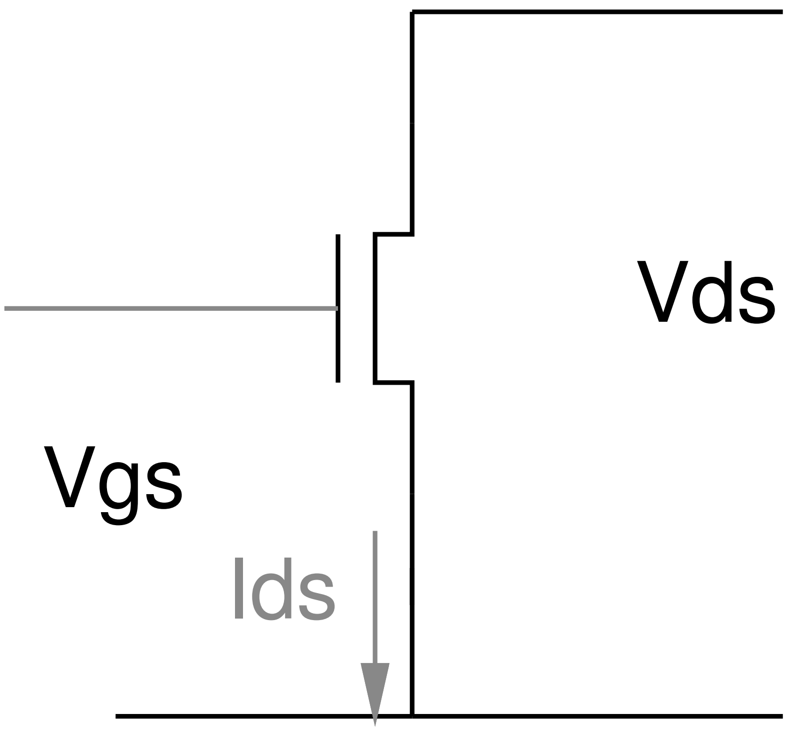
$$I_{DS}\propto V_{DS}$$

MOSFET – IV Characteristics



Preclass 2

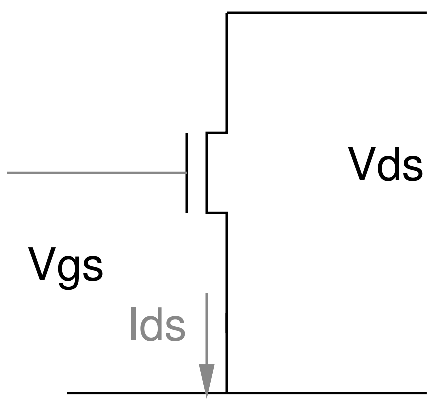
- Reference: I_{ds} for single transistor with Vgs and Vds bias

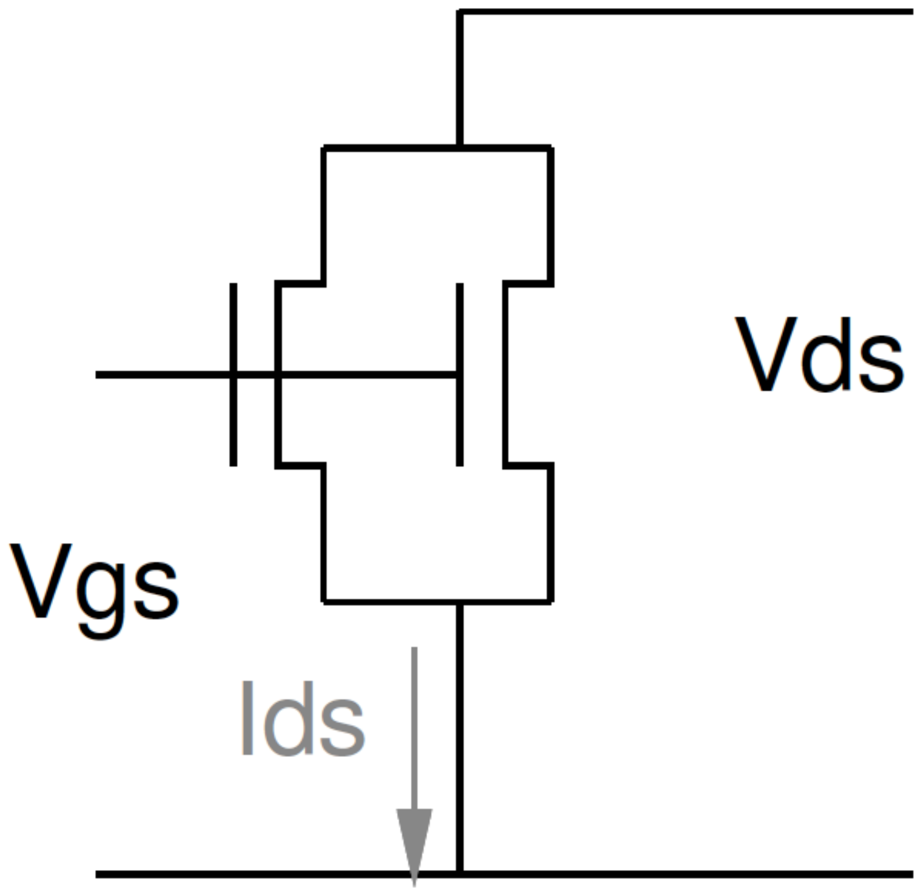


Preclass 2

- I_{ds} for identical transistors in parallel?

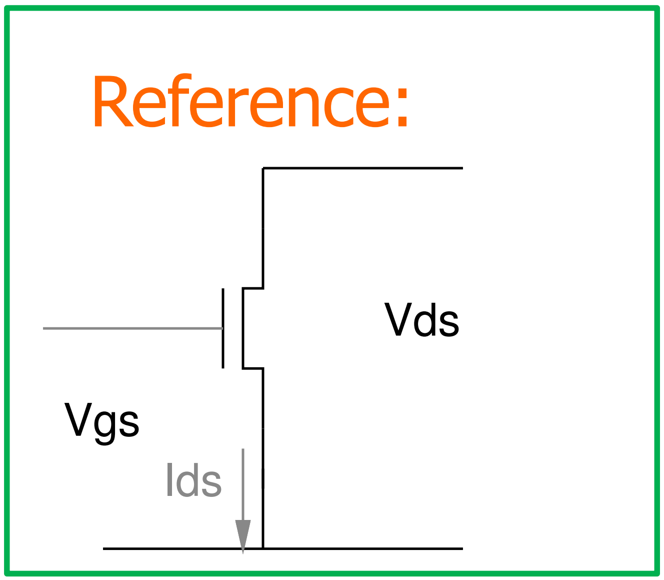
Reference:

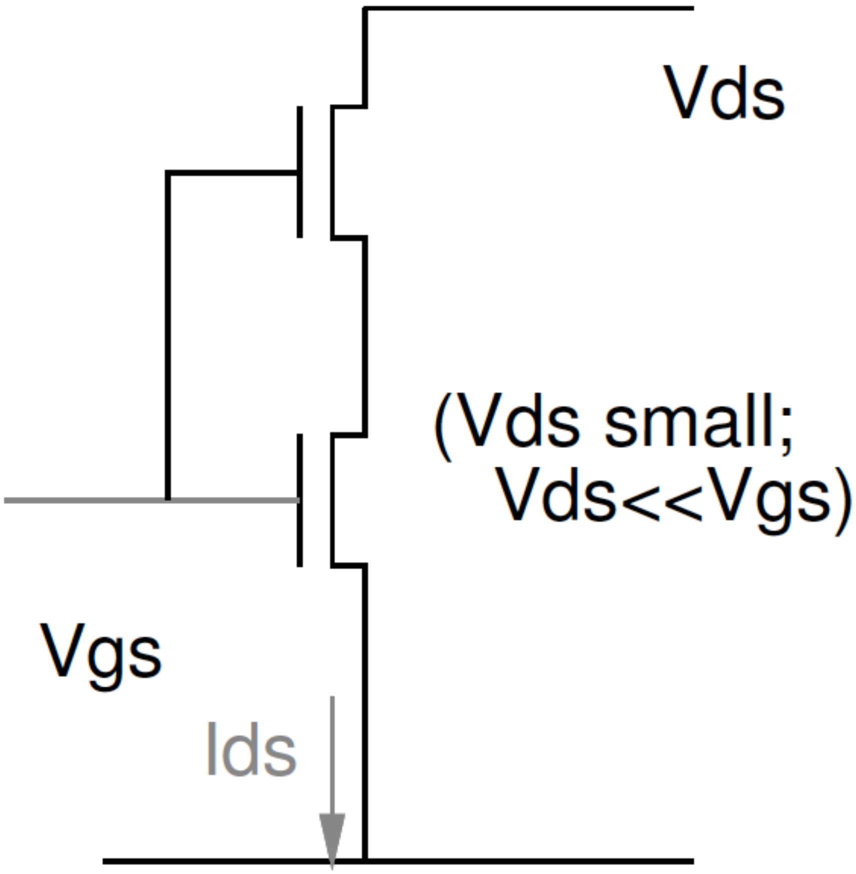




Preclass 2

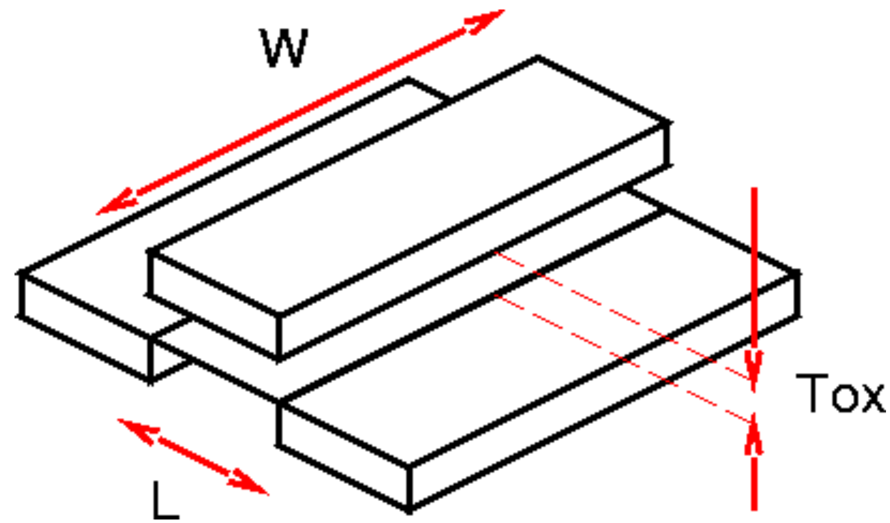
- I_{ds} for identical transistors in series?
  - (Vds small)

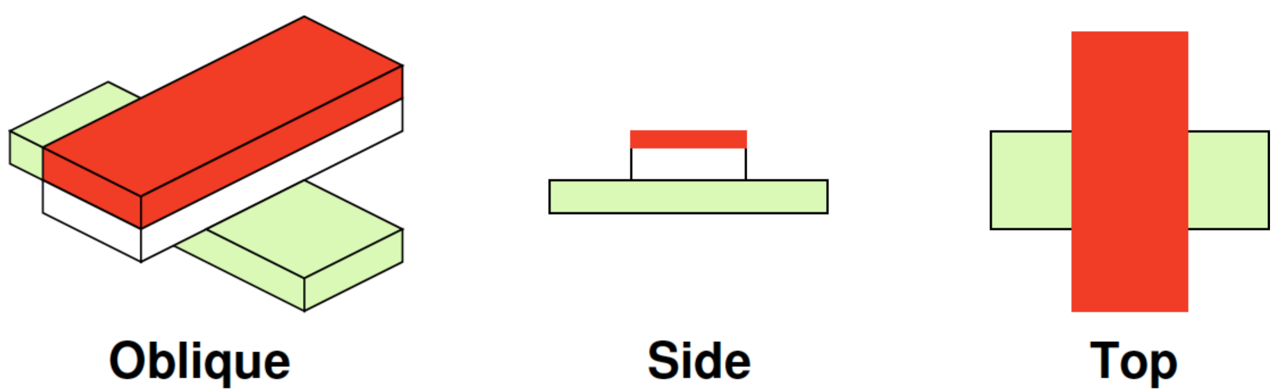




Dimensions

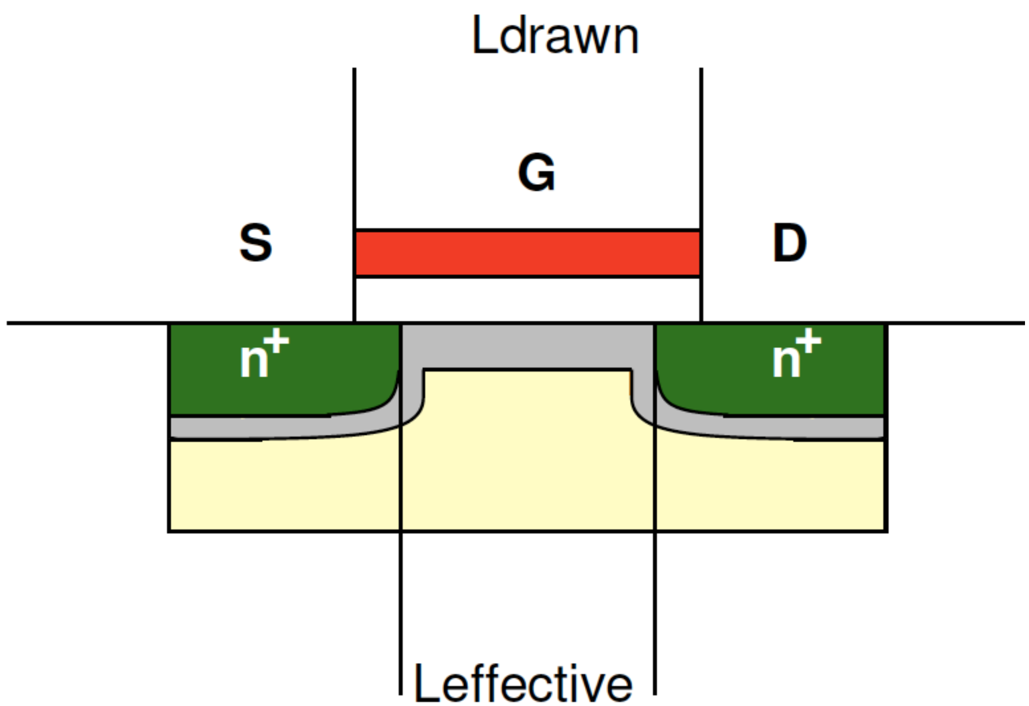
- Channel Length (L)
- Channel Width (W)
- Oxide Thickness (T_{ox})





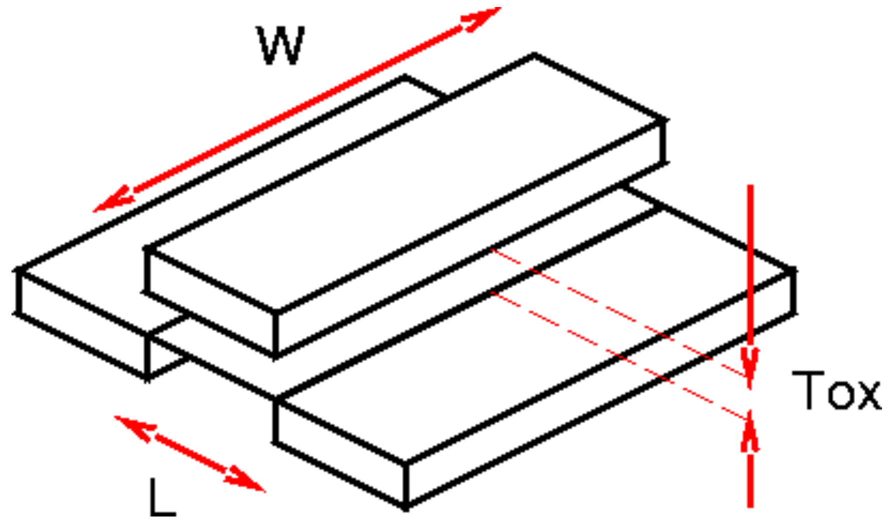
L_{drawn} vs. $L_{effective}$

- Doping not perfectly straight
- Spreads under gate
- Effective L smaller than draw gate width



Transistor Strength (W/L)

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$



$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Transistor Strength (W/L)

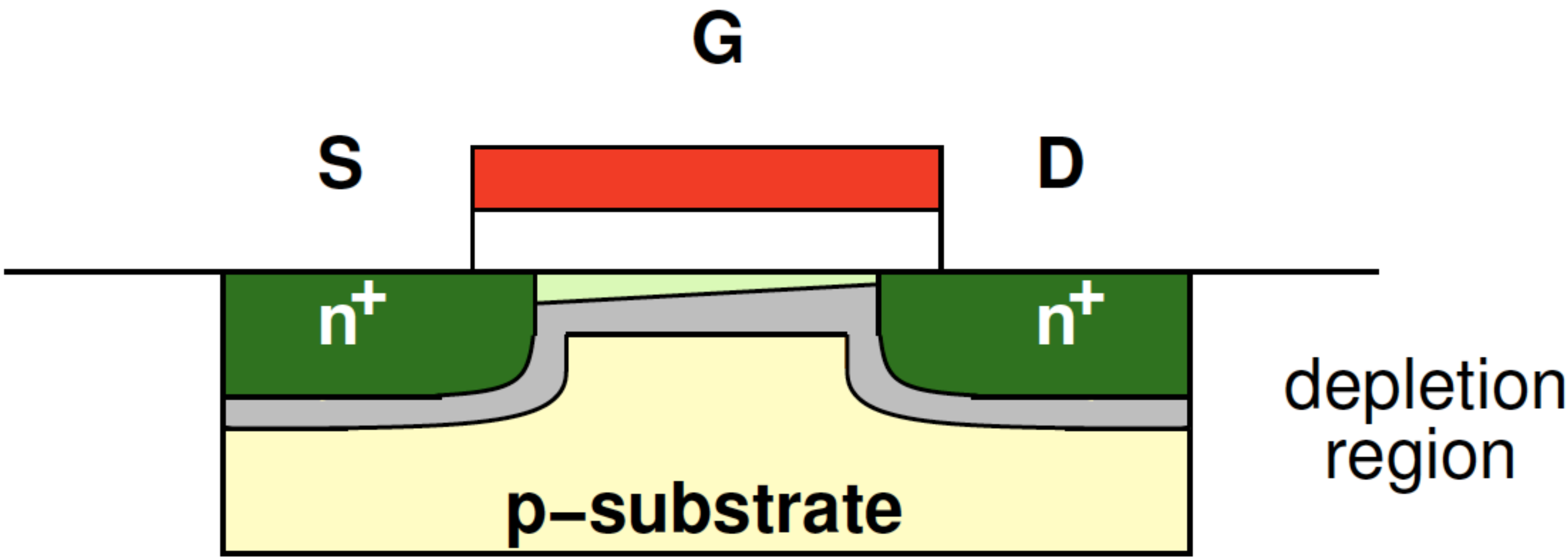
- Shape dependence match Resistance intuition
  - Wider = parallel resistors → decrease R
  - Longer = series resistors → increase R

$$R = \frac{\rho L}{A}$$

$$I_{DS} = \mu_n C_{OX} \left(\frac{W}{L}\right)\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

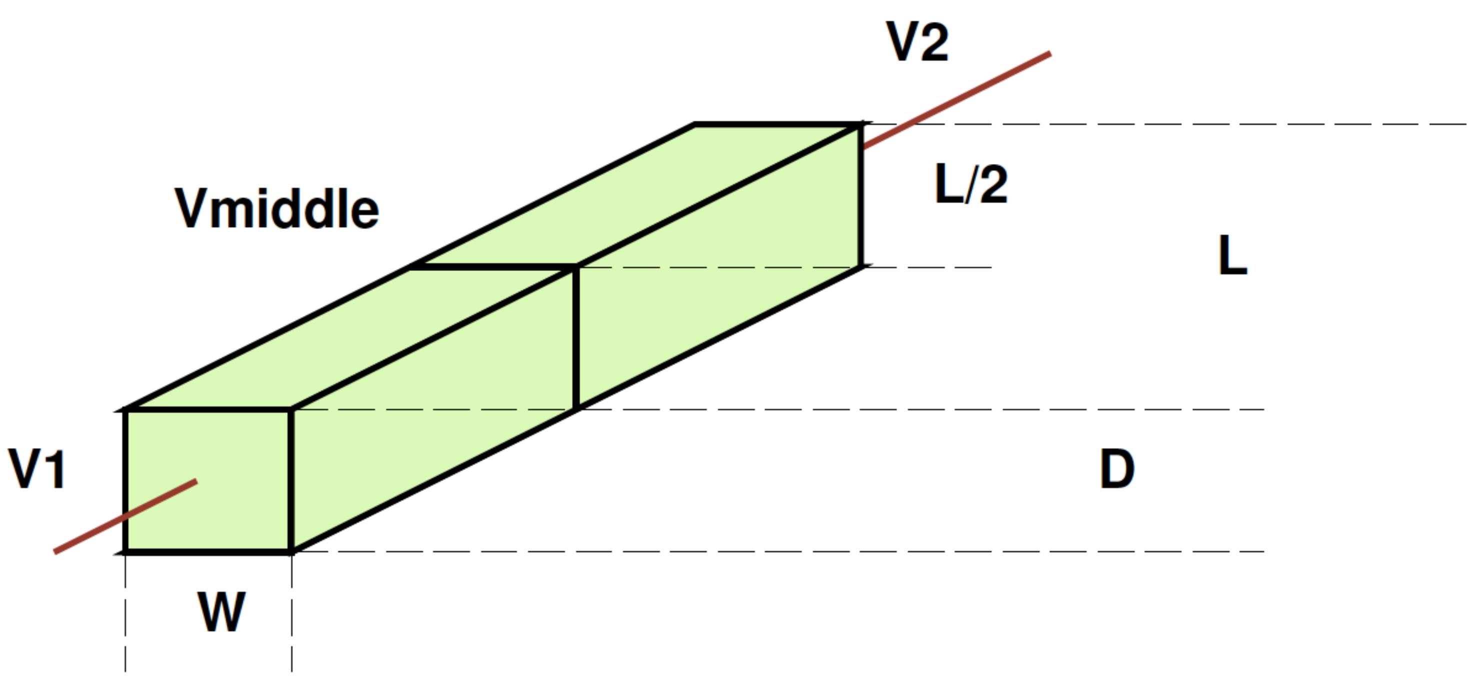
Channel Voltage

- Think of channel as resistor
- Voltage varies along channel



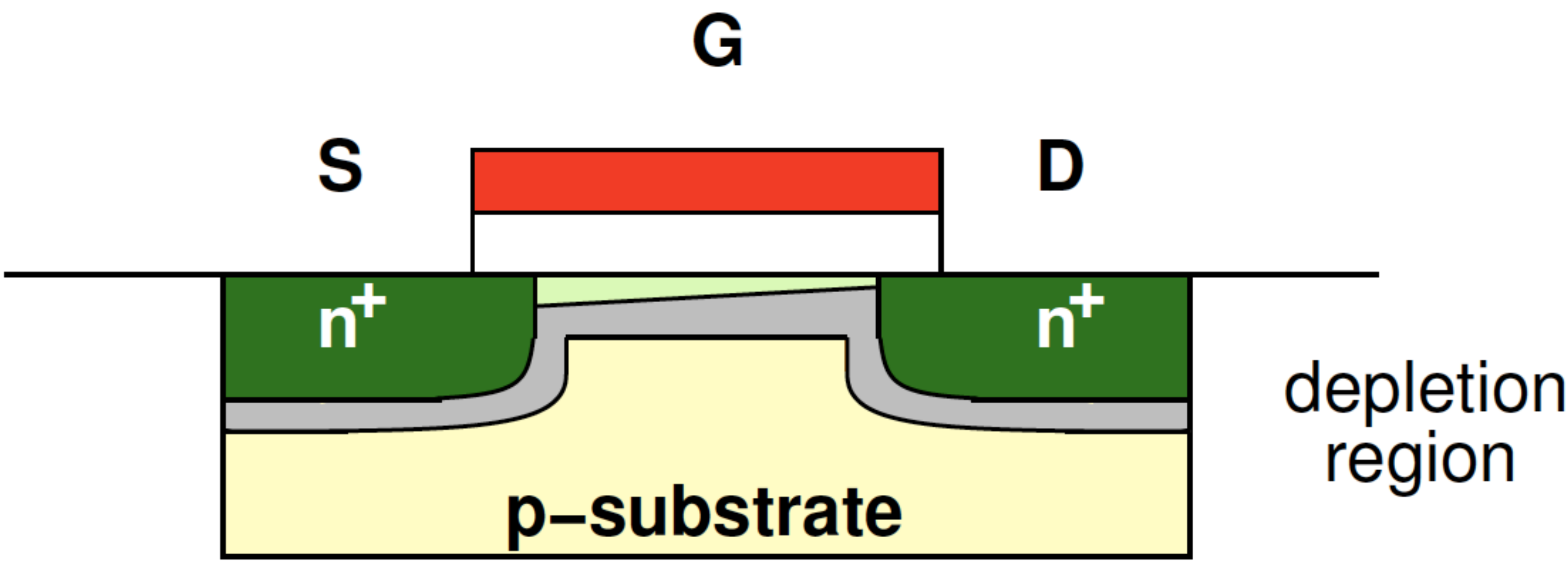
Preclass 3

- What is voltage in the middle of a resistive medium?
  - Relative to V1 and V2
  - halfway between terminals



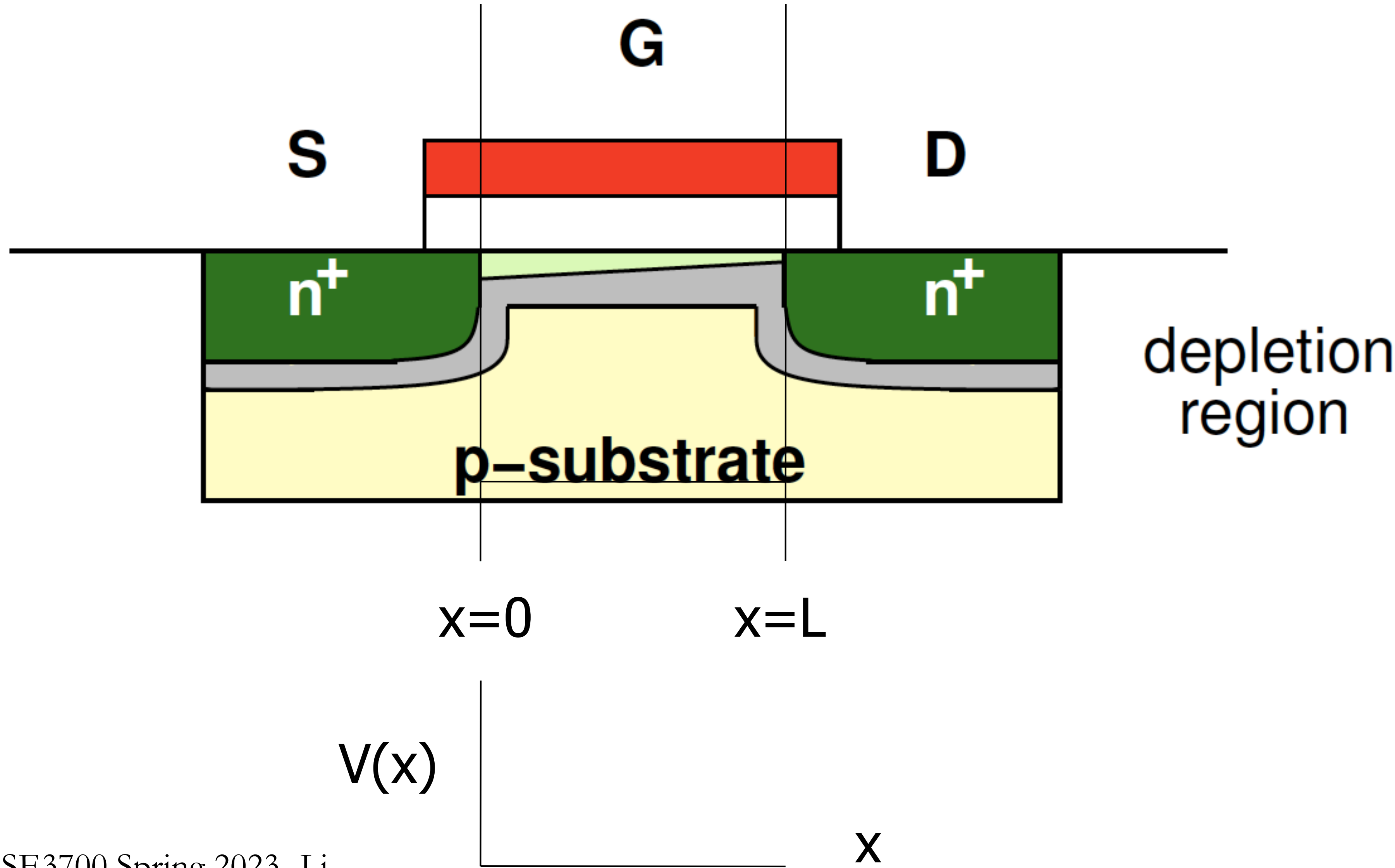
Channel Voltage

- Think of channel as resistor
- Voltage varies along channel
  - Serves as a voltage divider between V_S and V_D



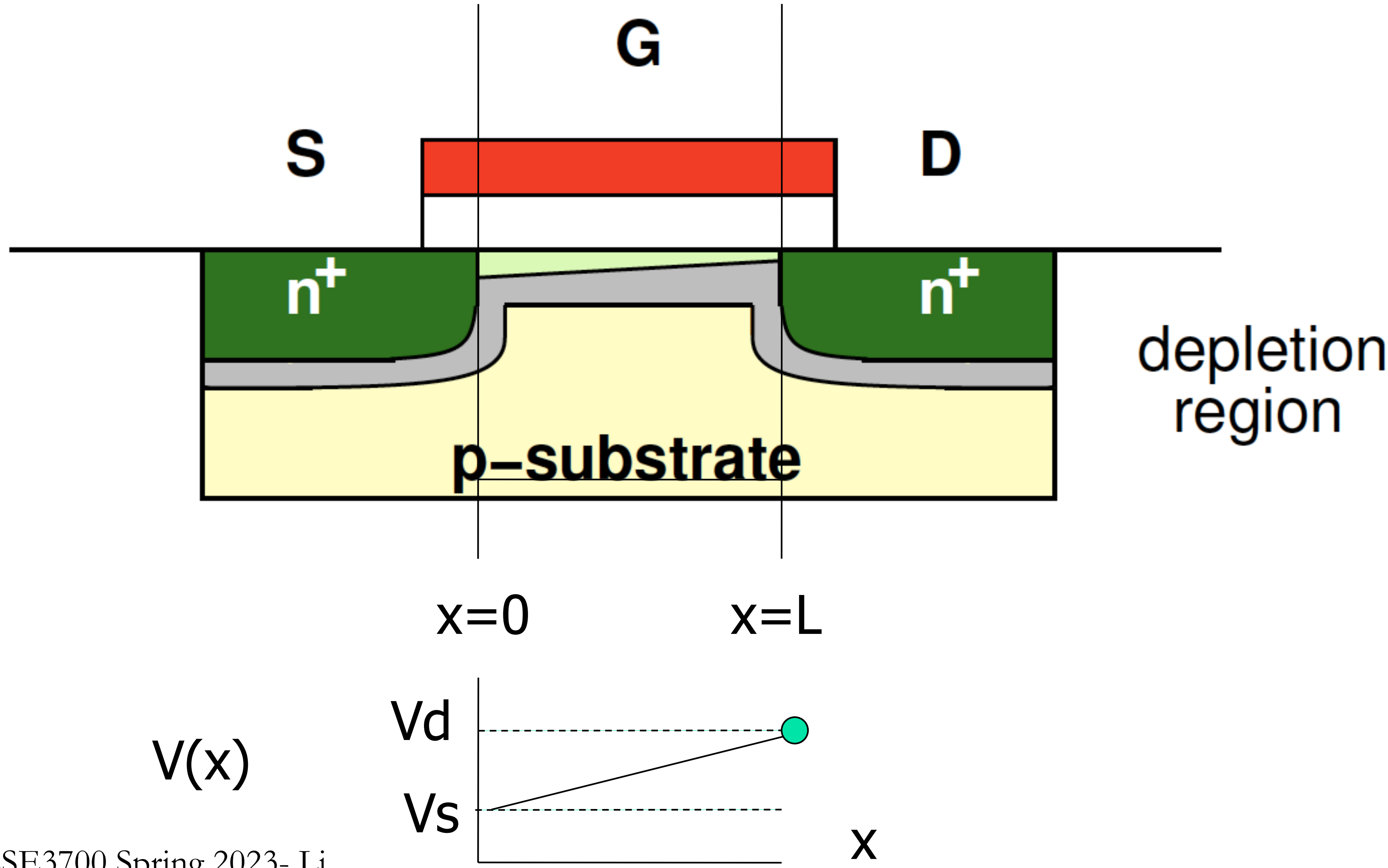
Voltage along Channel

- What does voltage along the channel look like?



Voltage along Channel

- What does voltage along the channel look like?



Device Operation (Current – Voltage Relation):

However: $\mathcal{E}(x) = \frac{dV}{dx}$ So: $\mathcal{V} = \mu_n \frac{dV}{dx}$

Therefore: $I_D dx = \mu_n C_{OX} W (V_{GS} - V - V_T) dV$

$$\int_0^L I_D dx = \int_0^{V_{DS}} \mu_n C_{OX} W (V_{GS} - V - V_T) dV$$

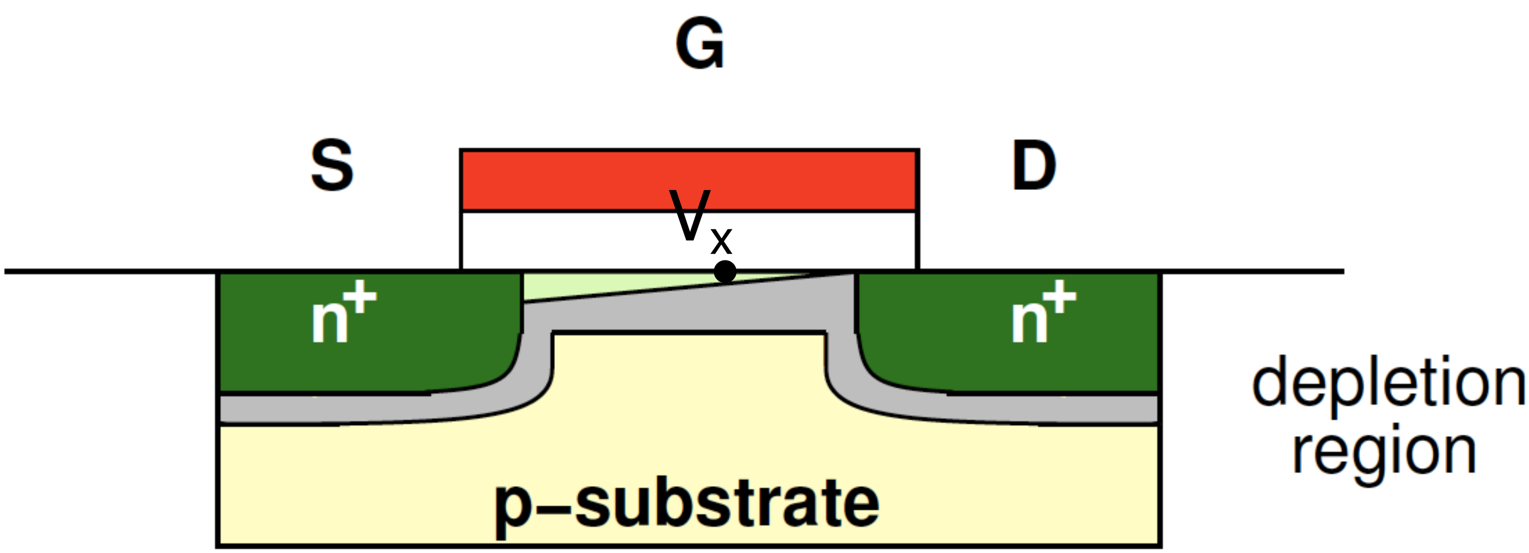
Which yields:

$$I_D = \mu_n C_{OX} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Which is valid for values of $V_{DS} < V_{GS} - V_T$ *(i.e. Linear Region)*

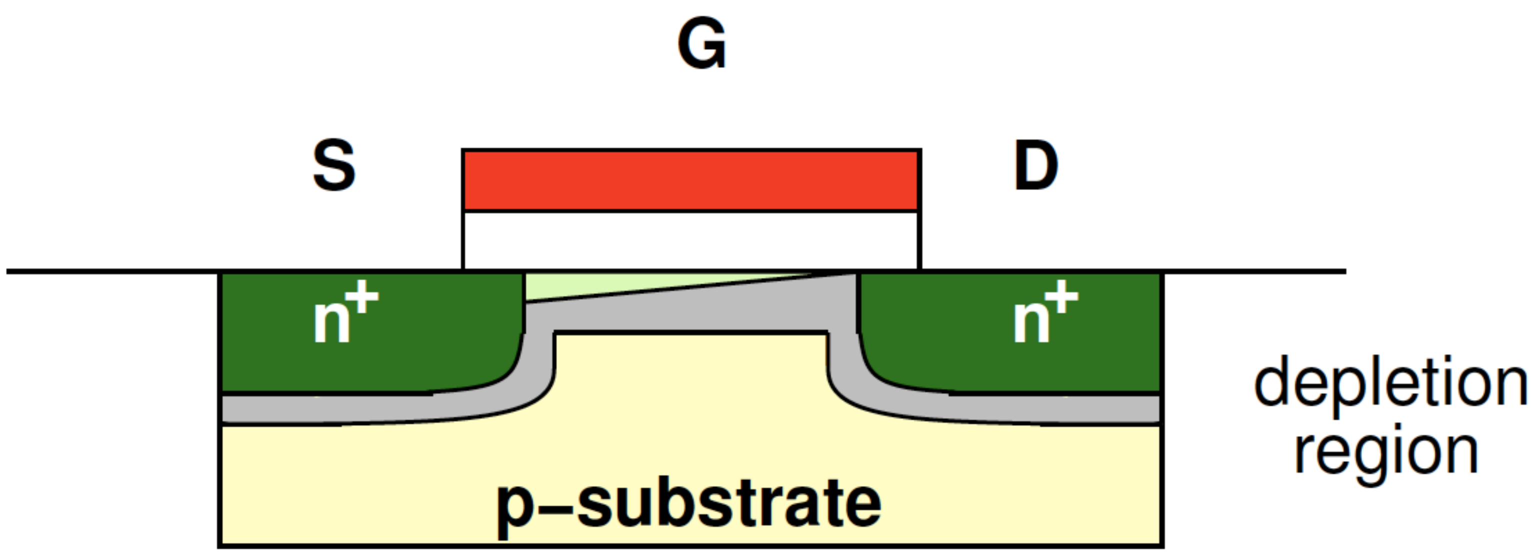
Channel Field

- When voltage gap V_G-V_x drops below V_{th}, drops out of inversion



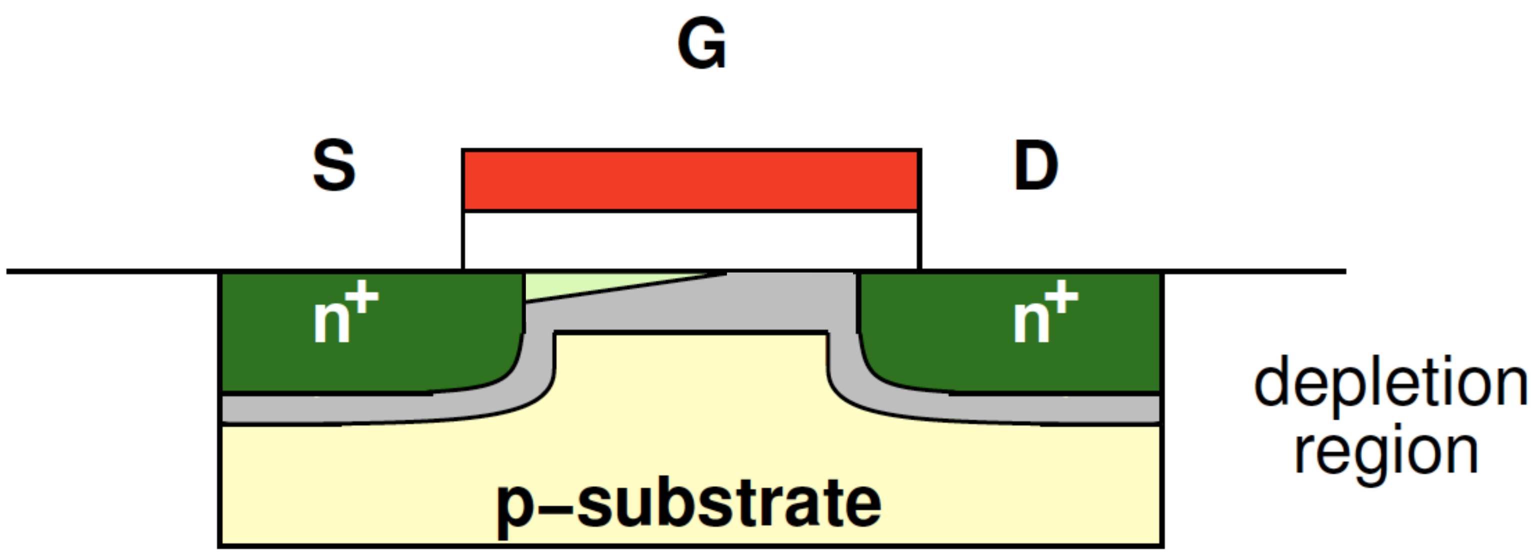
Channel Field

- When voltage gap V_G-V_x drops below V_{th}, drops out of inversion
  - Saturation Edge: $V_{DS} = V_{GS} - V_{th} \rightarrow V_G - V_X(@\ D) = ?$



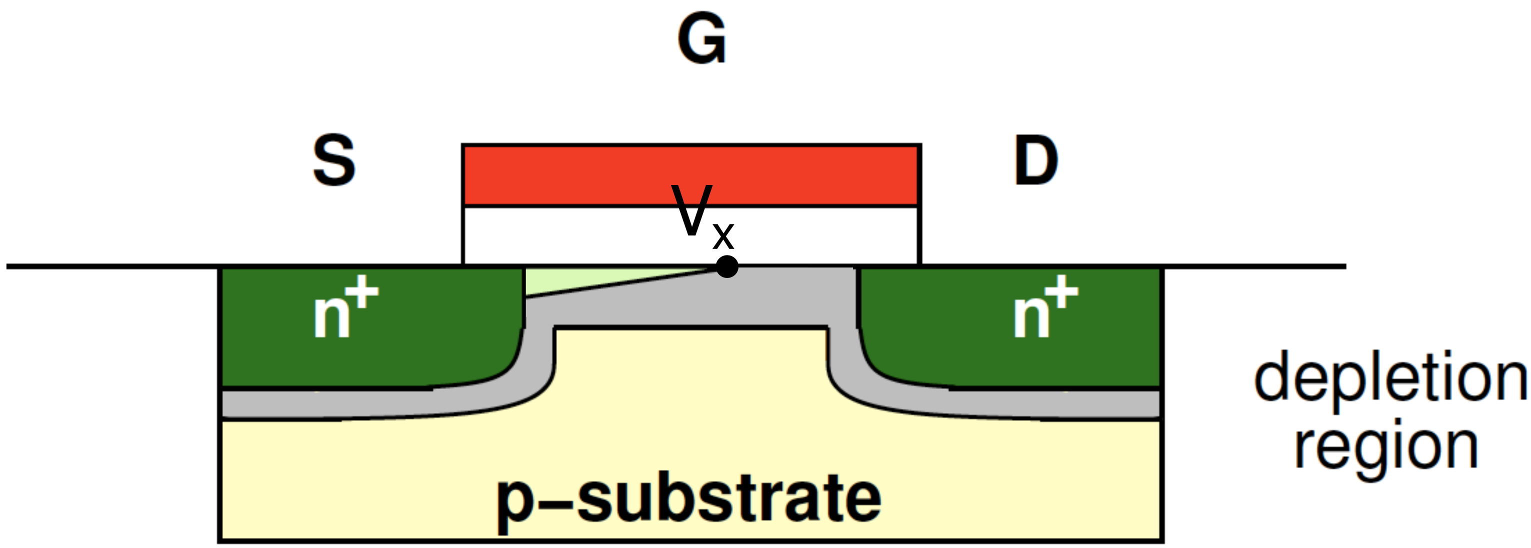
Channel Field

- When voltage gap V_G-V_x drops below V_{th}, drops out of inversion
  - Deep Saturation: $V_{DS} > V_{GS} - V_{th} \rightarrow V_G - V_X(@\ D) = ?$



Channel Field

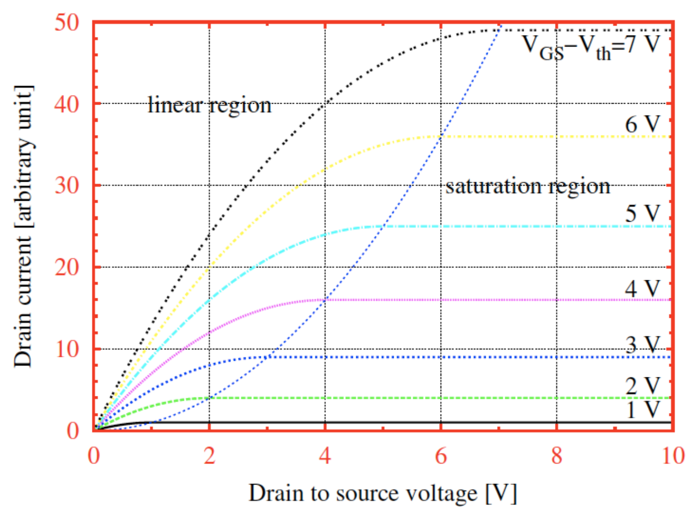
- When voltage gap V_G-V_x drops below V_{th}, drops out of inversion
  - Deep Saturation: $V_{DS} > V_{GS} - V_{th} \rightarrow V_G - V_X(@\ D) < V_{th}$
    Upper limit on current, channel is "pinched off"



Pinch Off

- When voltage along the channel drops below V_{th}, the channel drops out of inversion
  - Occurs when: $V_G - V_X(@\ D) < V_{th} \rightarrow V_{DS} > V_{GS} - V_{th}$

- **Conclusion:**
  - current cannot increase with V_{DS} once $V_{DS} > V_{GS}-V_T$
    - Not true! More later…



Saturation

- At edge of saturation, $V_{DS} = V_{GS} - V_T$

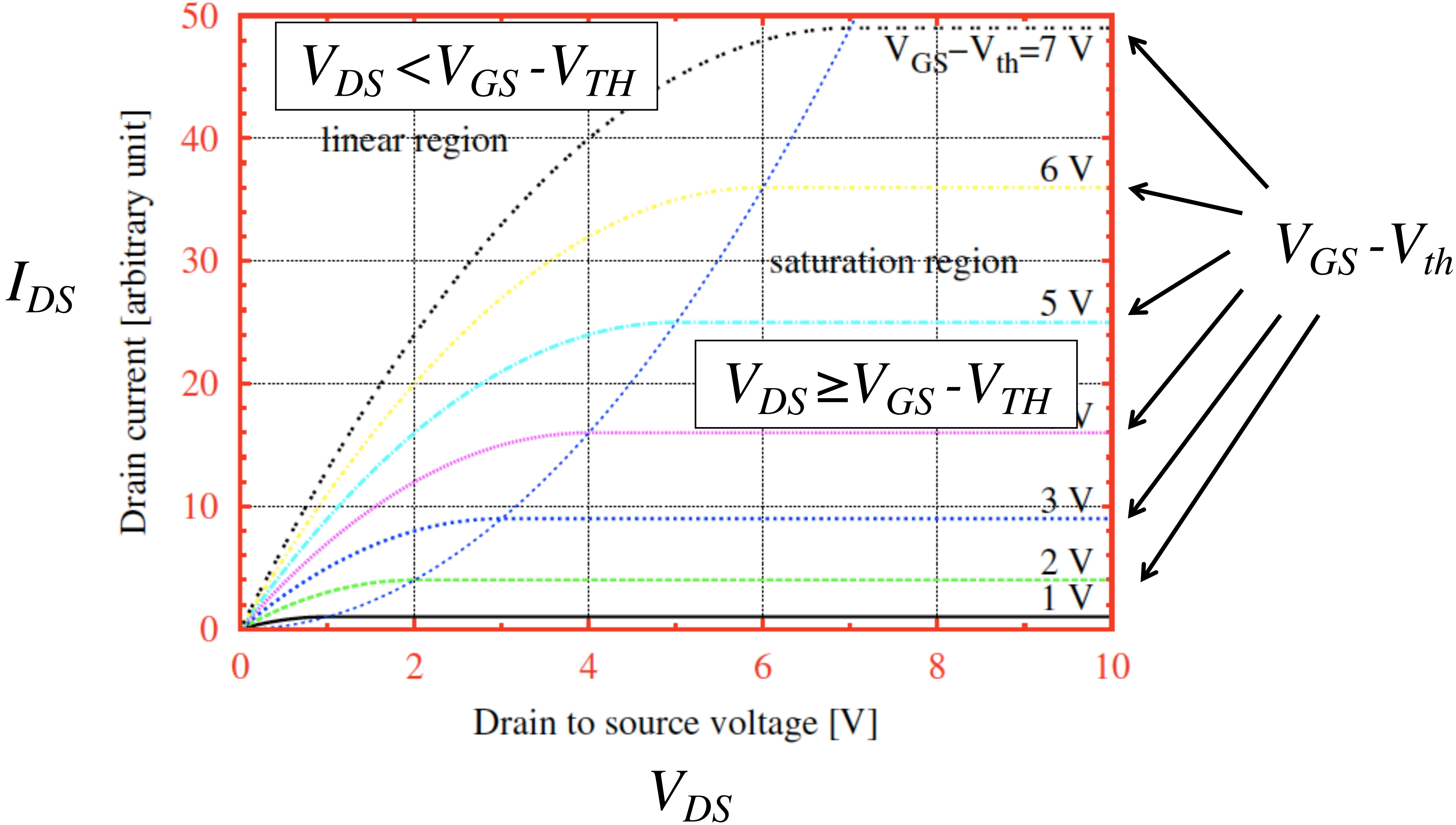
$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- Becomes:

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)^2 - \frac{\left(V_{GS} - V_T\right)^2}{2}\right]$$

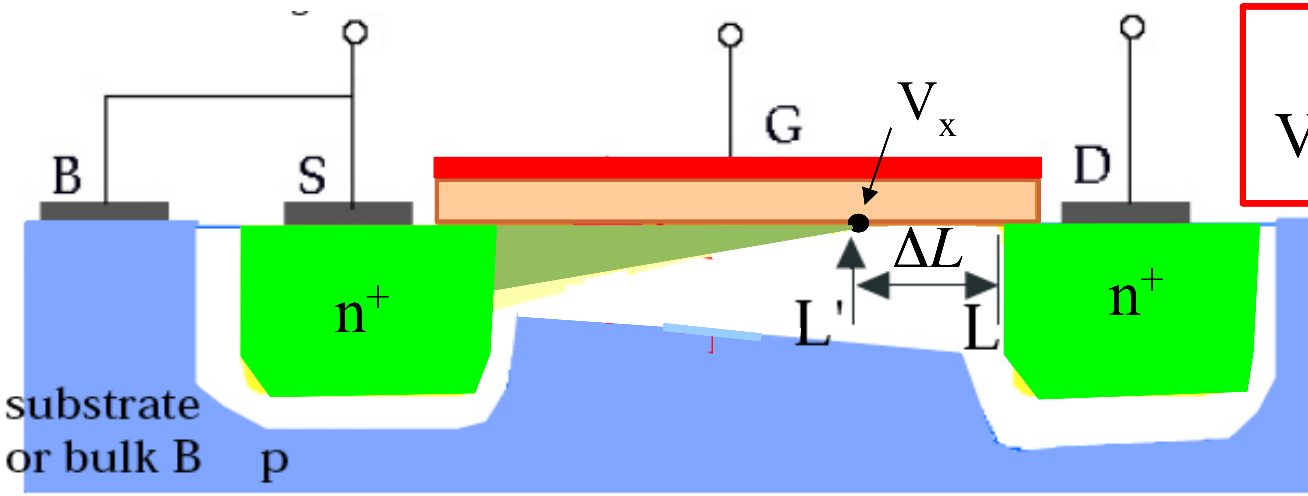
$$I_{DS} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)^2\right]$$

MOSFET – IV Characteristics



Channel Length Modulation

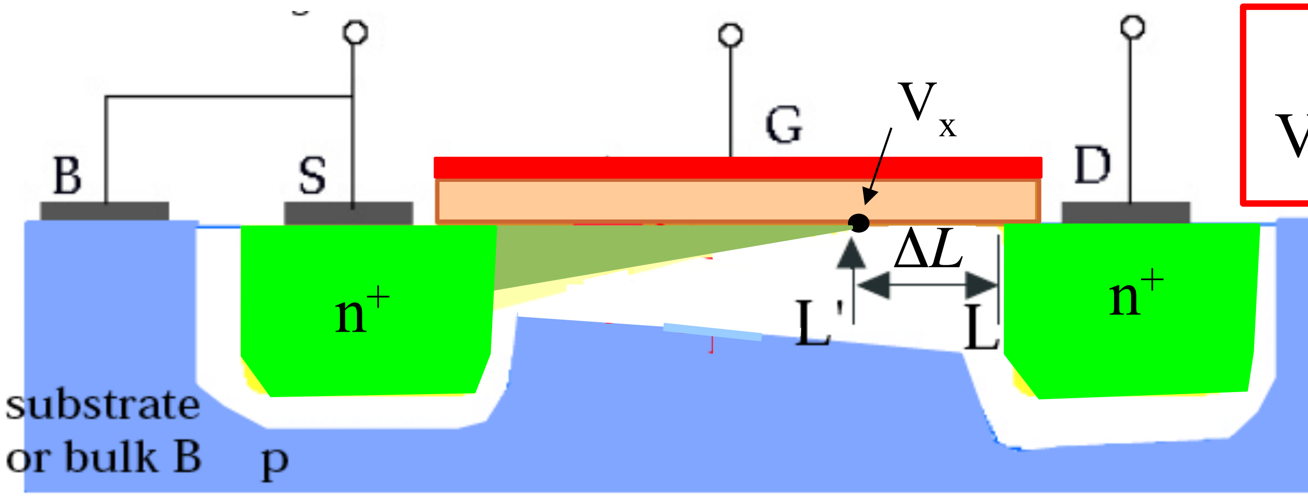
MOSFET IV Characteristics - Saturation



$V_{GS} > V_{T0}$
$V_{DS} > V_{GS} - V_{T0}$

$$I_{DS} = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L'} \left(V_{GS} - V_{T0}\right)^2 = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L - \Delta L} \left(V_{GS} - V_{T0}\right)^2$$

MOSFET IV Characteristics - Saturation



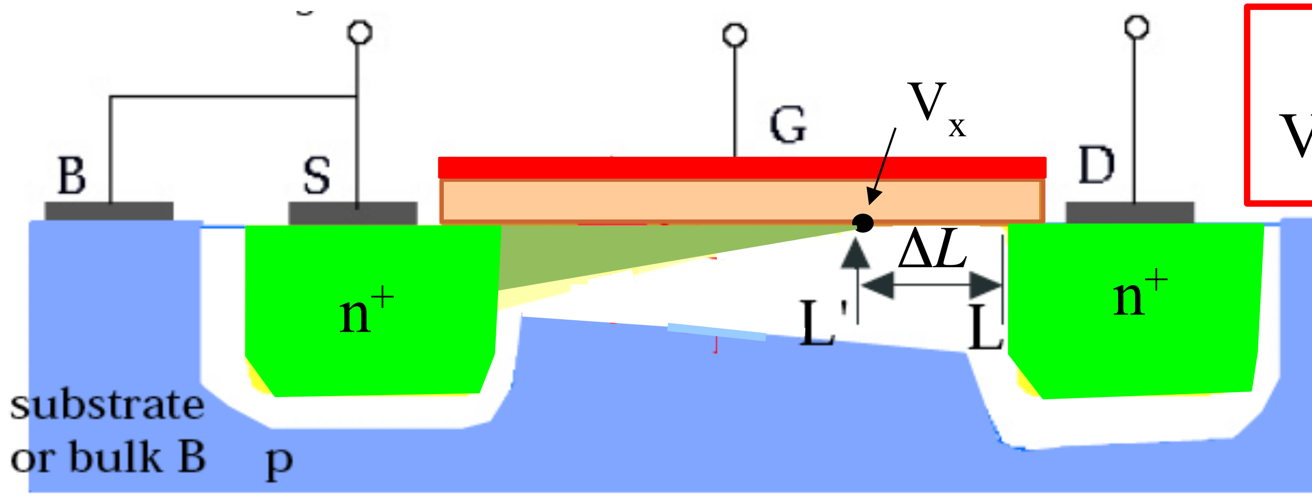
$$V_{GS} > V_{T0}$$
$$V_{DS} > V_{GS} - V_{T0}$$

$$I_{DS} = \frac{\mu_n \cdot C_{ox}}{2}\frac{W}{L'}\left(V_{GS}-V_{T0}\right)^2 = \frac{\mu_n \cdot C_{ox}}{2}\frac{W}{L-\Delta L}\left(V_{GS}-V_{T0}\right)^2$$

$$= \frac{\mu_n \cdot C_{ox}}{2}\frac{W}{L\left(1-\frac{\Delta L}{L}\right)}\left(V_{GS}-V_{T0}\right)^2$$

$$= \frac{\mu_n \cdot C_{ox}}{2}\frac{W}{L}\left(V_{GS}-V_{T0}\right)^2\frac{1}{\left(1-\frac{\Delta L}{L}\right)}$$

MOSFET IV Characteristics - Saturation

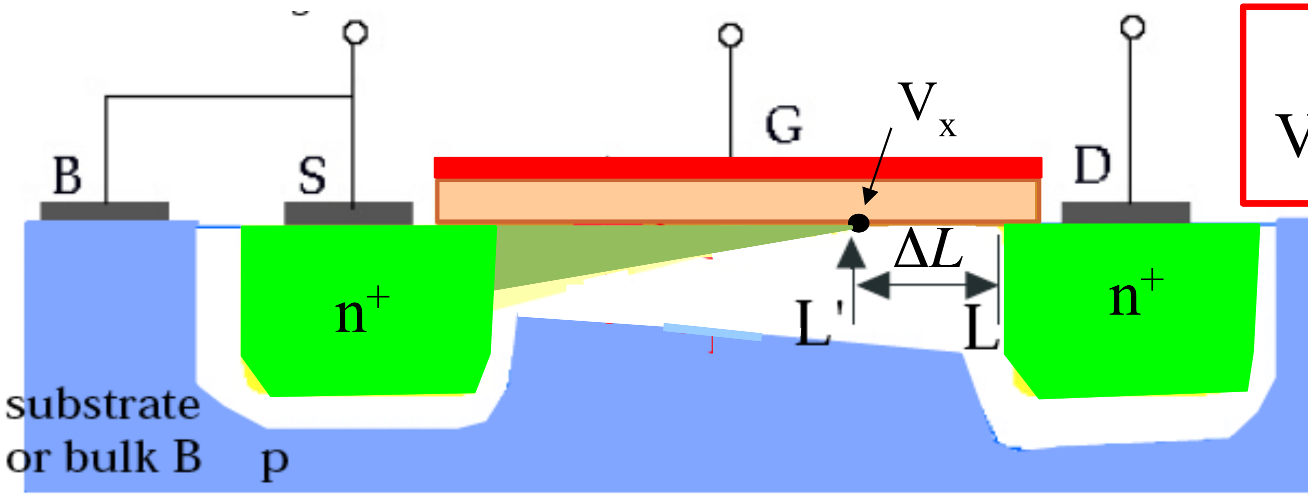


$V_{GS} > V_{T0}$
$V_{DS} > V_{GS} - V_{T0}$

$$I_{DS} = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_{T0}\right)^2 \frac{1}{\left(1 - \frac{\Delta L}{L}\right)}$$

$$\Delta L \propto \sqrt{V_{DS} - (V_{GS} - V_{T0})} \xrightarrow{\text{empirically}} 1 - \frac{\Delta L}{L} \approx 1 - \lambda \cdot V_{DS}$$

MOSFET IV Characteristics - Saturation



$V_{GS} > V_{T0}$
$V_{DS} > V_{GS} - V_{T0}$

$$I_{DS} = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_{T0}\right)^2 \frac{1}{\left(1 - \frac{\Delta L}{L}\right)}$$

$$\Delta L \propto \sqrt{V_{DS} - (V_{GS} - V_{T0})} \quad \xrightarrow{\text{empirically}} \quad 1 - \frac{\Delta L}{L} \approx 1 - \lambda \cdot V_{DS}$$

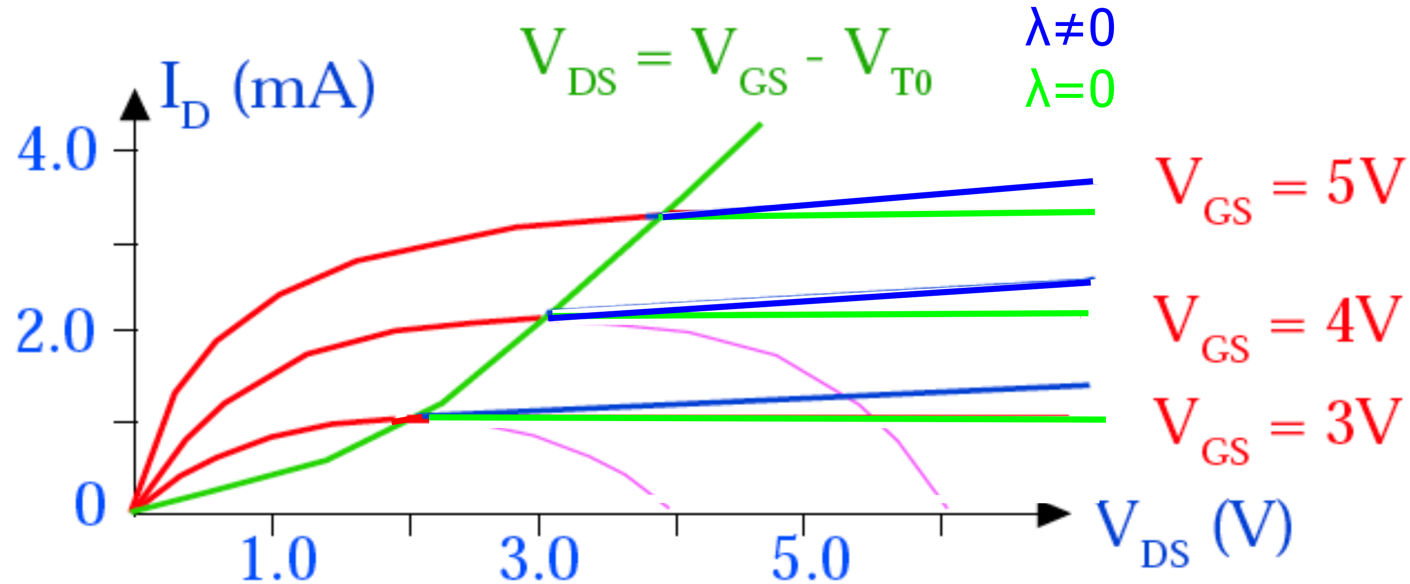
If $\lambda \cdot V_{DS} << 1$,

$$\left(1 - \frac{\Delta L}{L}\right)^{-1} \approx \boxed{1 + \lambda \cdot V_{DS}}$$

MOSFET IV Characteristics

Linear Region: $$I_D = \mu_n \cdot C_{ox} \frac{W}{L}\left((V_{GS} - V_{T0})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Saturation Region: $$I_D = \frac{\mu_n \cdot C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{T0}\right)^2 (1 + \lambda \cdot V_{DS})$$



MOSFET IV Characteristics

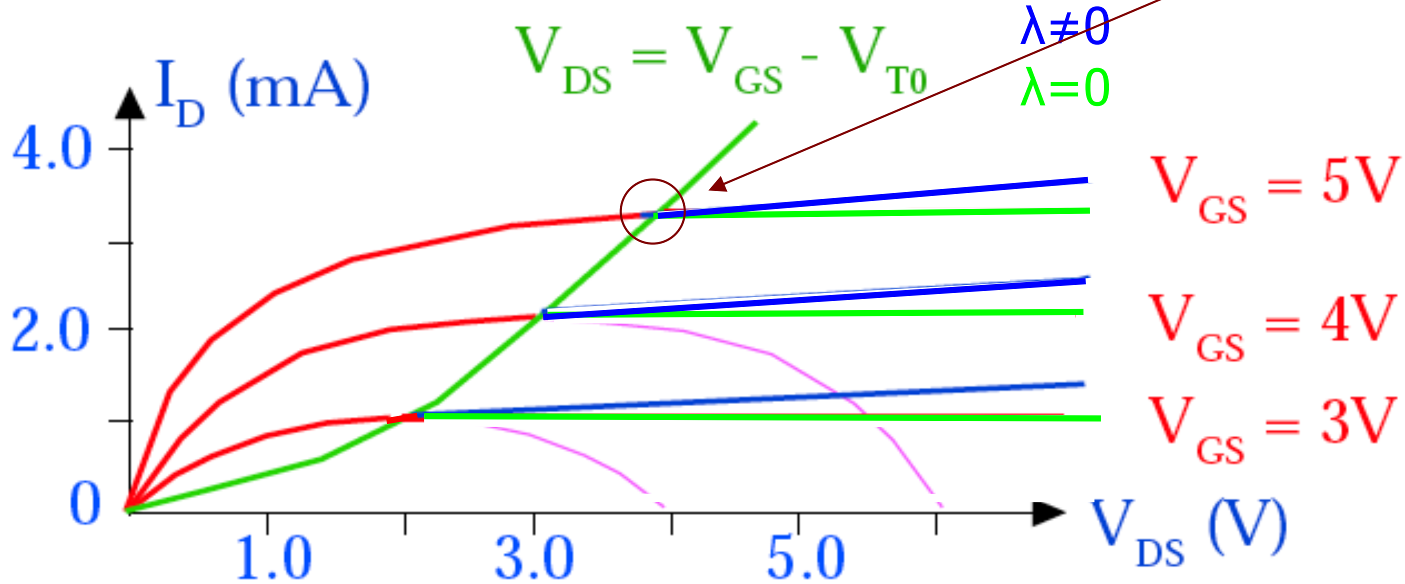
Linear Region:

$$I_D = \mu_n \cdot C_{ox} \frac{W}{L}\left((V_{GS} - V_{T0})V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Saturation Region:

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L}\left(V_{GS} - V_{T0}\right)^2 (1 + \lambda \cdot V_{DS})$$

DISCONTINUOUS!
@ $V_{DS} = V_{GS} - V_T$



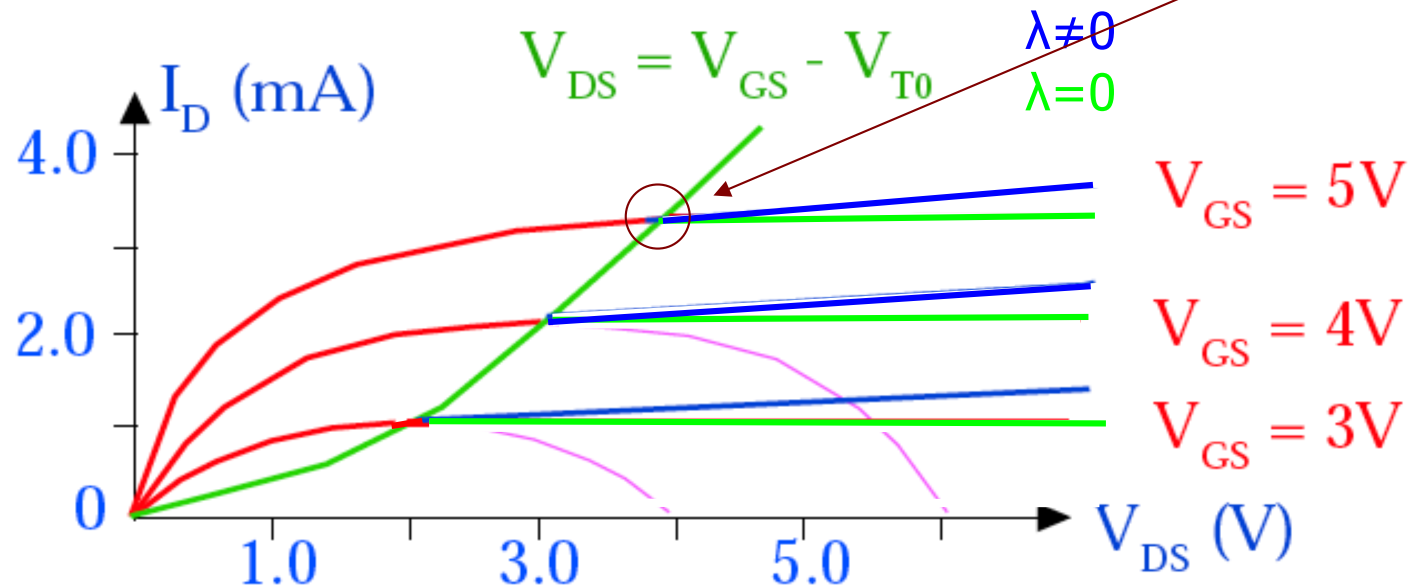
MOSFET IV Characteristics

Linear Region: $I_D = \mu_n \cdot C_{ox} \frac{W}{L}\left((V_{GS} - V_{T0})V_{DS} - \frac{V_{DS}^2}{2}\right)(1 + \lambda \cdot V_{DS})$

Saturation Region: $I_D = \frac{\mu_n \cdot C_{ox}}{2} \frac{W}{L}\left(V_{GS} - V_{T0}\right)^2 (1 + \lambda \cdot V_{DS})$

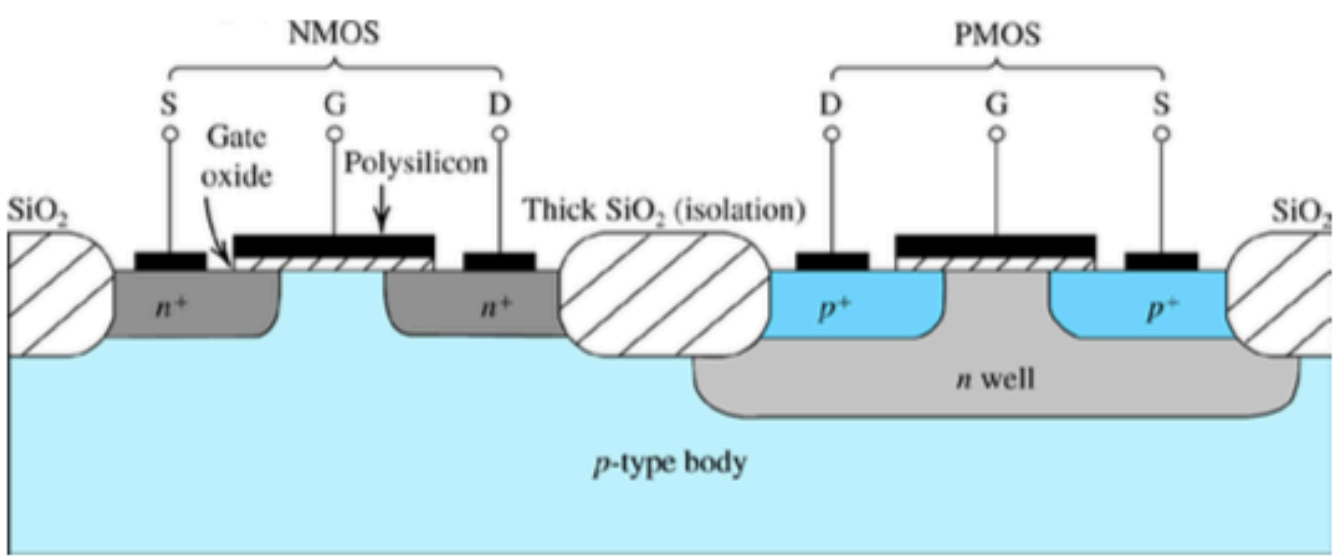
~~DIS~~CONTINUOUS!

@ $V_{DS} = V_{GS} - V_T$



pMOS Device

- Analogous phenomena to NMOS
- Opposite polarity
  - Negative V_{th}, λ
- Reason based on oppositely charged carriers

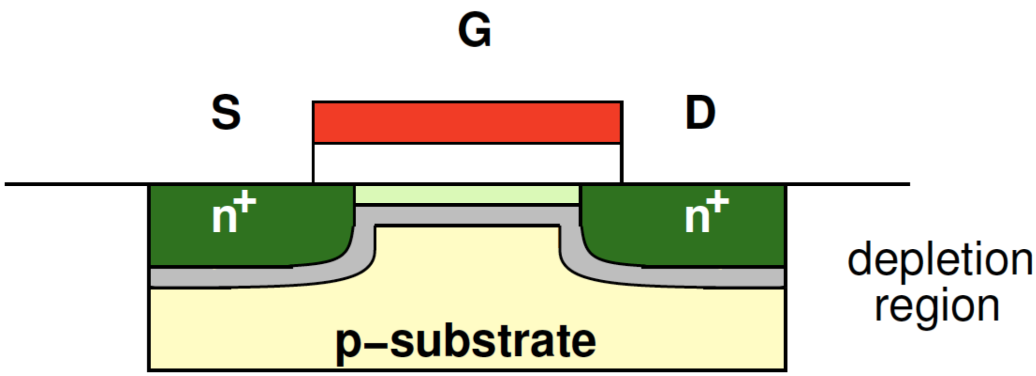


To summarize

Above Threshold

Linear Region

- $V_{GS} > V_{th}$ and V_{DS} small



$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$I_{DS} = \mu_n C_{OX} \left(\frac{W}{L}\right)\left[\left(V_{GS} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Saturation

- In saturation, $V_{DS\text{-effective}} = V_x = V_{GS} - V_T$

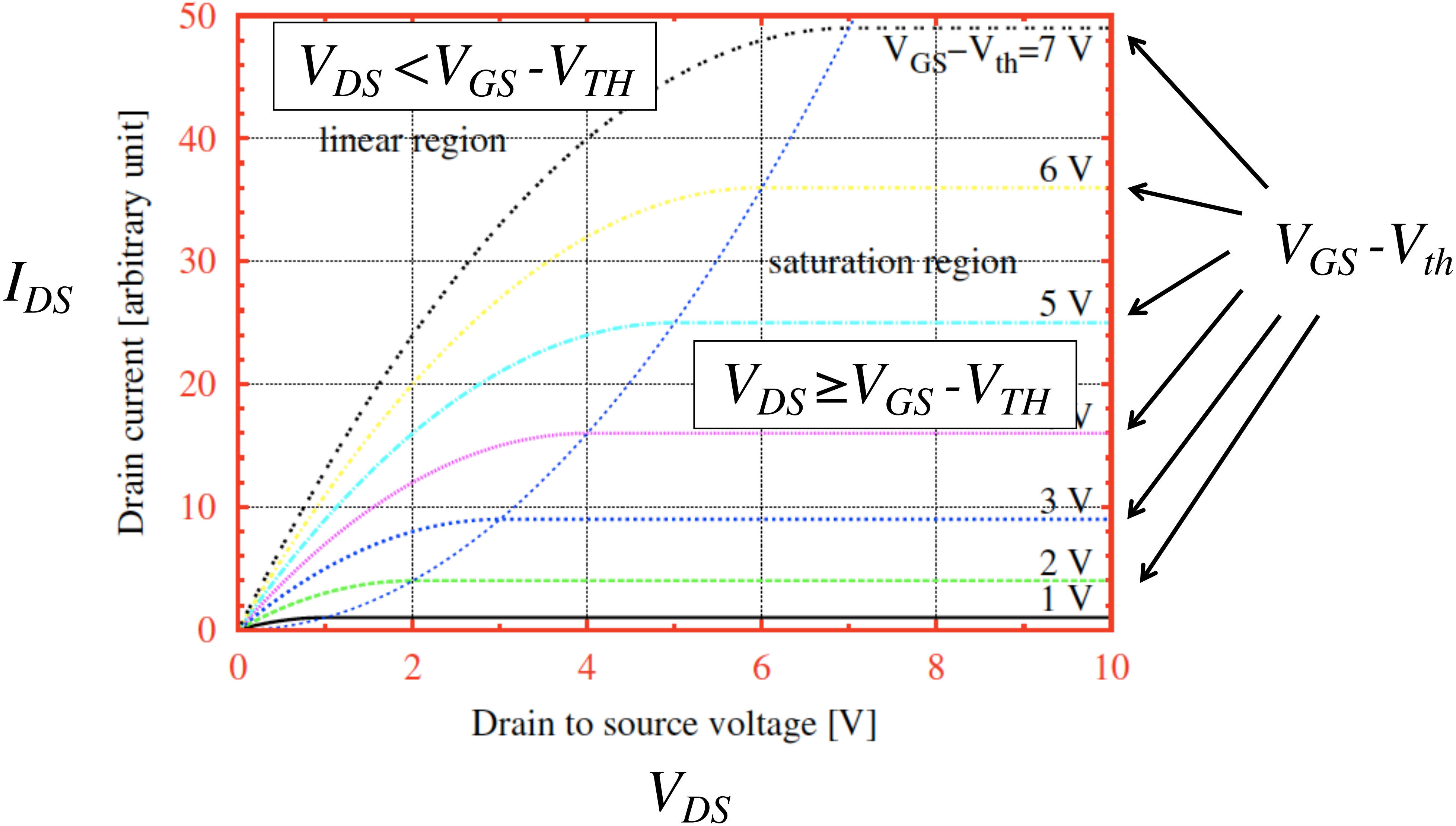
$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- Becomes:

$$I_{DS} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)^2 - \frac{\left(V_{GS} - V_T\right)^2}{2}\right]$$

$$\boxed{I_{DS} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)\left[\left(V_{GS} - V_T\right)^2\right]}$$

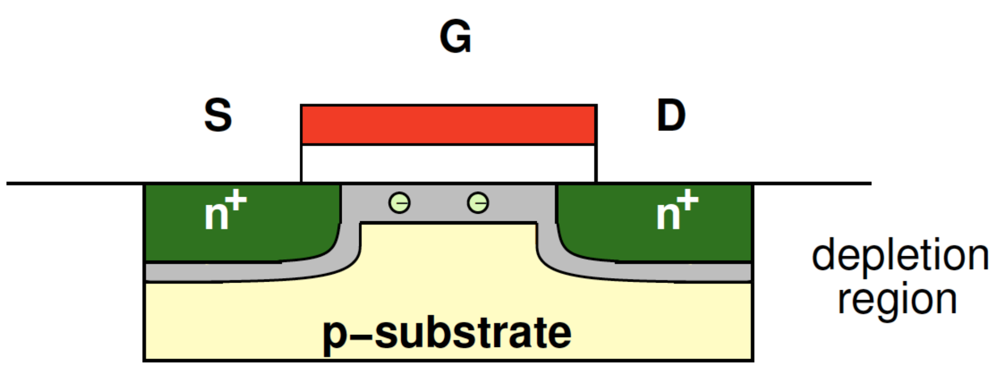
MOSFET – IV Characteristics

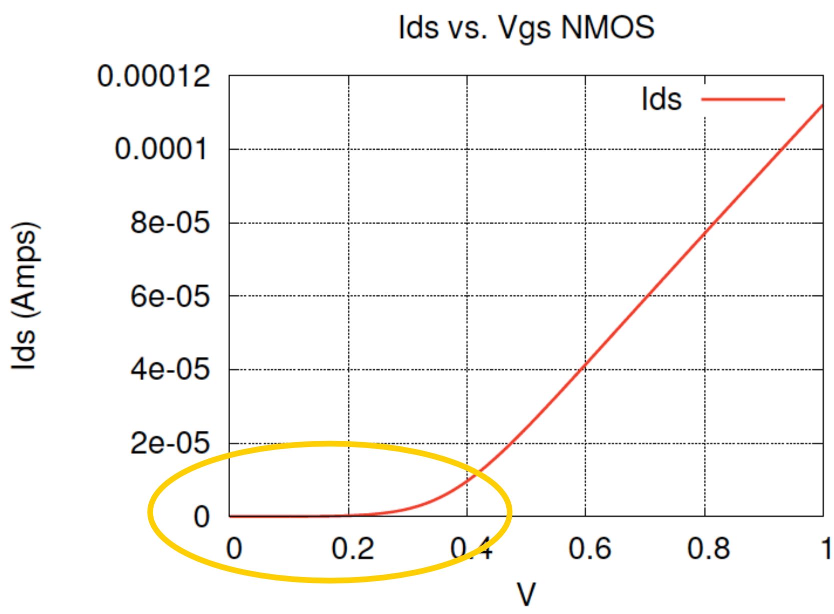


Subthreshold

Below Threshold

- Transition from insulating to conducting is non-linear, but not abrupt
- Current does flow
  - But exponentially dependent on V_{GS}





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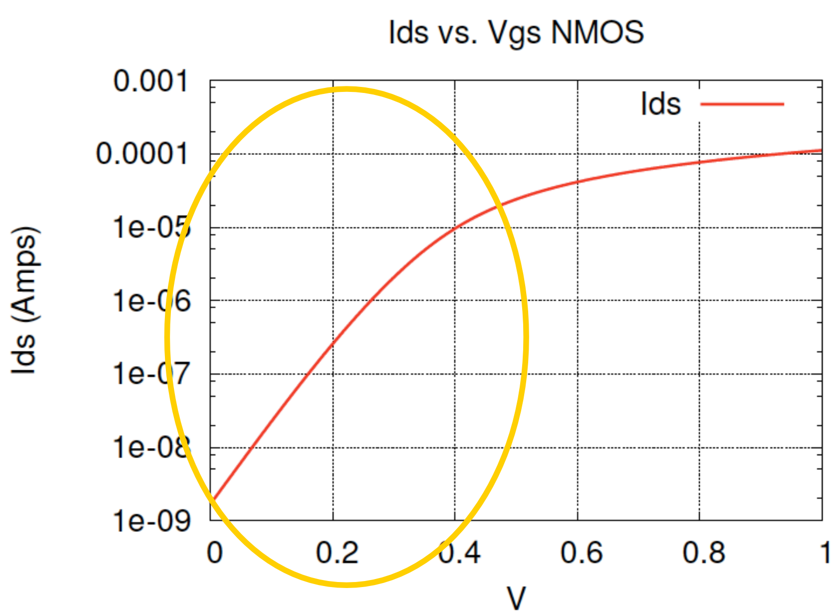
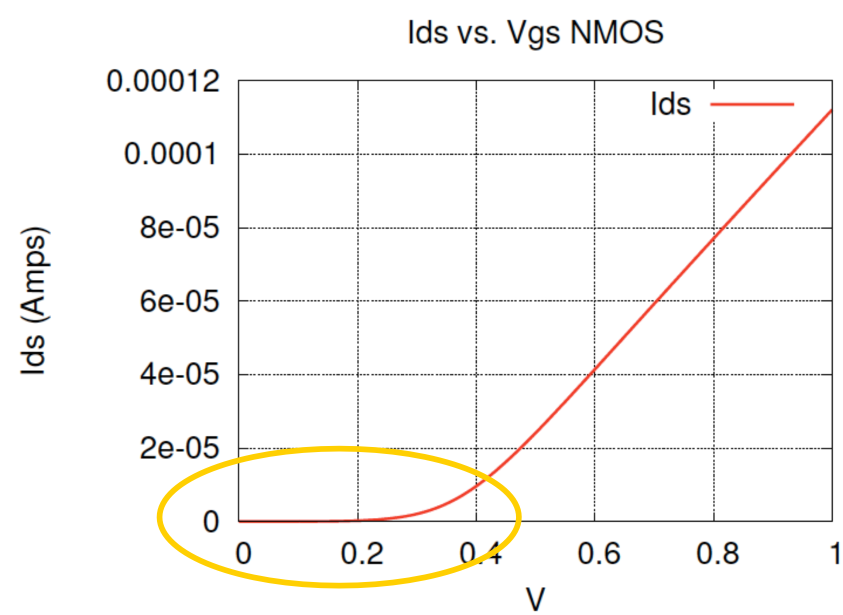
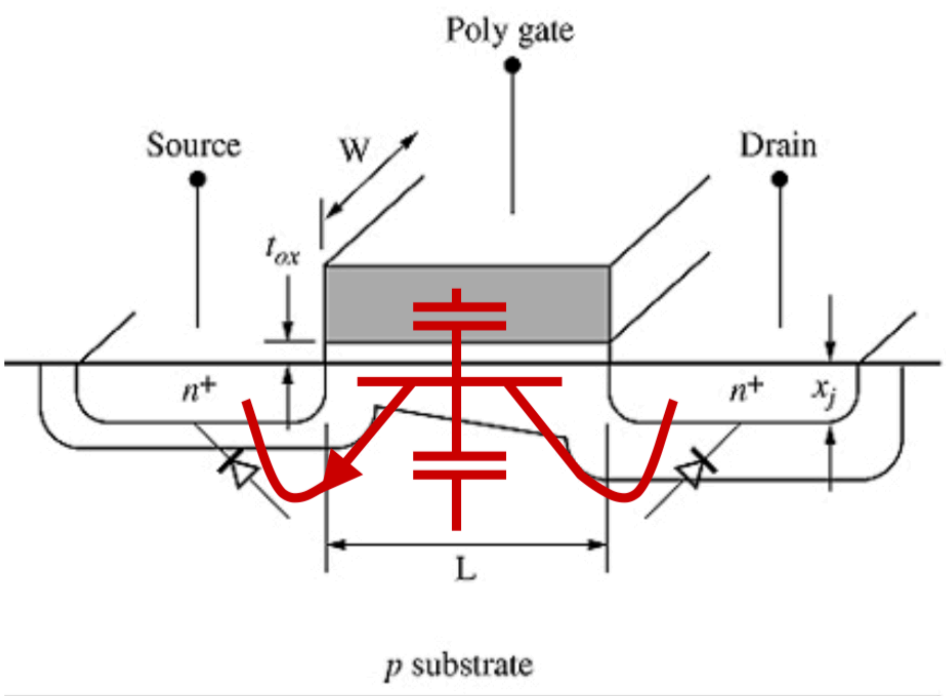




Parasitic NPN BJT

- We have an NPN sandwich, mobile minority carriers in the P region
- This is a BJT!
  - Except that the base potential is here controlled through a capacitive divider, and not directly an electrode



Subthreshold

$$\text{If} \quad V_{GS} < V_{th},$$

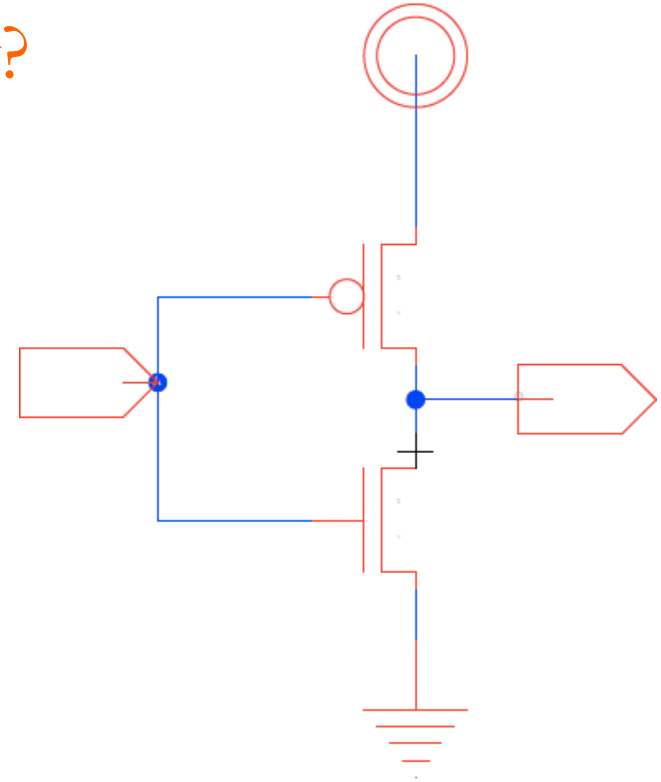
$$I_{DS} = I_S \left(\frac{W}{L}\right) e^{\left(\frac{V_{GS}-V_{th}}{nkT/q}\right)}$$

- Current is from the parasitic NPN BJT transistor when gate is below threshold and there is no conducting channel
  - n is the capacitive divider between parasitic capacitances
  - Typically 1 < n < 1.5

$$n = \frac{C_{js} + C_{ox}}{C_{ox}}$$

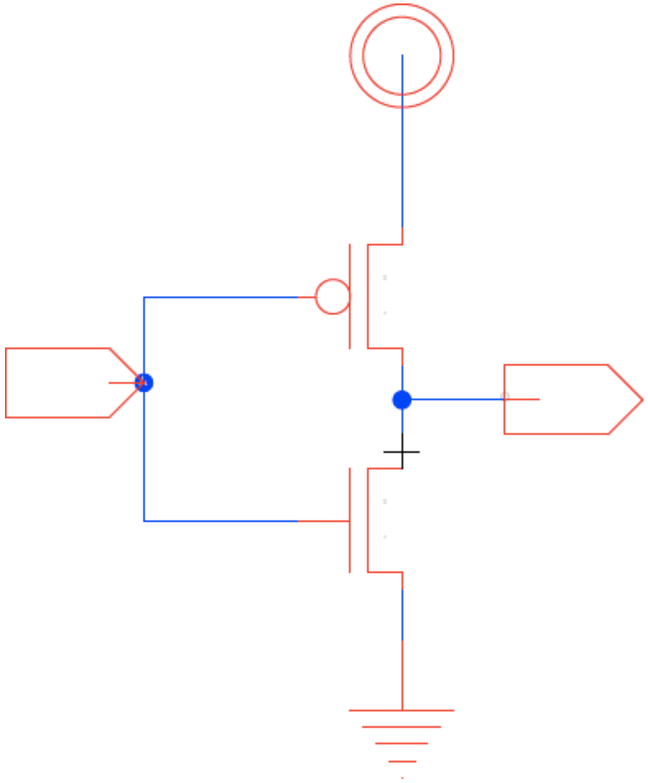
Steady State (Preclass 4)

- What current flows in steady state?
- What causes (and determines) the magnitude of current flow?
- Which device?



Leakage

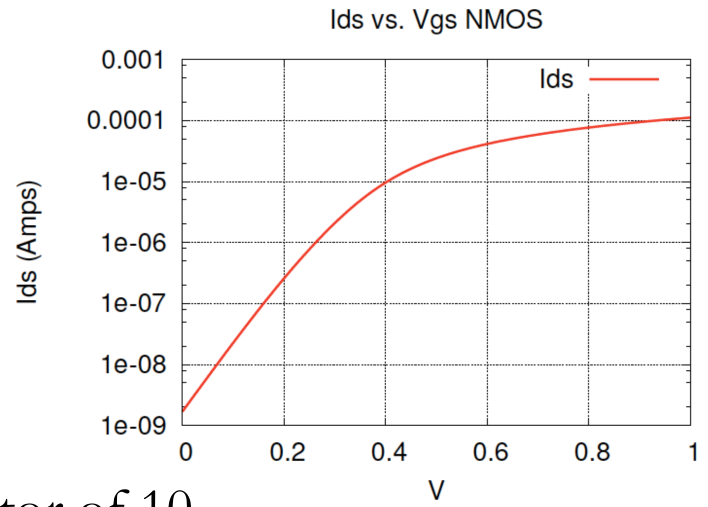
- Call this steady-state current flow leakage
  - $I_{ds,leakage}$



Subthreshold Slope Factor

- Exponent in V_{GS} determines how steep the turnon is

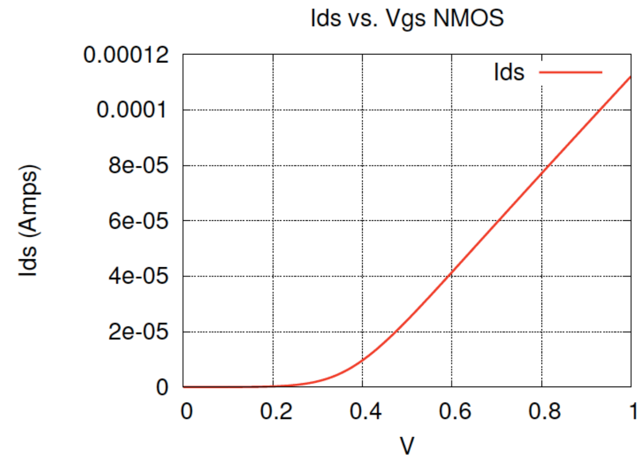
$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

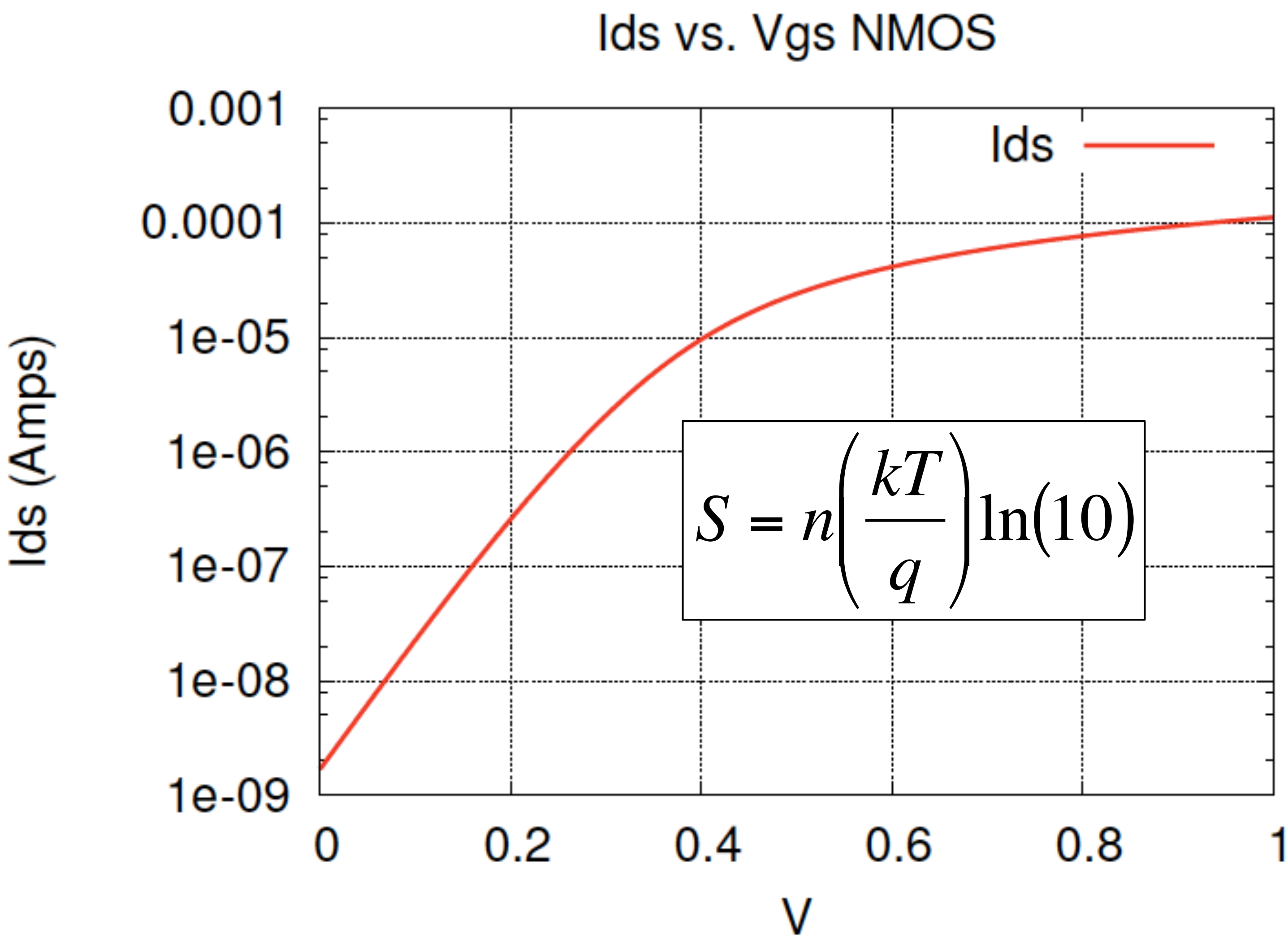


  - Units: V/decade
    - Every S Volts, I_{DS} is scaled by factor of 10

$$I_{DS} = I_S\left(\frac{W}{L}\right)e^{\left(\frac{V_{GS}-V_{th}}{nkT/q}\right)}$$

I_{DS} vs. V_{GS}





$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

(Logscale)

Subthreshold Slope Factor

- Exponent in V_{GS} determines how steep the turnon is

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

  - Units: V/dec
  - Every S Volts, I_{DS} is scaled by factor of 10

- n – depends on parasitic capacitance divider

$$n = \frac{C_{js} + C_{ox}}{C_{ox}}$$

  - n=1 → S=60mV at Room Temp. (ideal)
  - n=1.5 → S=90mV
  - Single gate structure showing S=90-110mV

Subthreshold Slope Factor (Preclass 5)

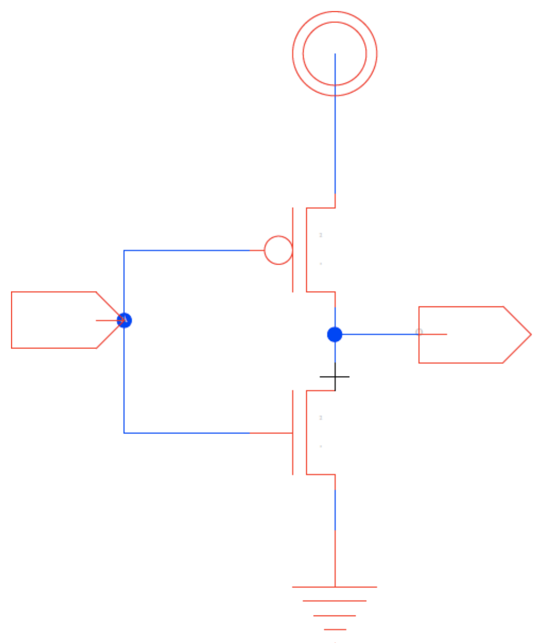
- If S=100mV and V_{th}=300mV,
  what is Ids(Vgs=300mV)/Ids(Vgs=0V) ?

- What if S=60mV?

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

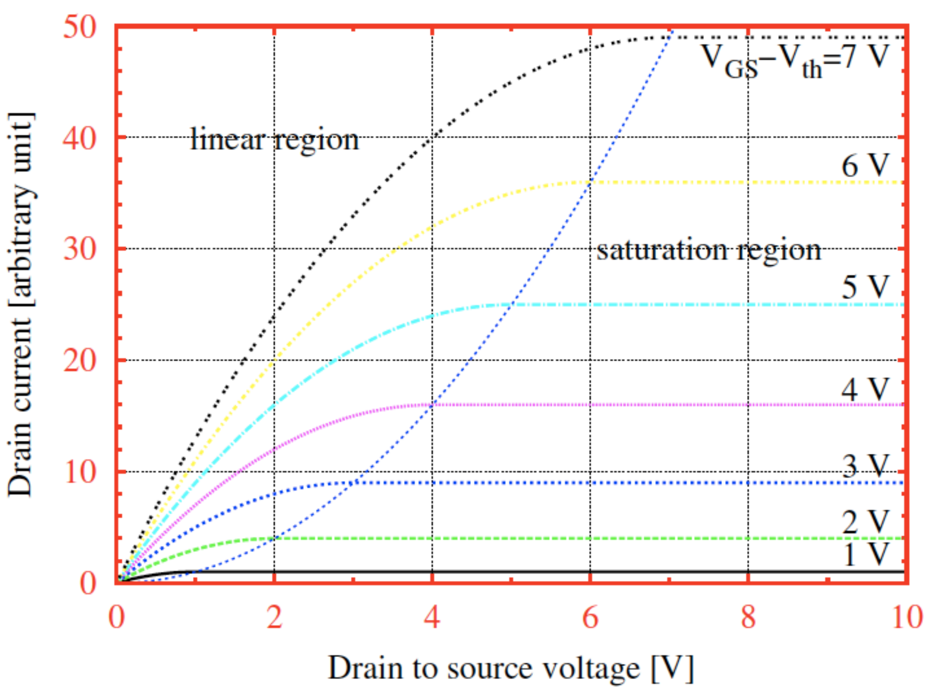
Approach

- Identify Region
- Understand governing equations
- Use region and equations to understand operation



Big Idea

- Semiconductor can act like metal or insulator
- Use electric field to modulate conduction state of semiconductor
- 3 Regions of operation for MOSFET
  - Linear
  - Saturation
    - With channel length modulation
  - Subthreshold



Admin

- HW 2 due 2/3 (Friday)

- More Fabrication Videos:
  - From sand to silicon (intel) - https://www.youtube.com/watch?v=Q5paWn7bFg4
  - How microchips are made - https://www.youtube.com/watch?v=F2KcZGwntgg

Acknowledgement

- Prof. André DeHon (University of Pennsylvania)
- Prof. Tania Khanna (University of Pennsylvania)

Background Reading (Optional)

Semiconductor Physics

Conduction

- Metal – conducts
- Insulator – does not conduct
- Semiconductor – can act as either

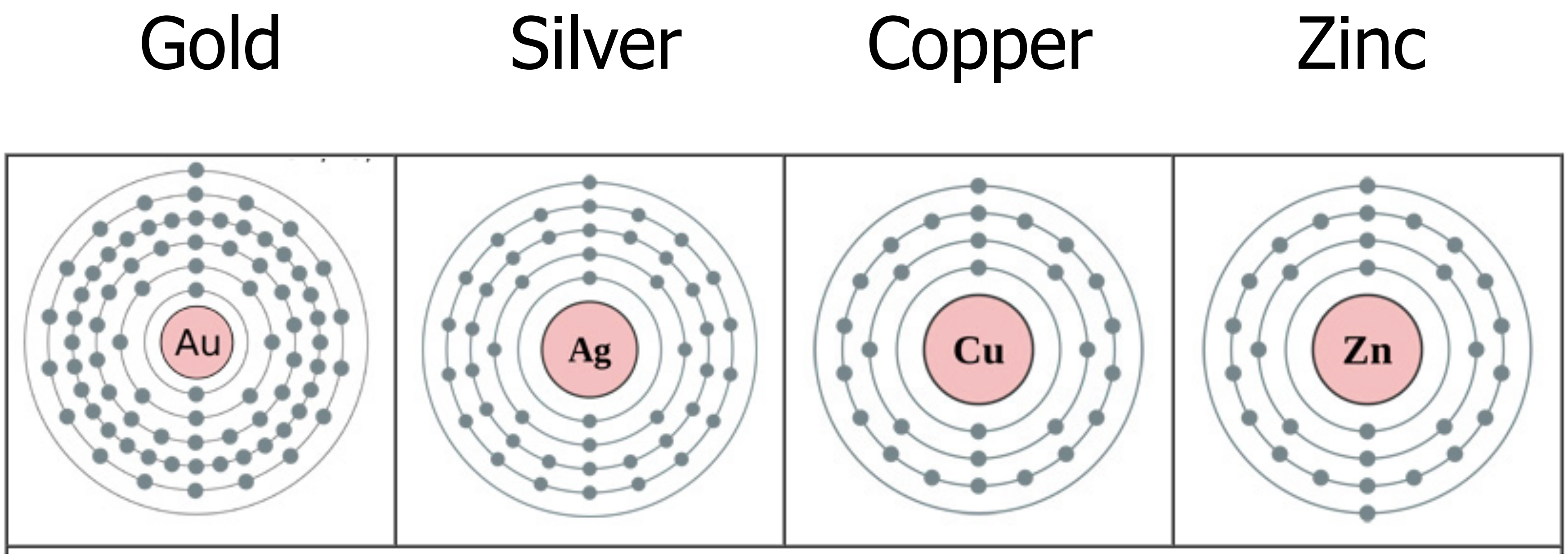
Why does metal conduct? (preclass 2)

Group → / ↓Period	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
1	1 H																	2 He
2	3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
3	11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
4	19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
5	37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
6	55 Cs	56 Ba		72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
7	87 Fr	88 Ra		104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 UUb	113 Uut	114 Uuq	115 Uup	116 Uuh	117 Uus	118 Uuo

Lanthanides	57 La	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu
Actinides	89 Ac	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr

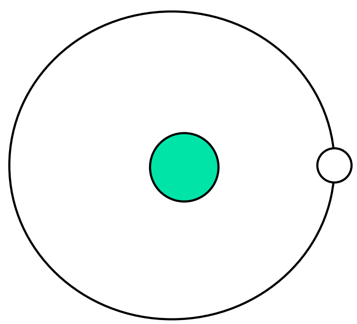
http://chemistry.about.com/od/imagesclipartstructures/ig/Science-Pictures/Periodic-Table-of-the-Elements.htm

Why does metal conduct? (preclass 2)



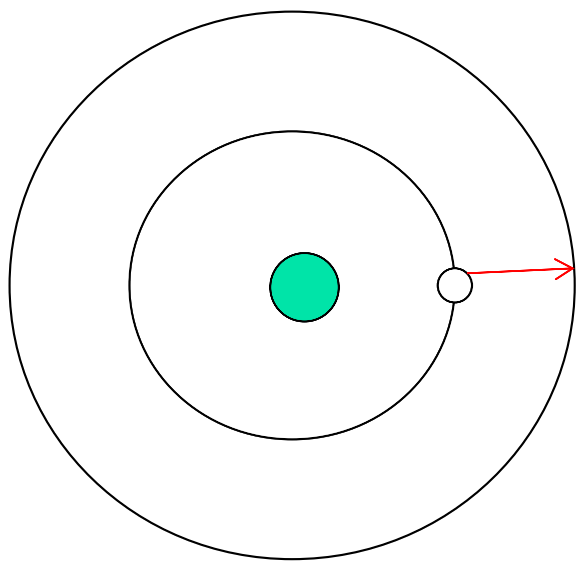
Conduction

- Electrons move
- Must be able to "remove" electron from atom or molecule



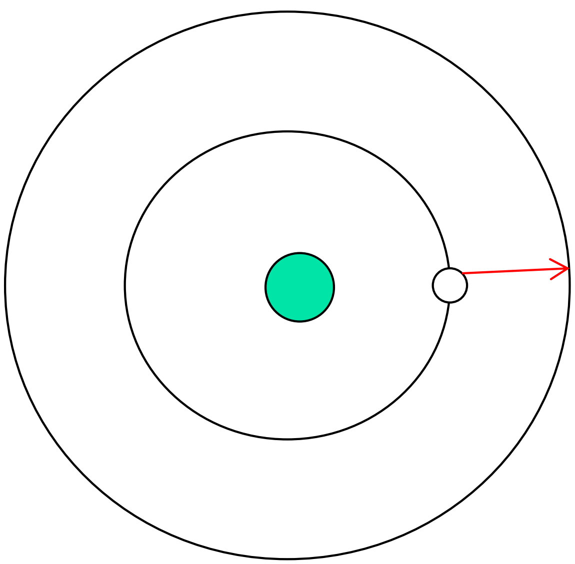
Atomic States

- Quantized Energy Levels (bands)
  - Valence and Conduction Bands
- Must have enough energy to change level (state)



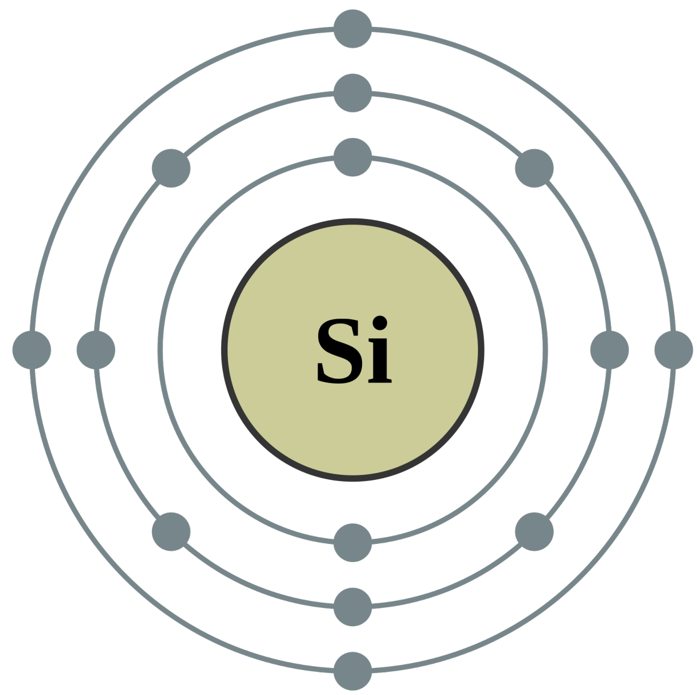
Thermal Energy

- Except at absolute 0
  - There is always free energy
  - Causes electrons to hop around
    - ….when there is enough energy to change states
  - Energy gap between states determines energy required



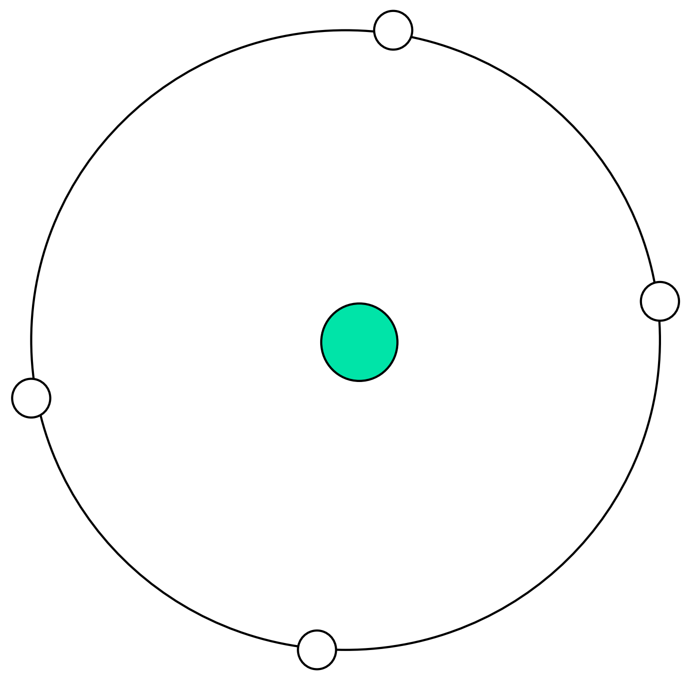
Silicon Atom (preclass 3)

- How many valence electrons?



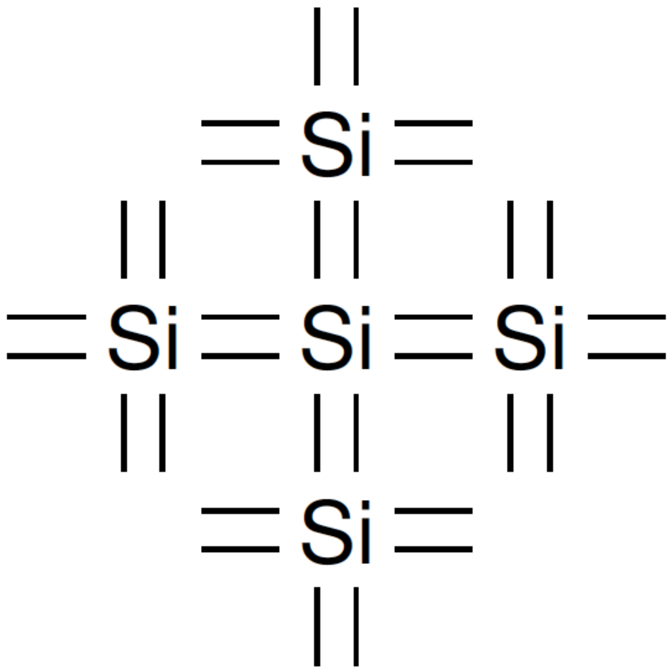
Silicon

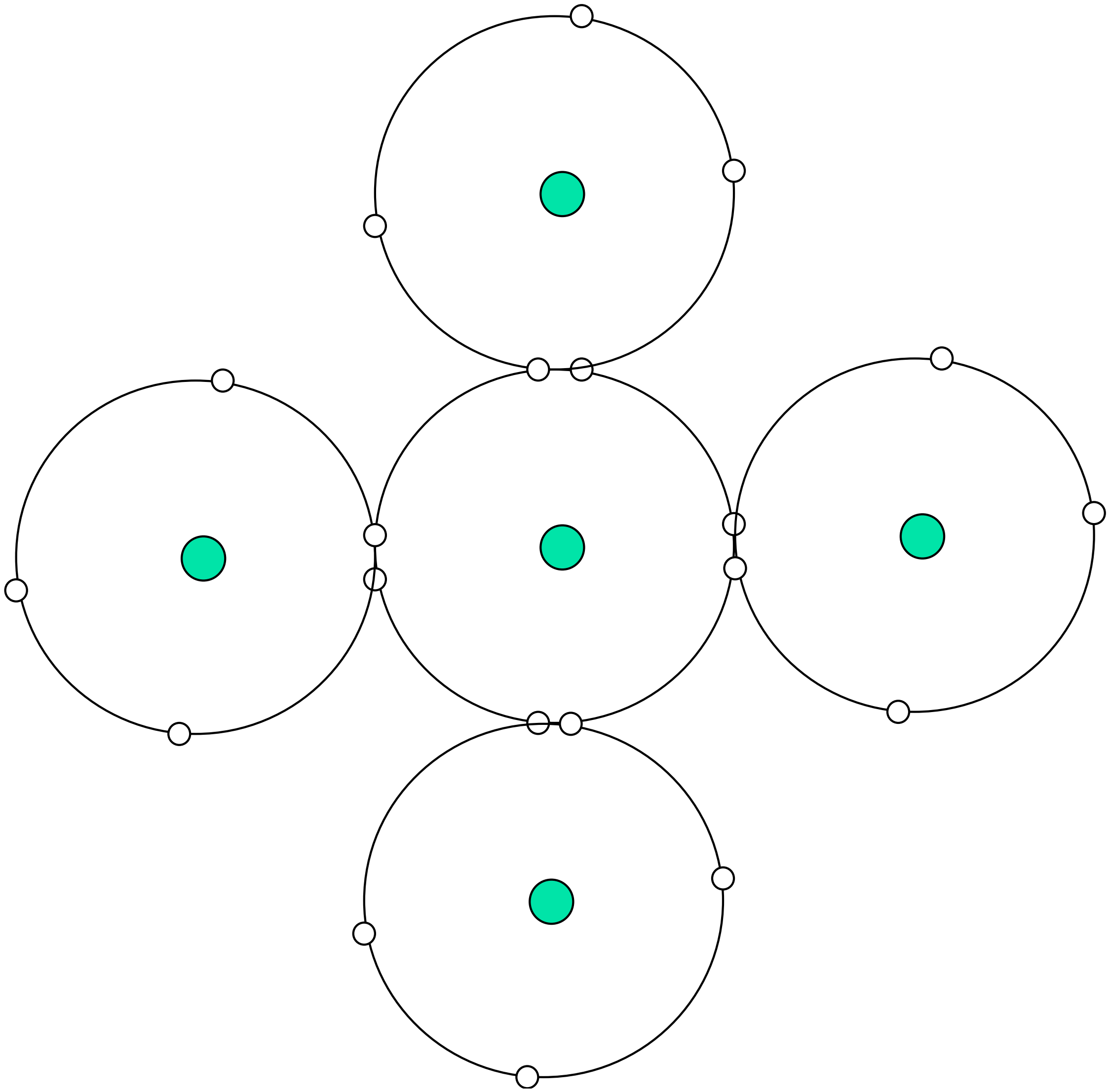
- 4 valence electrons
  - Inner shells filled
  - Only outer shells contribute to chemical interactions



Silicon-Silicon Bonding

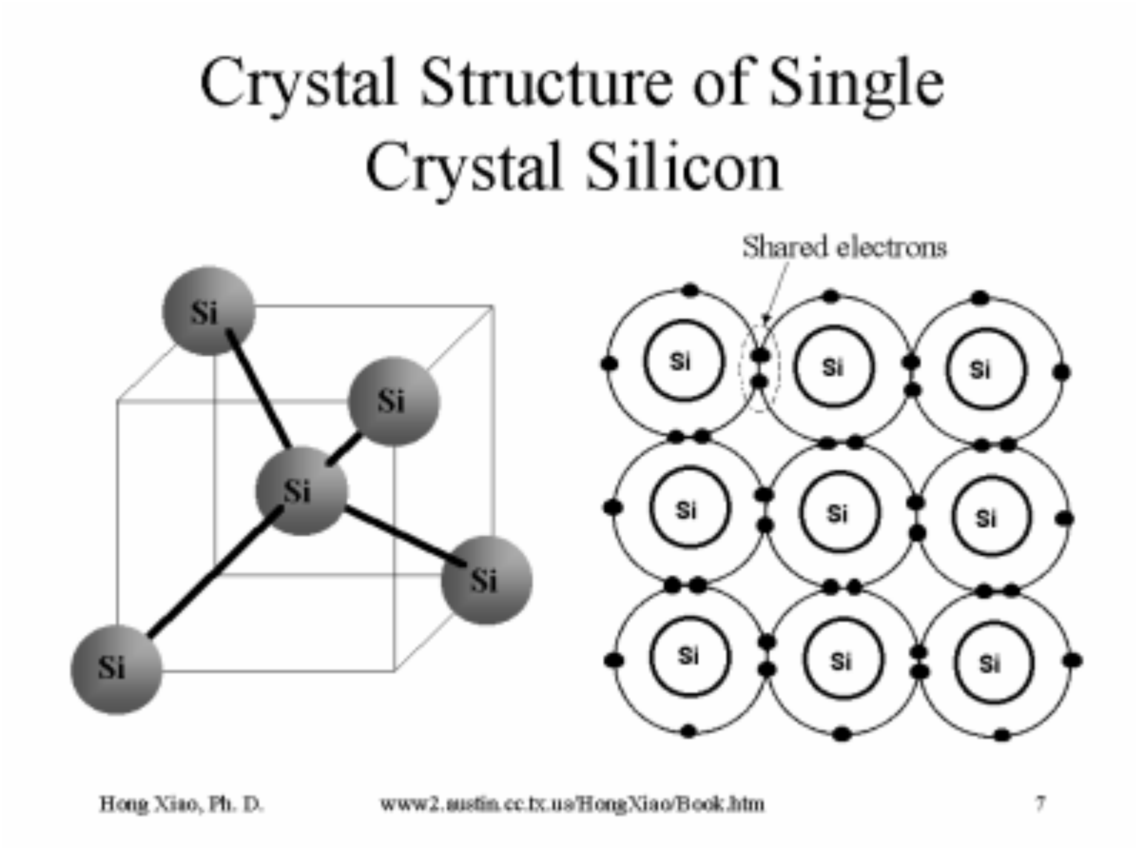
- Can form covalent bonds with 4 other silicon atoms

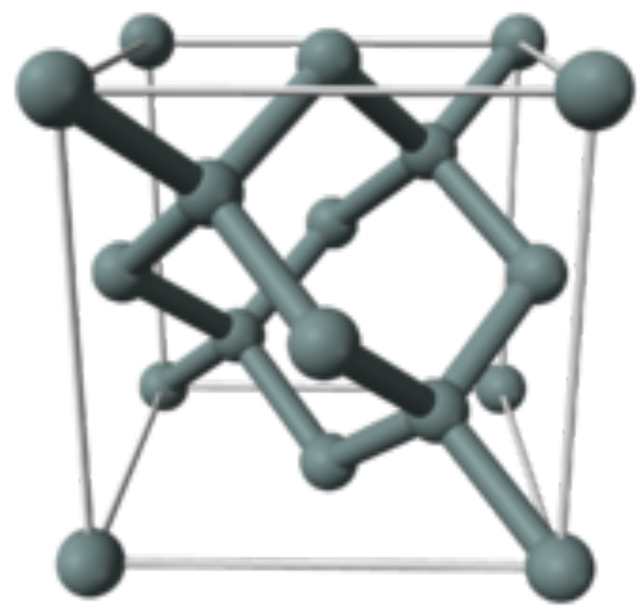




Silicon Lattice

- Forms into crystal lattice



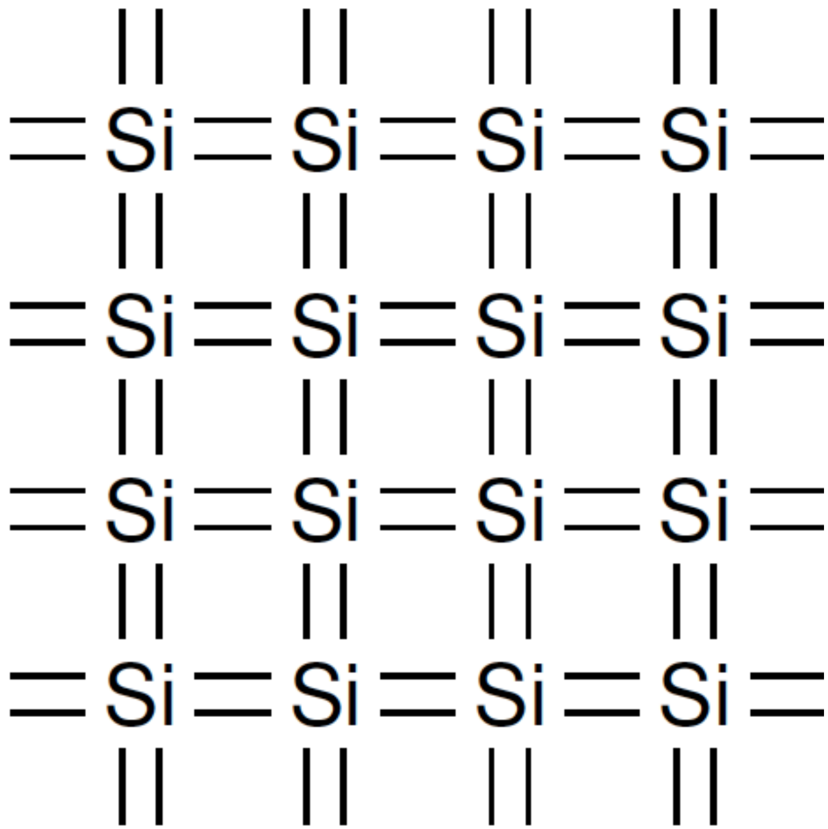


Silicon Ingot

1 impurity atom per 10 billion silicon atoms

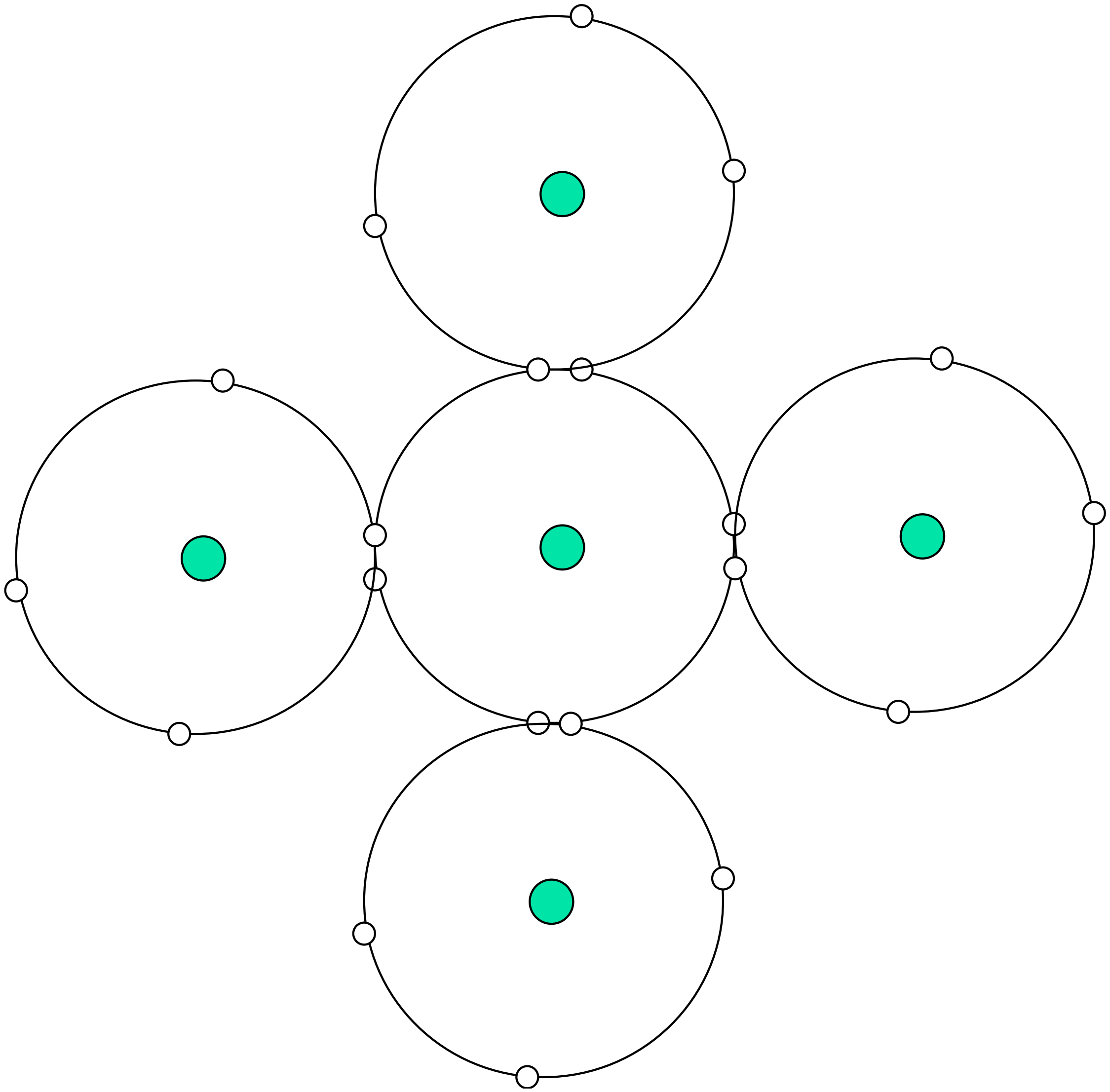
Silicon Lattice

- Cartoon two-dimensional view



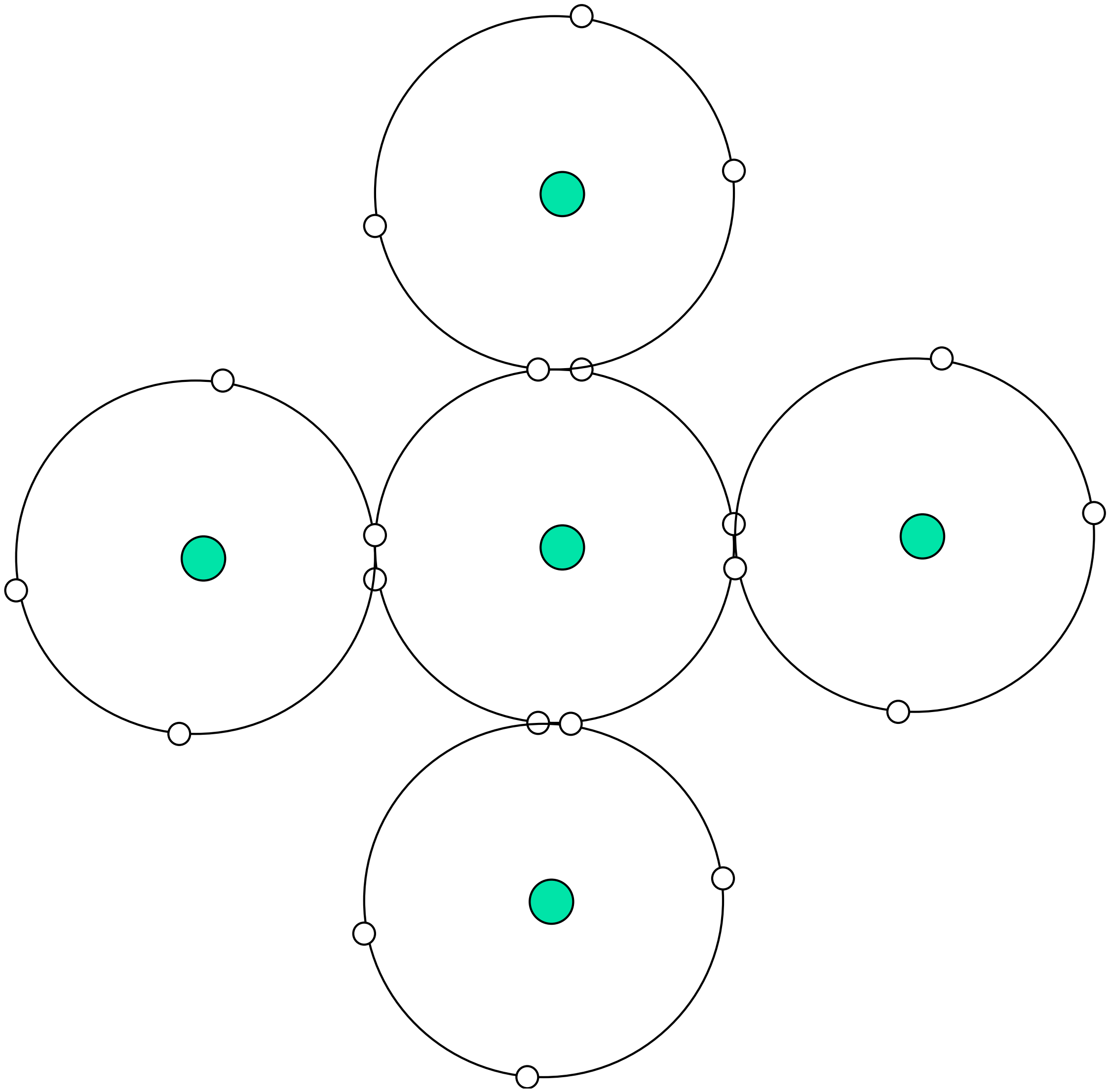
Outer Orbital?

- What happens to outer shell in Silicon lattice?



Energy?

- What does this say about energy to move electron?



Energy State View

Energy

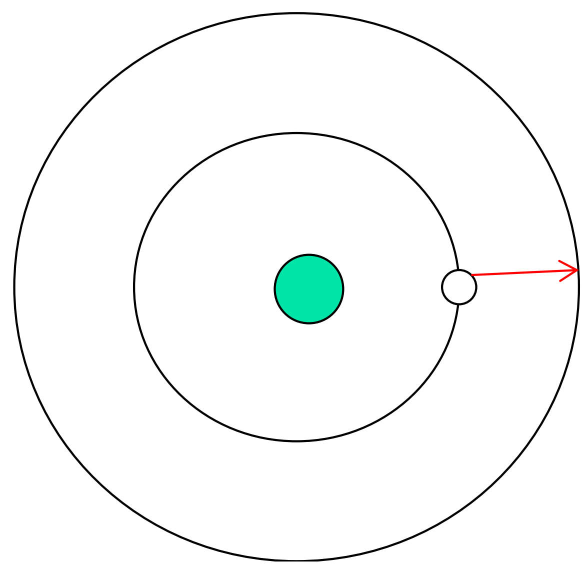
Valance Band – all states filled

Energy State View

Conduction Band– all states empty

Energy

Valance Band – all states filled



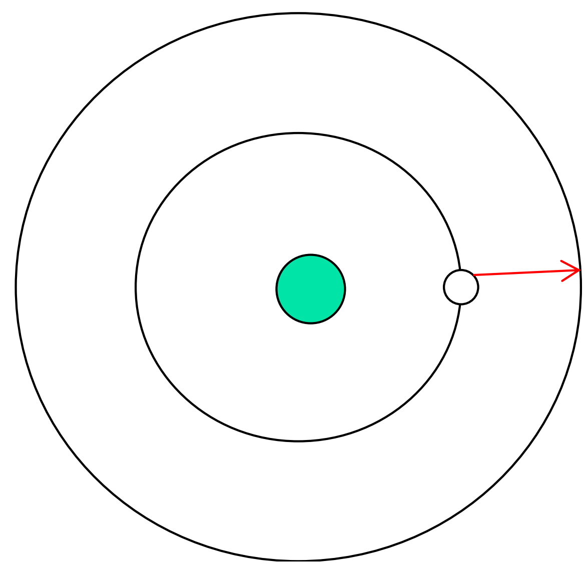
Energy State View

Conduction Band– all states empty

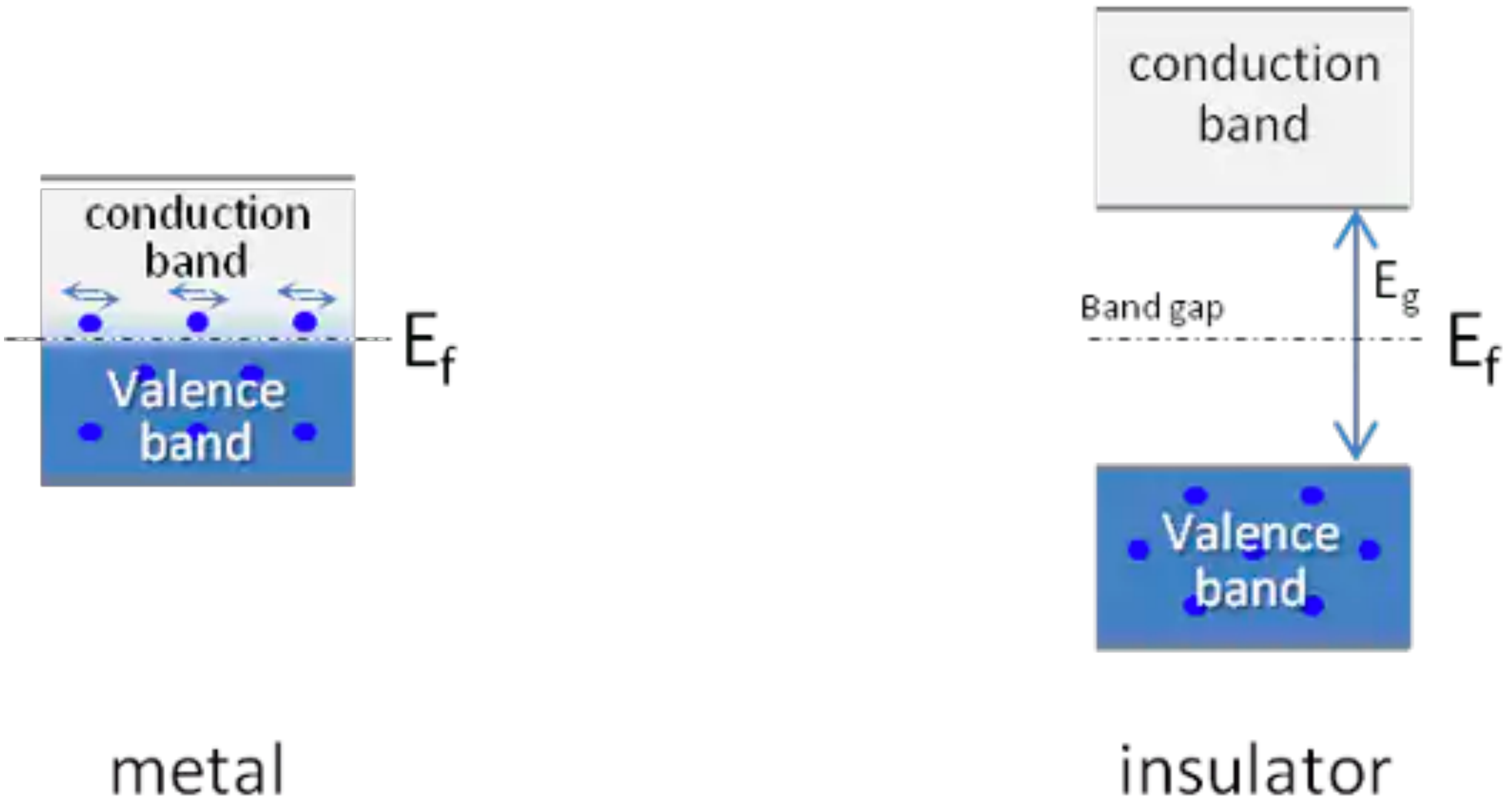
Energy

Band Gap

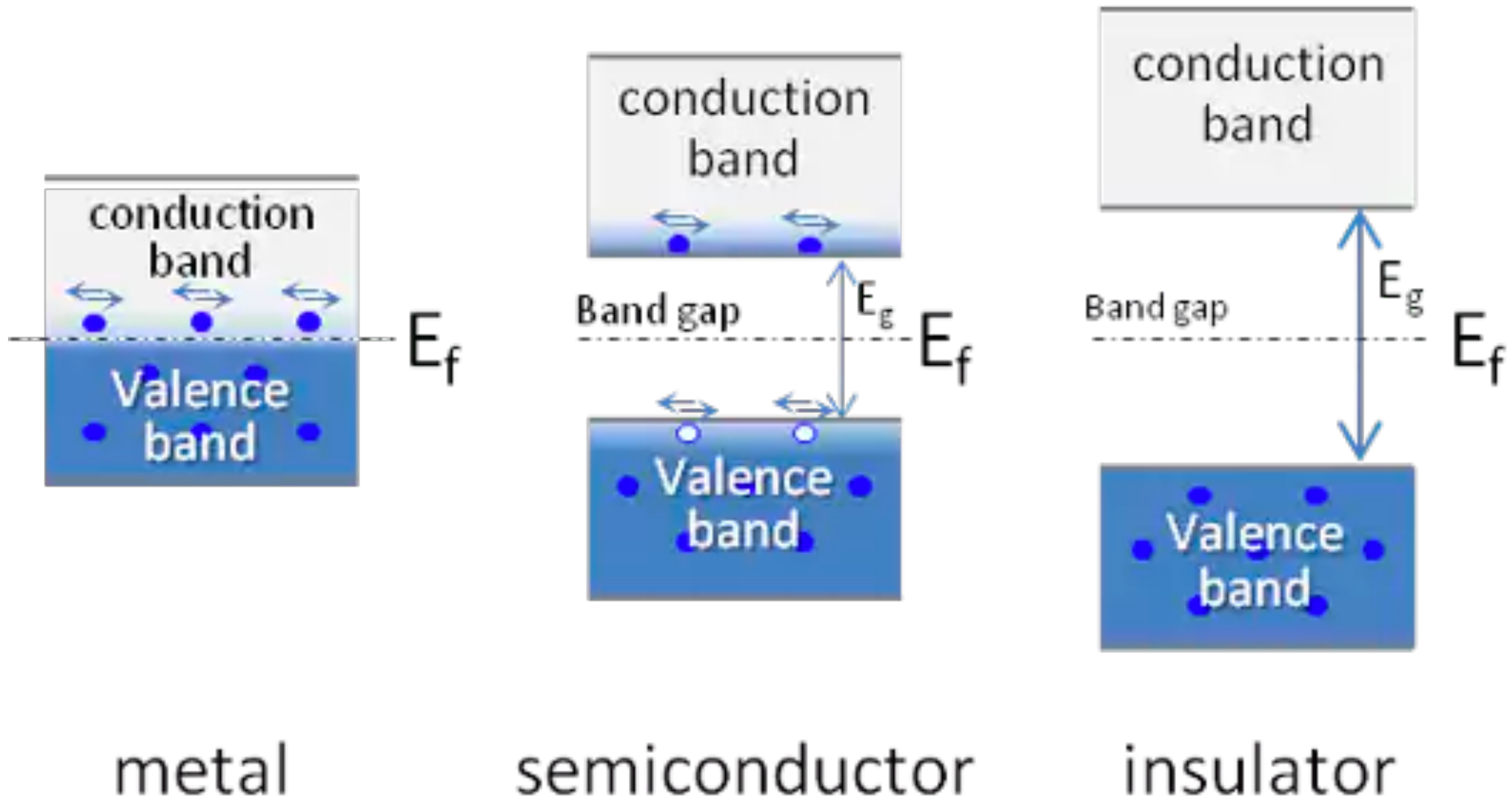
Valance Band – all states filled



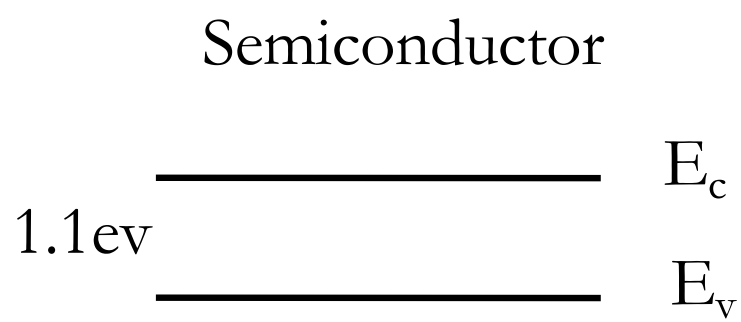
Band Gap and Conduction



Band Gap and Conduction



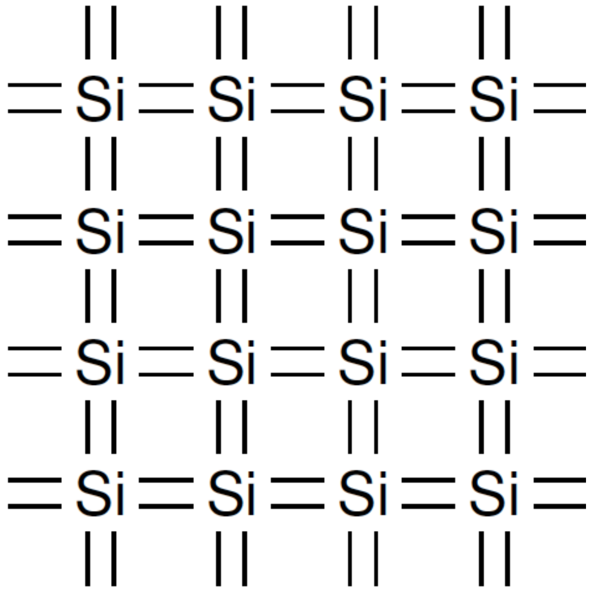
Band Gap and Conduction

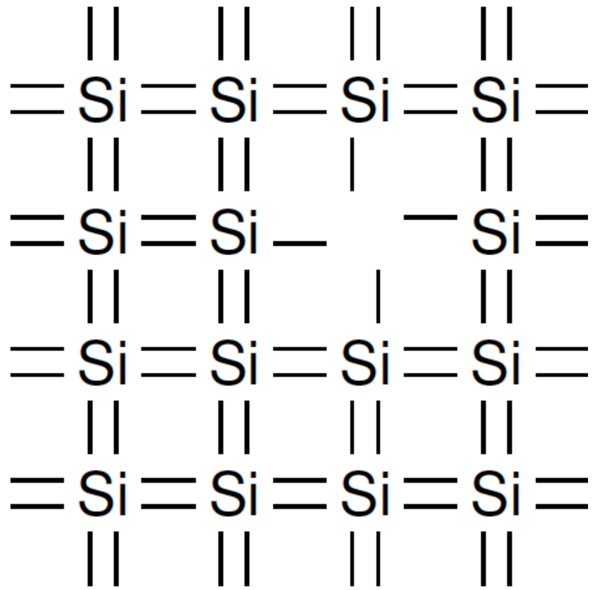


1eV = 160 zeptojoules (10^{-21} J)

Doping

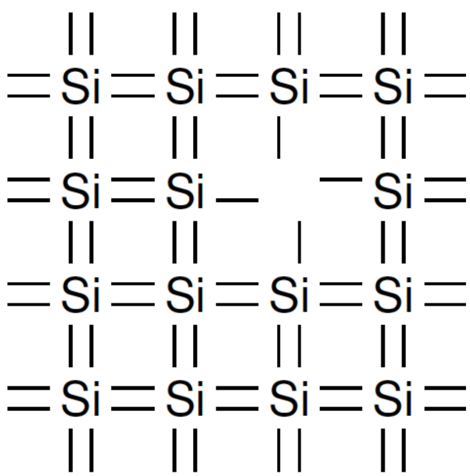
- Add impurities to Silicon Lattice
  - Replace a Si atom at a lattice site with another

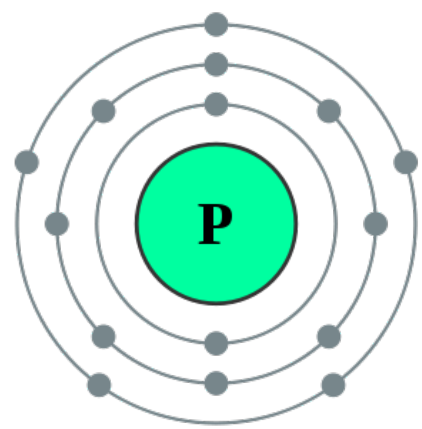




Doping

- Add impurities to Silicon Lattice
  - Replace a Si atom at a lattice site with another
- Add a Group 15 element
  - *E.g.* P (Phosphorus)
  - How many valence electrons?





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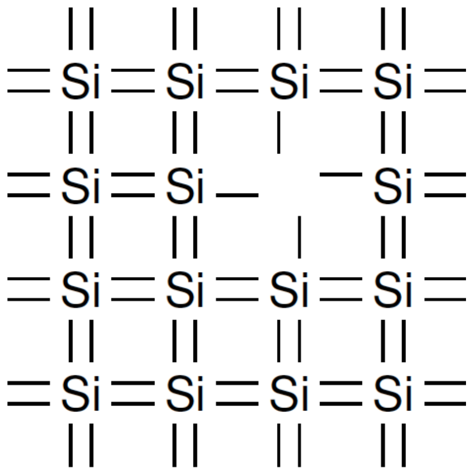
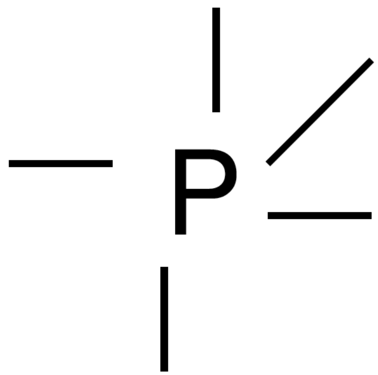
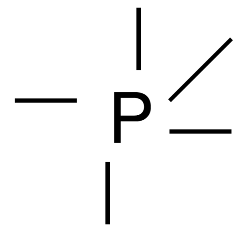
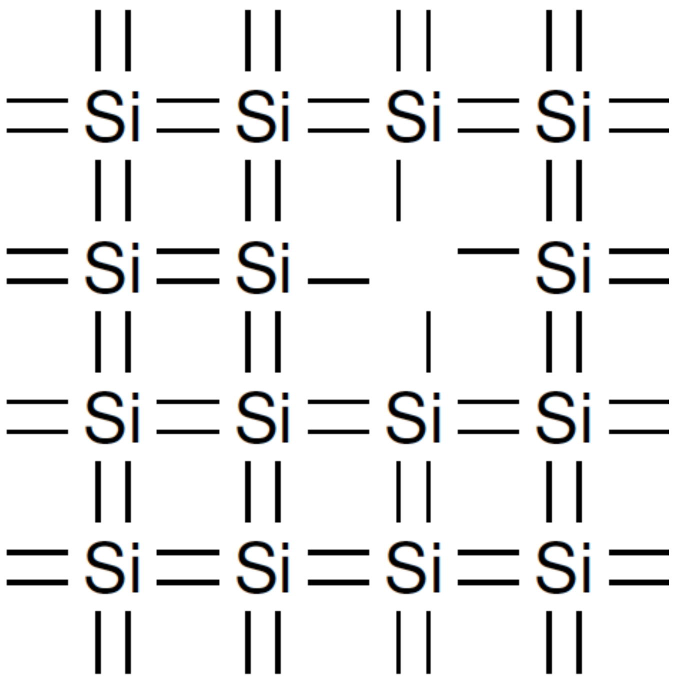
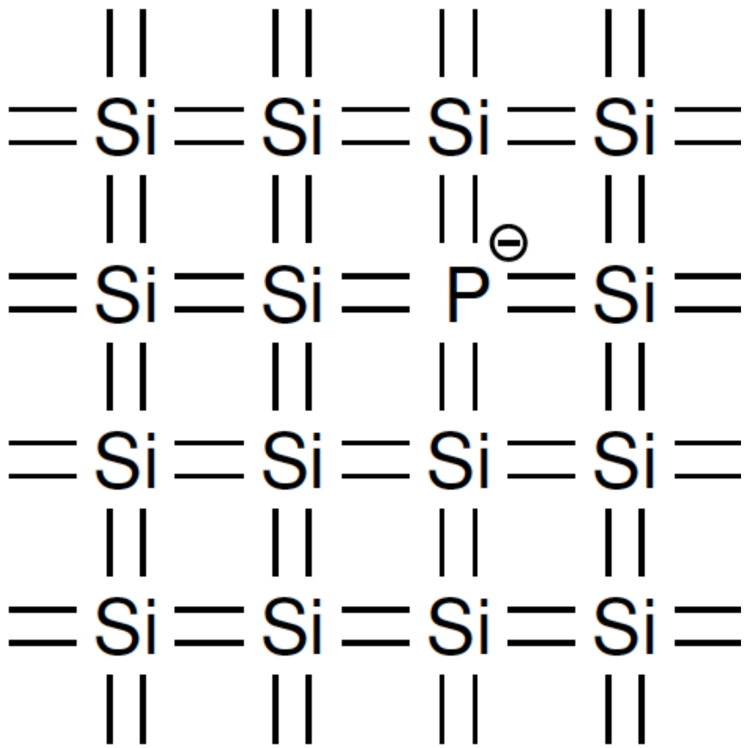




Doping with P

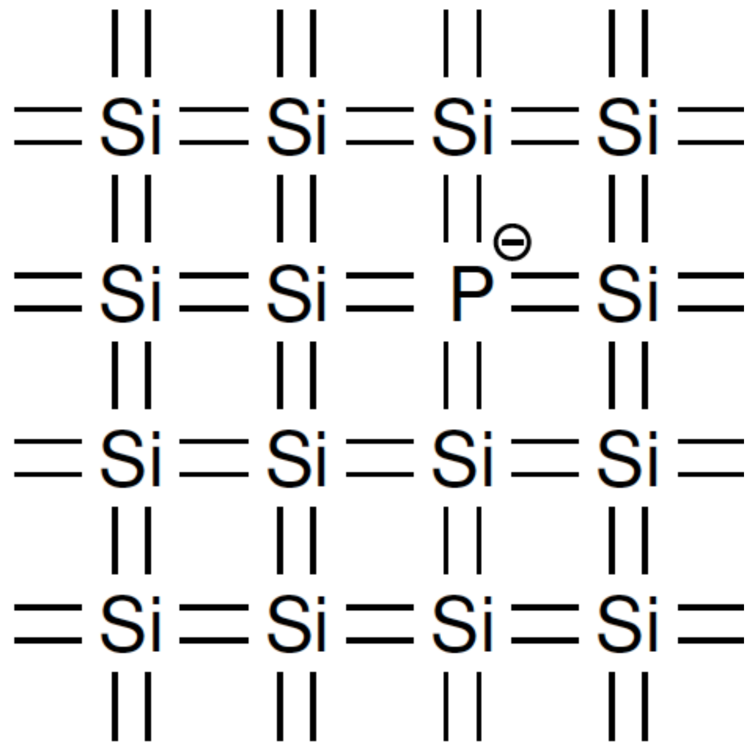






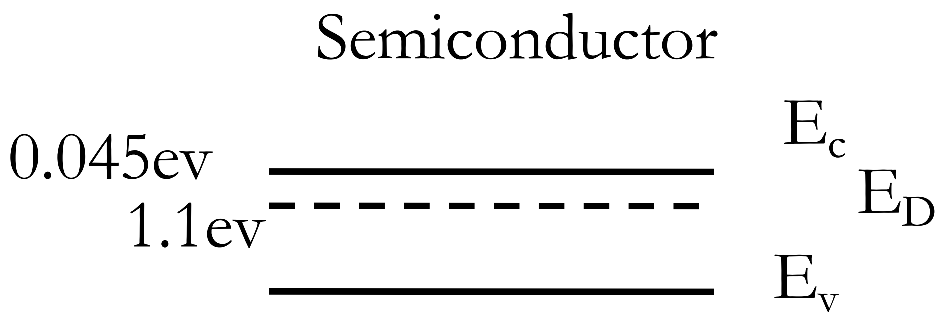
Doping with P

- End up with extra electrons
  - Donor electrons
- Not tightly bound to atom
  - Low energy to displace
  - Easy for these electrons to move



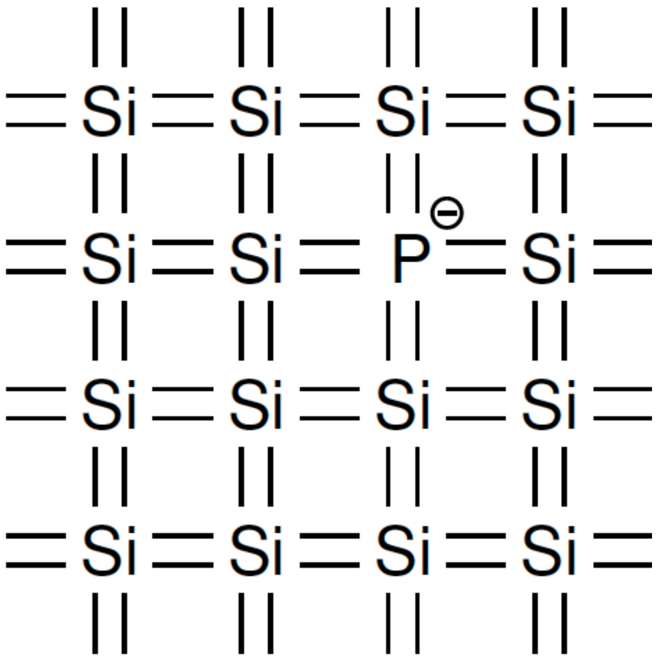
Doped Band Gaps

- Addition of donor electrons makes more metallic
  - Easier to conduct



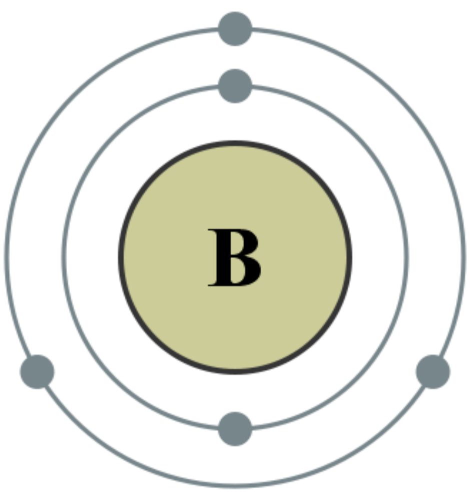
Localized

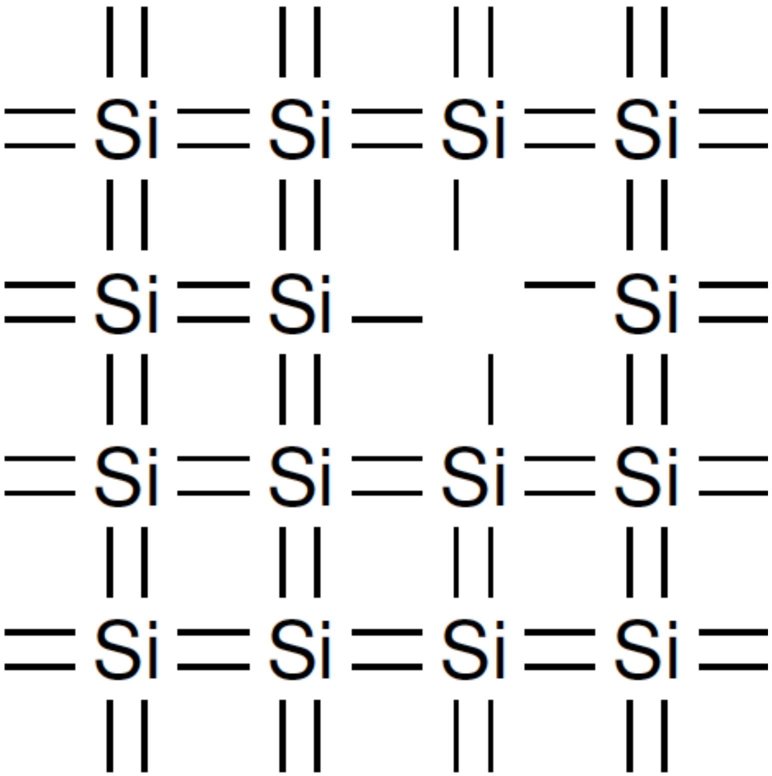
- Donor electron is localized
  - Won't go far if no low energy states nearby
- Increasing doping concentration
  - Ratio of P atoms to Si atoms
  - Decreases energy to conduct



Doping

- What happens if we replace Si atoms with group 13 atom instead?
  - E.g. B (Boron)
  - Valance band electrons?





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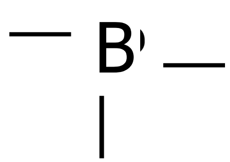
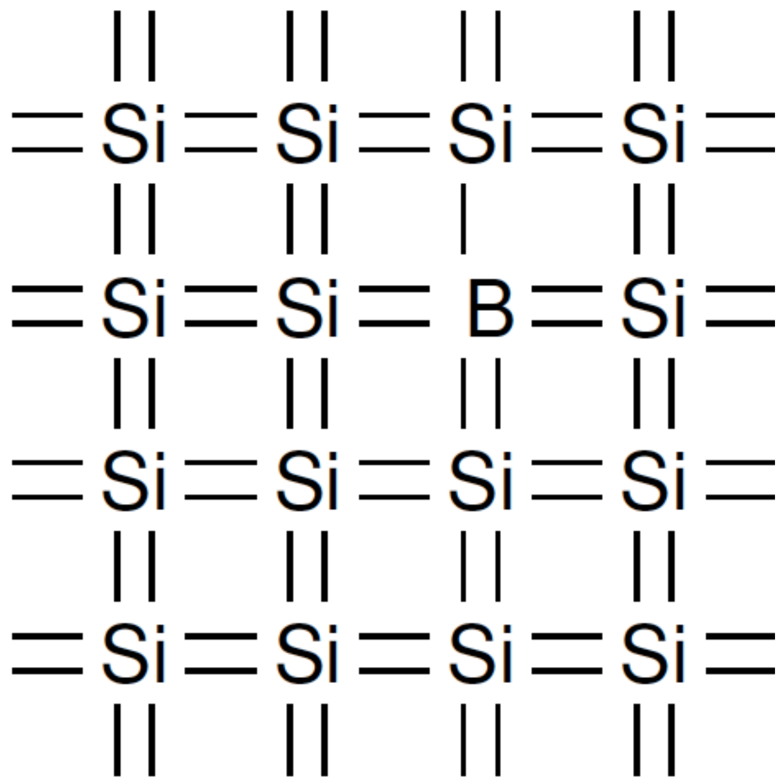
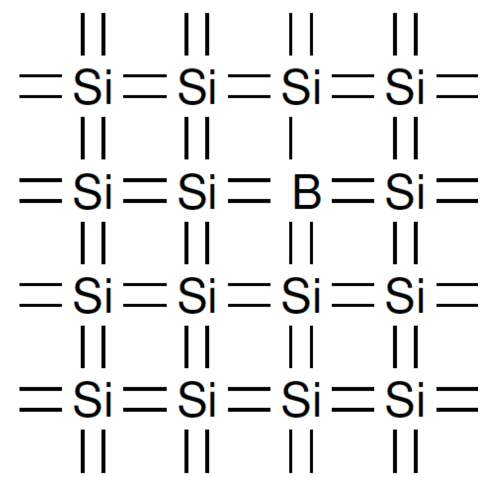




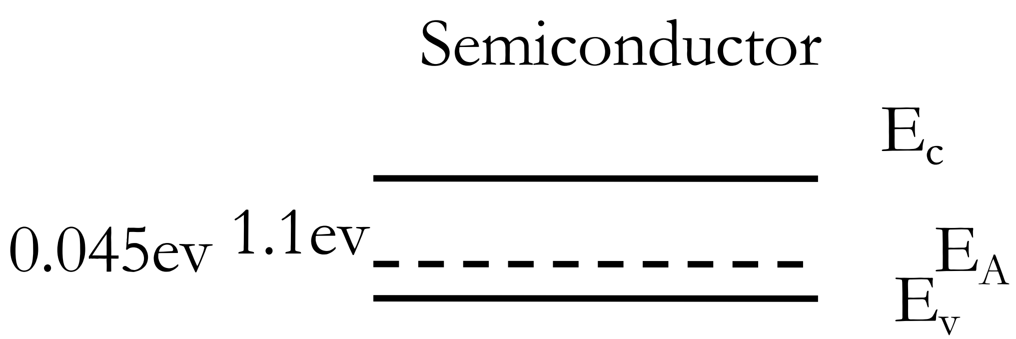
Doping with B

- End up with electron vacancies -- Holes
  - Acceptor electron sites
- Easy for electrons to shift into these sites
  - Low energy to displace
  - Easy for the electrons to move
    - Movement of an electron best viewed as movement of hole



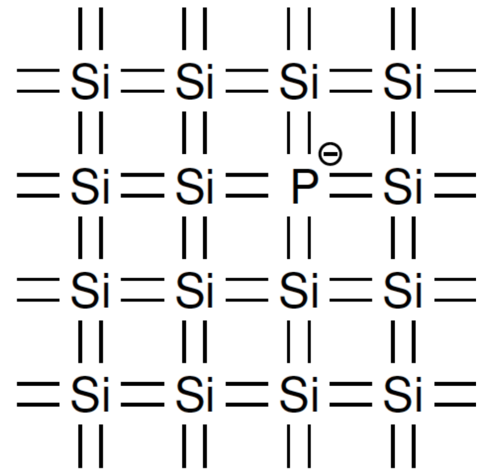
Doped Band Gaps

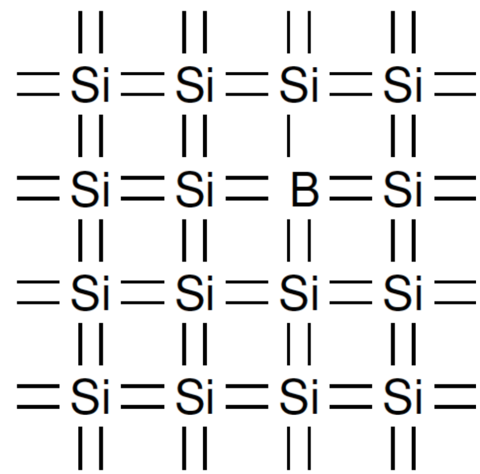
- Addition of acceptor sites makes more metallic
  - Easier to conduct



MOSFETs

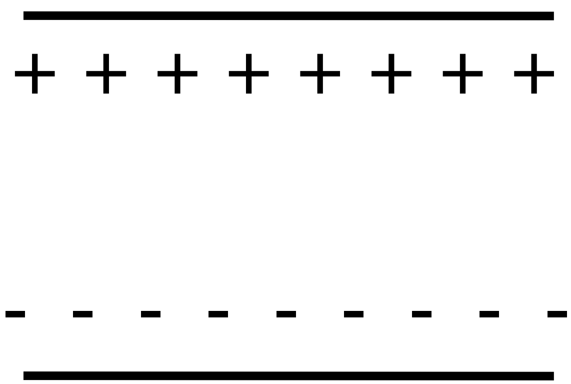
- Donor doping
  - Excess electrons
  - Negative or N-type material
  - NFET
- Acceptor doping
  - Excess holes
  - Positive or P-type material
  - PFET

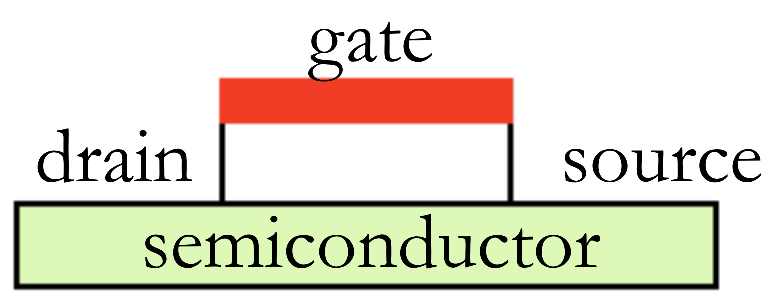




Capacitor Charge

- Remember capacitor charge

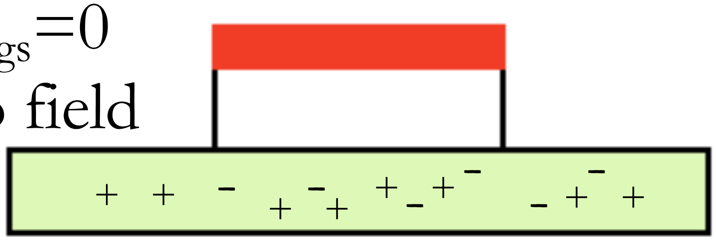




MOS Field?

- What does "capacitor" field do to the doped semiconductor channel?

V_{gs}=0
No field



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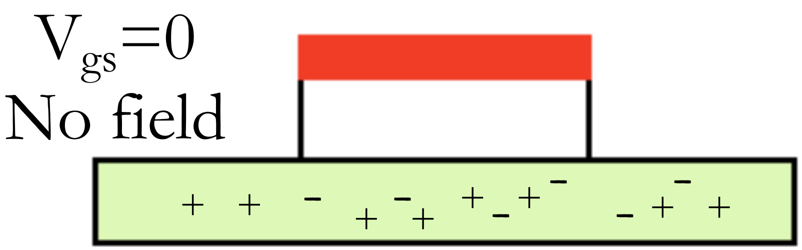

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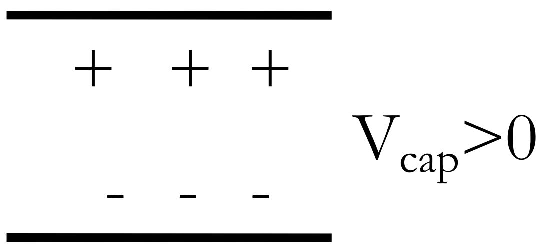

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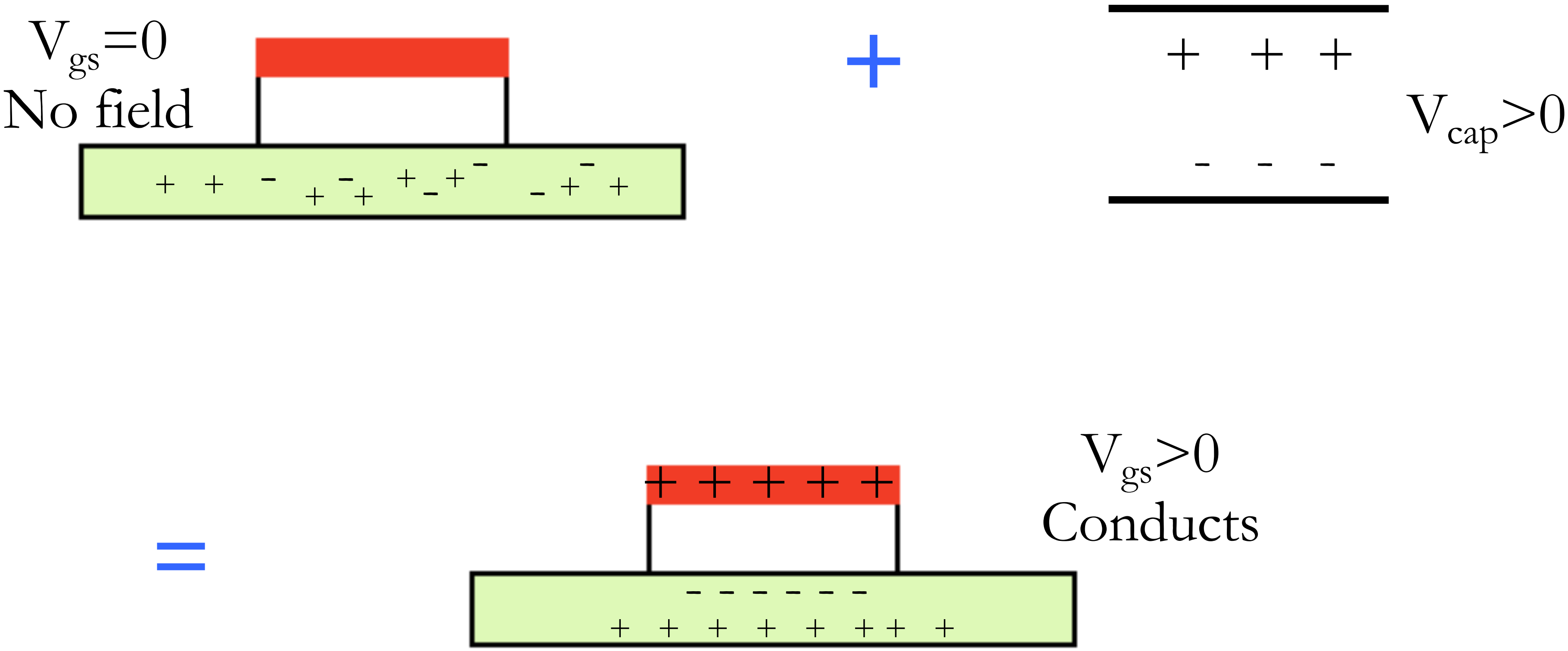

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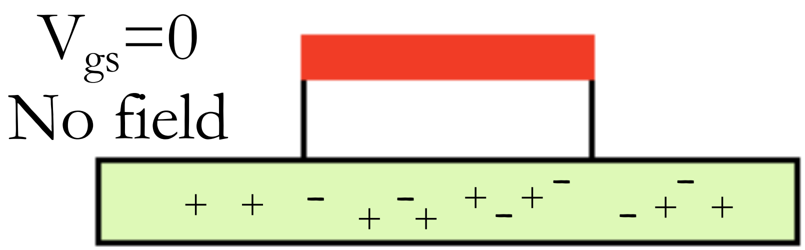

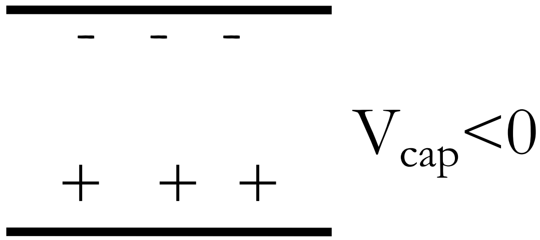

MOS Field?

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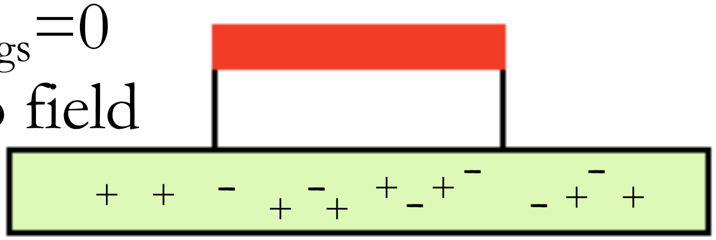
No field



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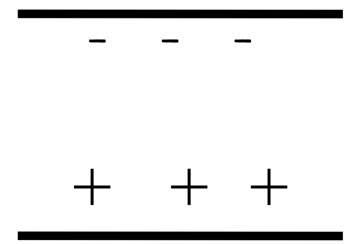
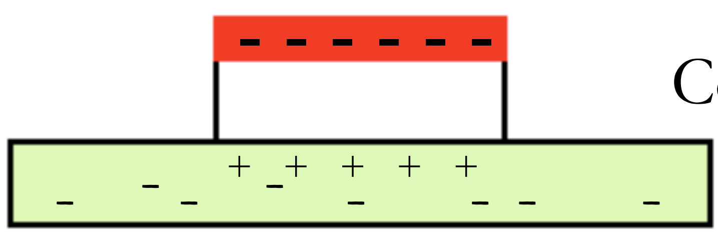


$V_{cap}<0$

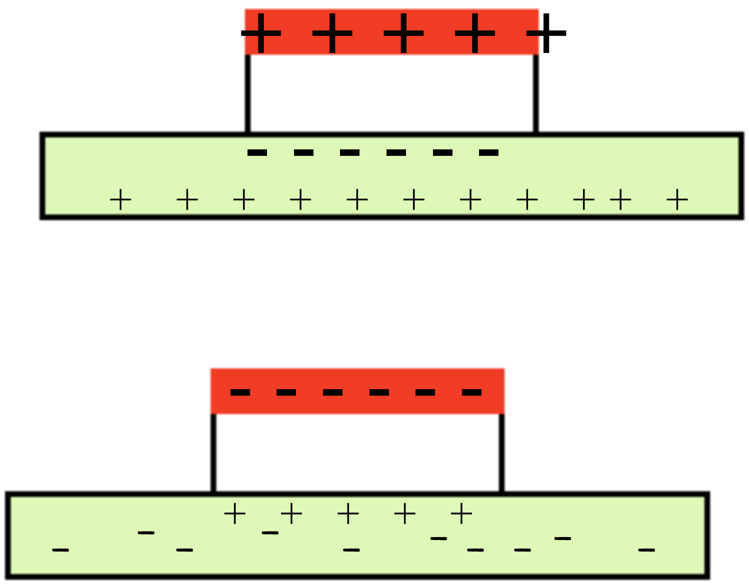
=



$V_{gs}<0$
Conducts

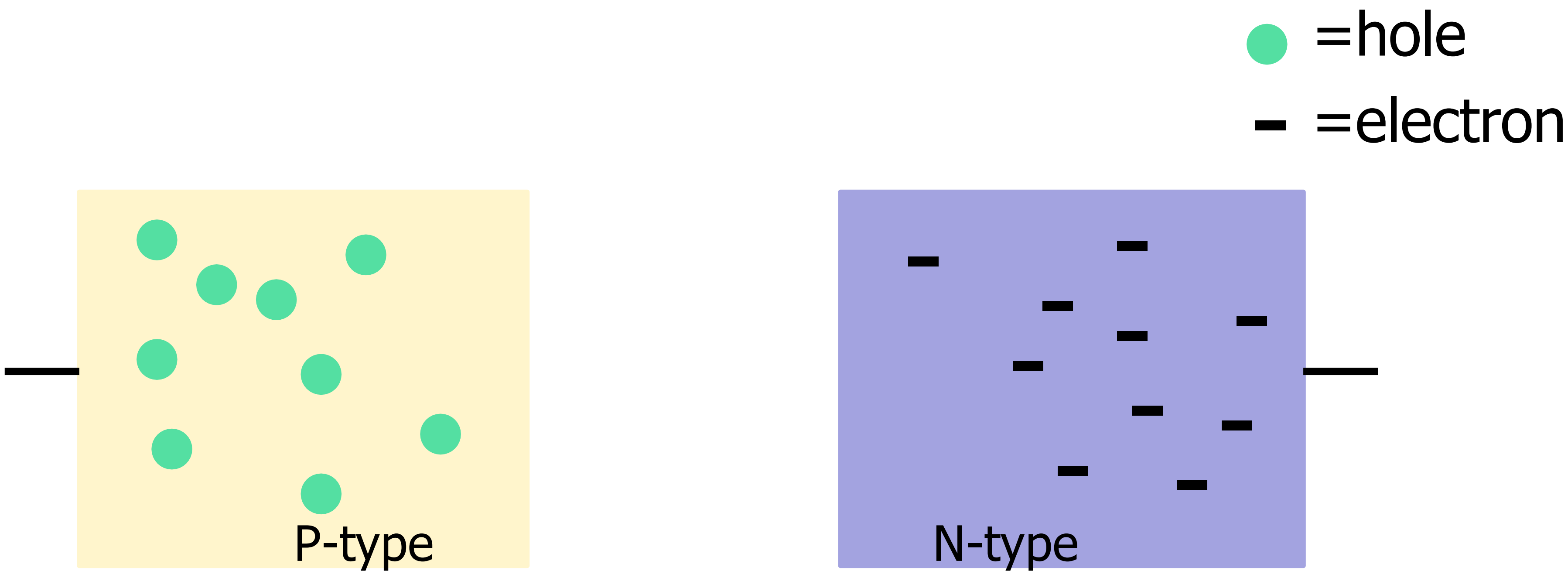
MOS Field Effect

- Charge on capacitor
  - Attract or repel charges to form channel
  - NMOS: Positive field on p-type substrate
    - Attracts electrons to surface to form conducting channel
  - PMOS: Negative fiend on n-type substrate
    - Attracts holes to surface to form conducting channel



PN Junction

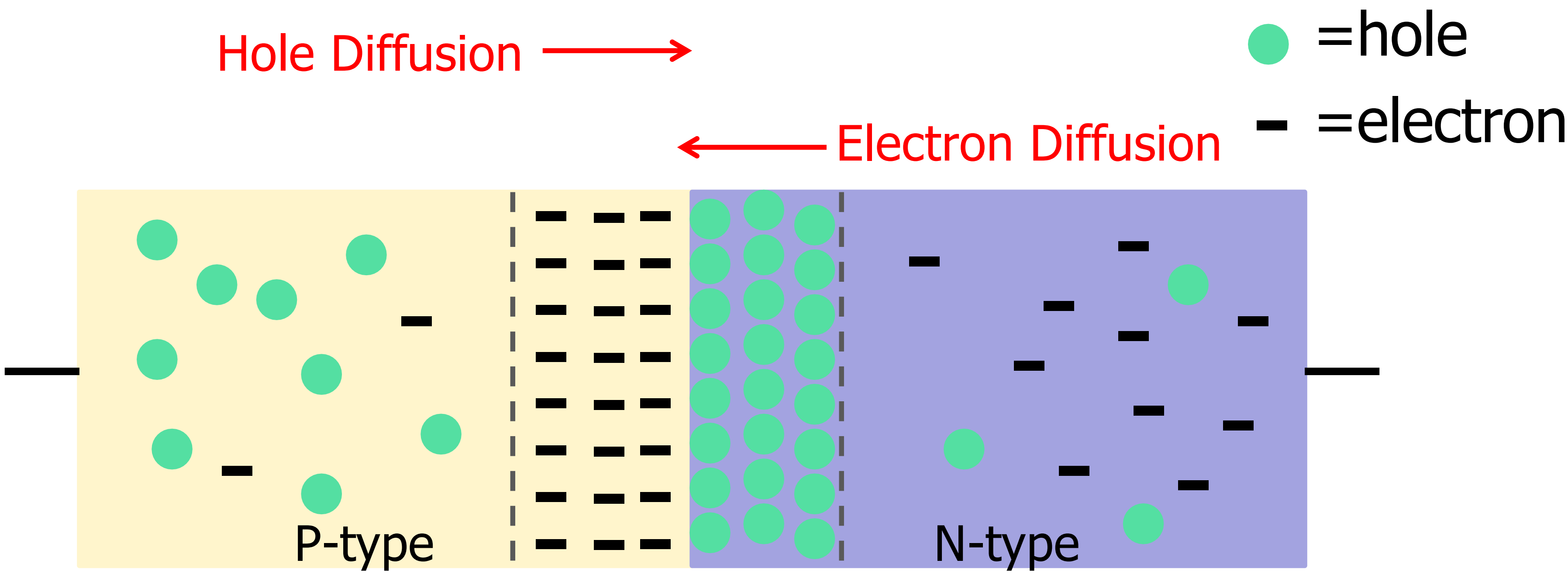
Doped Silicon



Excess holes

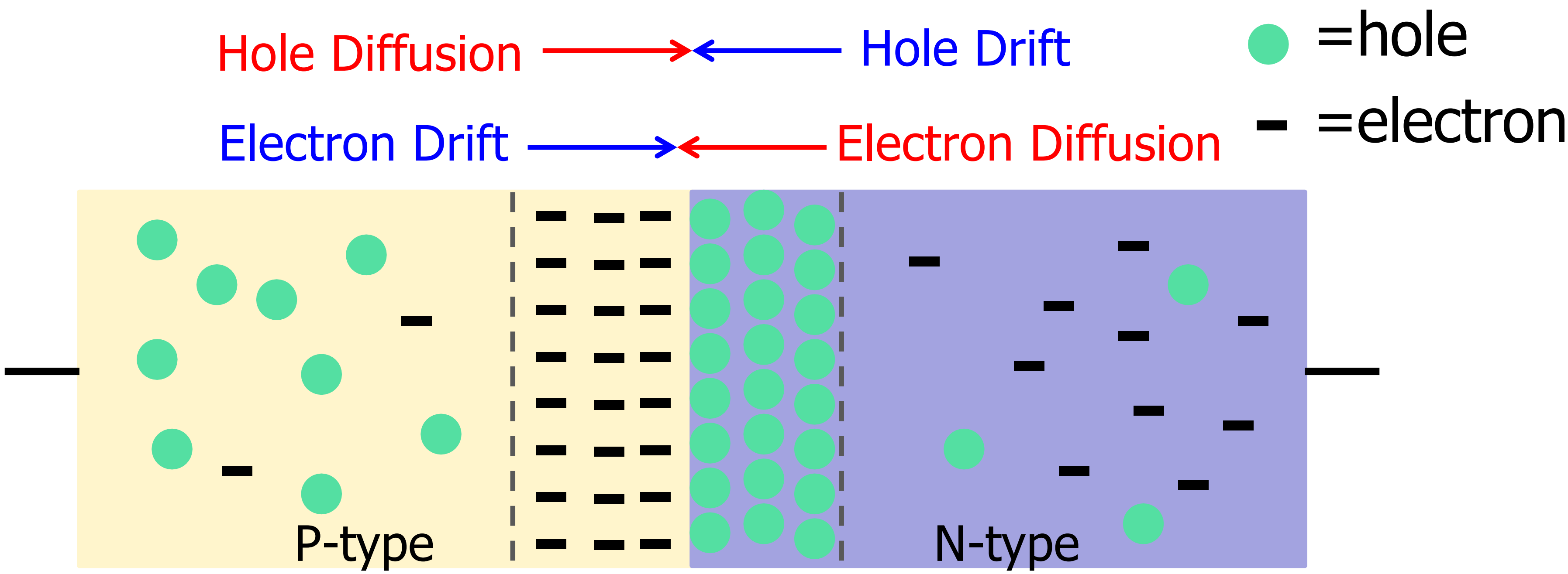
Excess electrons

PN Junction



- PN junction causes a depletion region to form
  - Electrons diffuse from N-type to P-type
  - Holes diffuse from P-type to N-type
    - Diffusion current caused by diffusion of carriers

PN Junction

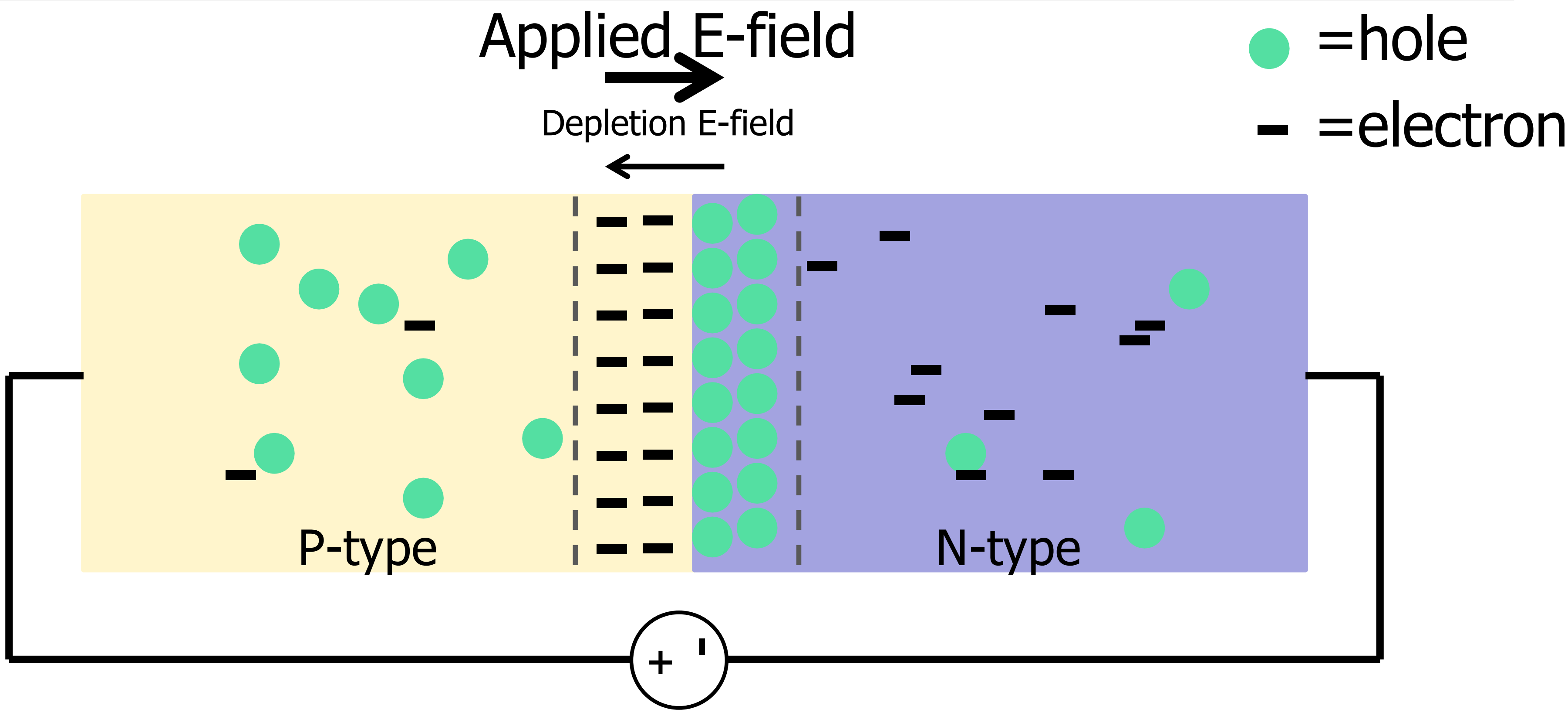


- PN junction causes a depletion region to form
  - Electrons diffuse from N-type to P-type
  - Holes diffuse from P-type to N-type
    - Diffusion current caused by diffusion of carriers
- Equilibrium achieved when V_{bi}, built-in potential, is formed across the depletion region
  - Drift current cause by E-field due to V_{bi} to counteract diffusion current

Drift/Diffusion Currents

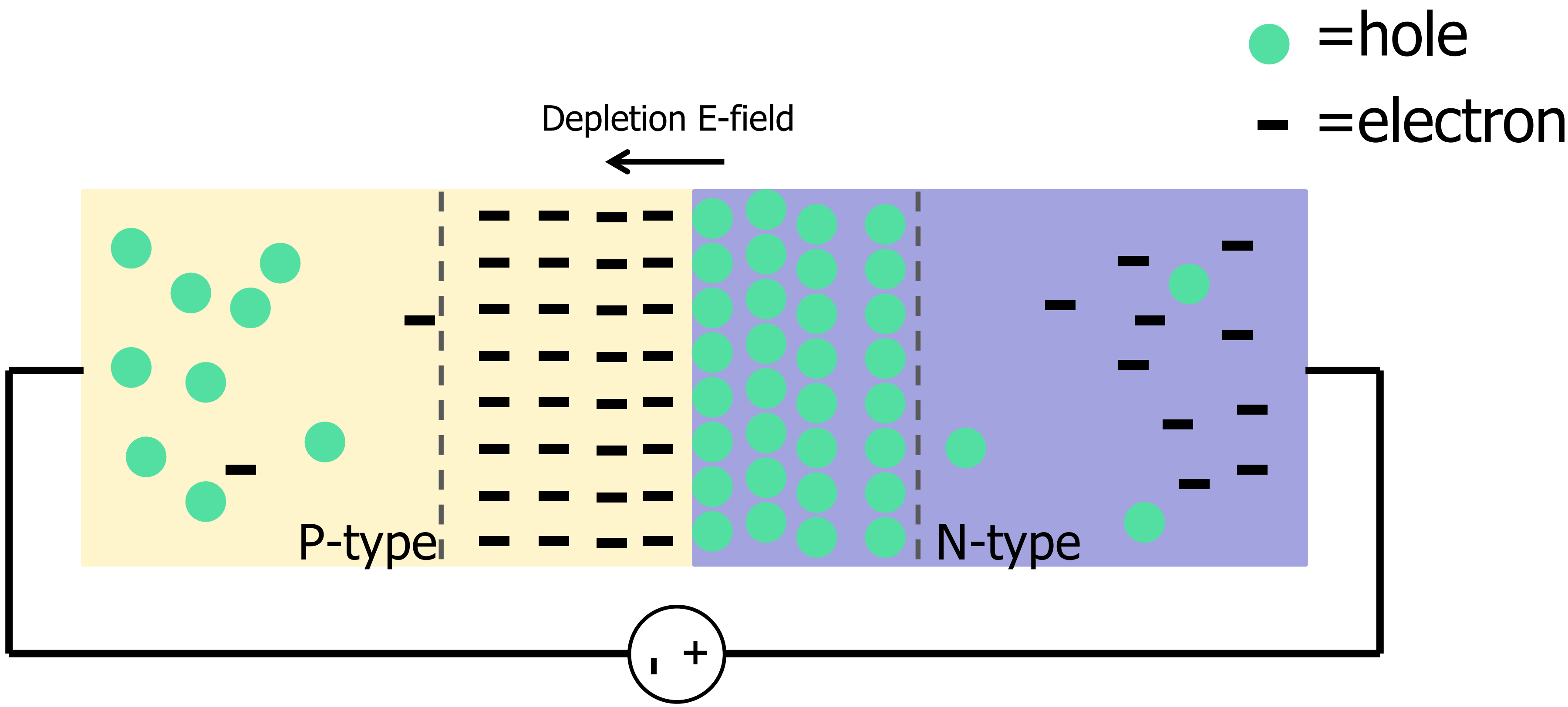
- Diffusion current
  - Current caused by semiconductor diffusion of holes and electrons
- Drift current
  - Current due to movement of holes and electrons caused by force from potential difference induced e-field

PN Junction – Forward Biasing



- Forward biasing connect positive terminal to p-type and negative terminal to n-type
  - Holes/electrons pushed towards depletion region, causing it to narrow
  - The applied voltage e-field continues to narrow the depletion region (i.e reduce the depletion e-field)
  - current flows through the device from p-type to n-type

PN Junction – Reverse Biasing



- Reverse biasing connect positive terminal to n-type and negative terminal to p-type
  - Holes/electrons attracted away from depletion region, causing it to widen
    - No current flows through the device
  - If reverse bias increases past breakdown voltage, the depletion e-field increases until breakdown occurs and reverse biased current flows causing thermal damage to junction