University of Pennsylvania
Department of Electrical and System Engineering
System-on-a-Chip Architecture

ESE532, Fall 2017 — Energy Milestone — Wednesday, November 8

Due: Friday, Nov. 17, 5:00PM

Group: Develop and validate functionality. Measure and estimate energy.

Individual: Writeup is an individual task.

1. Complete a functional implementation for the project task that can run on the Zynq ARM and produce a valid compressed output stream that works with the supplied decompressor.
   Writeup on functional implementation can build on your previous assignment and should provided complete, updated information on:
   (a) Code sources (e.g., URLs) for any open-source code you used as a starting point or as a primary reference
   (b) Current compression status and breakdown of contribution from deduplication and from LZW compression; current throughput achieved for full task.
   (c) Description of all validation performed on your current functional implementation.
2. Move some part of your design onto the FPGA for acceleration.
   Writeup should identify what you moved onto the FPGA, how you validated it, and how you tuned it. Identify the current throughput achieved and the current bottleneck(s).
3. Turn in a tar file with your functional and FPGA accelerated code to the designated assignment component in canvas.
4. Measure and report the energy to encode the Linux source code on the two implementations corresponding to Problems 1 and 2 (if you have had a chance to explore multiple design options using the FPGA for acceleration, measure the highest performing you have currently found.)
5. Estimate the energy to encode the Linux source code for the same two designs based on metrics provided by the Xilinx tools.

We don't expect significant FPGA acceleration on this milestone, but do want you to become familiar with how to measure and estimate the energy including that of the FPGA mapping so you will be prepared to characterize your more mature designs.

Measure Energy

The ZedBoard provides a current sense probe (J21). You may find this posting useful on how to use and interpret. The current sense measurement and calculation gives you power. You will need to also consider the total end-to-end runtime to compute energy. Note that this includes everything on the ZedBoard, not just the Zynq chip.

Estimate Energy

You can obtain the power by opening the Vivado project file generated by SDSoC in Vivado (like we did before to show the block diagram), and opening the *Project Summary*. The power consumption is given as *Total On-Chip Power* in the *Power* section at the bottom right. The same section also has a tab called *On-Chip* that shows the dynamic and static power. Dynamic power is further divided into clocks, signals, logic, BRAM, and PS7.