University of Pennsylvania
Department of Electrical and System Engineering
System-on-a-Chip Architecture

ESE532, Spring 2017 — HW7: Model Computation — Monday, March 13

Due: Friday, March 17, 5:00PM

In this assignment, we will model the video encoder and a potential accelerator.

Work individually on this assignment.

Homework Task

Please be concise in your answers.

1. **Modeling**

   Start with your modified `fullsearch` from HW6.

   (a) Capture an up to date profile of your encoder.

   (b) Report the total runtime for the full mpeg encoder and the runtime for the `fullsearch`.

   (c) Develop a model (in the spirit of midterm, problem 2) to explain the runtime of `fullsearch`.

   - collect data as necessary on operations performed to support your model
   - try to keep the model to major effects (read/writes from cache, read/writes from DRAM, major instruction classes)
   - likely will be useful to look at the assembly for your compiled routines

   (d) How many adds are required for the sum-of-absolute-difference computations (both difference and sum) during this same `fullsearch` runtime?

   (e) Focusing on the `dist` function, what constitutes the difference between instructions required for `dist` and the adds required for sum-of-absolute-difference computation within `dist`? Identify both number of instructions and the functionaliy provided by the instructions.

2. **Hardware Acceleration**

   (a) Design a hardware accelerator for a fully unrolled `dist` routine that is pipelined to produce one result per cycle (hierarchical schematics allowed).

   (b) How many adder bits does the hardware `dist` accelerator require?

   (c) How many register bits does the hardware `dist` accelerator require?

   (d) Use BRAMs for line buffers. Assuming a line fits in a BRAM (18Kb BRAM can hold up to 2K 8b pixels), show how BRAMs interface with the hardware accelerator so that the complete unit with BRAMs and accelerator needs only one pixel input per output. (This is thinking about data movement beyond a single `dist` call. Think about the sequence of `dist` calls within `fullsearch`.)

   (e) Provide a revised timing model for the ARM processor working with the hardware accelerator and estimate the potential speedup. Assume the BRAMs operating at 500 MHz are the limitation to the cycle time on the accelerator. Provide revisions to `fullsearch` as necessary to show how the accelerator is integrated.

   (f) Compare the resources required by this accelerator (LUTs (assume one LUT per adder bit), registers, BRAMs) with the resources available on the Zynq FPGA programmable logic fabric.

   (g) With the accelerator in place, where is the bottleneck in the computation?

3. **Reflect**

   (a) How does the performance of this modeled accelerator relate to your solution to HW6?

   (b) Using your model and data from HW6, identify potential sources of mismatch.