University of Pennsylvania
Department of Electrical and System Engineering
System-on-a-Chip Architecture

ESE532, Spring 2017 — Energy Milestone — Friday, April 7

Due: Friday, April 14, 5:00PM

Group: Measure and estimate energy.

Individual: Writeup.

1. Measure the energy to encode a frame for your current best (highest performing) design and the original baseline design.
2. Estimate the energy to encode a frame for the same two designs based on metrics provided by the Xilinx tools.

- Our original plan was to ask that you try to push up the frequency of your accelerator. From our experimentation, it looks like some of the SDSoC infrastructure (e.g., Data Movers) often end up limiting the accelerator frequency to about 200 MHz rather than the accelerator logic. As such, we cannot currently suggest a path to reliably achieving higher frequencies. If you are seeing frequencies well below 200 MHz, we suspect you can push them up to 200 MHz, and we leave it to your discretion to decide if that is a useful place to spend your design optimization time.

Measure Energy

The ZedBoard provides a current sense probe (J21). You may find this posting useful on how to use and interpret. The current sense measurement and calculation gives you power. You will need to also consider the total end-to-end runtime to compute energy. Note that this includes everything on the ZedBoard, not just the Zynq chip.

Estimate Energy

You can obtain the power by opening the Vivado project file generated by SDSoC in Vivado (like we did before to show the block diagram), and opening the *Project Summary*. The power consumption is given as *Total On-Chip Power* in the *Power* section at the bottom right. The same section also has a tab called *On-Chip* that shows the dynamic and static power. Dynamic power is further divided into clocks, signals, logic, BRAM, and PS7.