University of Pennsylvania
Department of Electrical and System Engineering
System-on-a-Chip Architecture

ESE532, Spring 2017 MPEG Encoder Project Monday, March 20

Due: Friday, April 21, 5:00PM

1 Goal

Accelerate MPEG Encoding as much as possible (we expect 10–100× over -O3 HW6 software-on-ARM baseline) and estimate the requirements for a custom chip that would achieve real-time performance for 1080p30 video (1920×1080 at 30 fps). Benchmark is for full compression not including the loading and storing of frames and configuration. Note that we made a bugfix to the encoder, so please download an updated version here.

This is a 5 week project assignment; the intent is to allow you to plan and execute a significant, open-ended design exploration and mapping. You will not achieve the implementation goal or the course learning goals by trying to do this in one week. We give you milestones to help provide some structure, but the milestones are minimal and doing the minimum to hit the milestone each week will be insufficient to get you where you need to be at the end. We are giving you flexibility in planning and ordering rather than lock-step specifying exactly what you need to do each week.

2 Final Report

- Describe your final Zynq XC7Z020 mapped design. [5 pages]
  - Performance achieved and energy required
  - Key design aspects: task decomposition, parallelism, mapping to Zynq resources, include diagrams to support
  - Model to explain performance, area, and energy of design
  - Current bottleneck preventing higher performance
- Describe design that achieves real-time and estimate chip area and costs. [3 pages]
  - Key design aspects. Build on description in first section, describing differences for this design from the Zynq XC7Z020 design
  - Use or expand model introduced in first section to show how you meet real time for the 1920×1080 at 30 fps encoding problem
  - Custom implementation area estimate with area model support
- Describe the key lessons you learned from this design experience. [1 page]
- Describe design space explored and show graphs and models to support design selection. [any number of pages as needed]
- Describe who did what. [1 page]

3 Milestones

We will provide precise requirements for milestones each week. These may include a few exercises to help prepare you for questions that may be on the final in addition to the project specific components. Milestones and feedback feed into the final report. In most cases, the milestones can serve as a first draft of a component of your report, and the feedback we give you will help provide guidenace on how to refine it for the report.

- Analysis and teaming [3/24]
- Parallelism and design space [3/31]
- Minimum performance improvement of 4× and custom area estimates for that design [4/7] (intervening lectures and this milestone specifications will specify area model)
- Energy estimate and cycle time improvement [4/14] (intervening lectures and this milestone specification will clarify what we want for energy model)
- Final Report [4/21]

4 Ground Rules

- Project work is done in teams of 2. You select partners during first week.
- Collaboration between teams is limited as specified on the course web page.
- Individual milestone and final writeups, including individual solution of exercises.