

University of Pennsylvania
Department of Electrical and System Engineering
Computer Organization

ESE534, Spring 2012

HW1: Logic

Wednesday, January 11

Due: Monday, January 23, 12:00PM

For all assignments in this class: Writeups *must* be done in electronic form and submitted through blackboard. Use CAD or drawing tools where appropriate. **Handwritten assignments and hand-drawn figures are not acceptable.**

You may use hierarchical schematics. Use of a schematic drawing program for circuits is encouraged.

1. Implement $A > B$ out of 2-input NAND gates
 - (a) Design the bit slice that takes in $A[i]$, $B[i]$ and two bits from the next more significant bit slice ($i + 1$) and produces two bits that communicate to the next less significant bit slice ($i - 1$).
 - (b) Show how the bit slices compose for 4b unsigned numbers.
2. Using your comparison function from Problem 1, show logic for a spatial sorting function to sort 4, 4-bit inputs into ascending order.
3. Consider all two-input functions. (How many functions are there?)
For each function, identify if the function is universal. You may tie the inputs of a function to a constant 0 or 1. You may connect the same signal into both gate inputs. Your writeup should be a table, with the following entries for each two-input function:
 - list on-set minterms (*i.e.* the truth table)
 - logic expression for function
 - universal?
 - explanation of why or why not
4. Counting each gate as unit size, give an upper bound on the size ratio between:
 - an implementation that uses only 2-input NOR gates
 - an optimal implementation of an arbitrary n -input function when the implementation may use an optimal mixture of the full set of 2-input functions from Problem 3 as gates